ETCHED NANOFIN TRANSISTORS

Cross Reference To Related Applications

Benefit of priority is hereby claimed to "Nanowire Transistor With Surrounding Gate," U.S. Application Serial No. 11/397,527, filed on April 4, 2006; "Grown Nanofin Transistors," U.S. Application Serial No. 11/397,430, filed on April 4, 2006; "DRAM With Nanofin Transistors," U.S. Application Serial No. 11/397,413, filed on April 4, 2006; and "Tunneling Transistor With Sublithographic Channel," U.S. Application Serial No. 11/397,406, filed on April 4, 2006, which applications are herein incorporated by reference.

Technical Field

This disclosure relates generally to semiconductor devices, and more particularly, to nanofin transistors.

Background

The semiconductor industry has a market driven need to reduce the size of devices, such as transistors, and increase the device density on a substrate. Some product goals include lower power consumption, higher performance, and smaller sizes. FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k. The continuous scaling of MOSFET technology to the deep sub-micron region where channel lengths are less than 0.1 micron (100 nm or 1000 Å) causes significant problems in the conventional transistor structures. For example, junction depths should be much less than the channel length. Thus, with reference to the transistor 100 illustrated in FIG. 1, the junctions depths 101 should be on the order of a few hundred Angstroms for channels lengths 102 that are approximately 1000 Å long. Such shallow junctions are difficult to form by conventional implantation and diffusion techniques. Extremely high levels of channel doping are required to suppress short-channel effects such as drain induced barrier lowering, threshold

voltage roll off, and sub-threshold conduction. Sub-threshold conduction is particularly problematic in DRAM technology as it reduces the charge storage retention time on the capacitor cells. These extremely high doping levels result in increased leakage and reduced carrier mobility. Thus, the expected improved performance attributed to a shorter channel is negated by the lower carrier mobility and higher leakage attributed to the higher doping.

Leakage current is a significant issue in low voltage and lower power battery-operated CMOS circuits and systems, and particularly in DRAM circuits. The threshold voltage magnitudes are small to achieve significant overdrive and reasonable switching speeds. However, as illustrated in FIG. 2, the small threshold results in a relatively large sub-threshold leakage current.

Some proposed designs to address this problem use transistors with ultra-thin bodies, or transistors where the surface space charge region scales as other transistor dimensions scale down. Dual-gated or double-gated transistor structures also have been proposed to scale down transistors. As commonly used in the industry, "dual-gate" refers to a transistor with a front gate and a back gate which can be driven with separate and independent voltages, and "double-gated" refers to structures where both gates are driven when the same potential. An example of a double-gated device structure is the FinFET. "TriGate" structures and surrounding gate structures have also been proposed. In the "TriGate" structure, the gate is on three sides of the channel. In the surrounding gate structure, the gate surrounds or encircles the transistor channel. The surrounding gate structure provides desirable control over the transistor channel, but the structure has been difficult to realize in practice.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, and front and back gates separated from a semiconductor body by gate insulators, and also illustrates an electric field generated by the drain. Some characteristics of the dual-gated and/or double-gated MOSFET are better than the conventional bulk silicon MOSFETs, because compared to a single gate, the two gates better screen the electric field generated by the drain electrode from the source-end of the

channel. The surrounding gate further screens the electric field generated by the drain electrode from the source. Thus, sub-threshold leakage current characteristics are improved, because the sub-threshold current is reduced more quickly as the gate voltage is reduced when the dual-gate and/or double gate MOSFET turns off. FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, or surrounding gates MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

FIGS. 5A-C illustrate a conventional FinFET. FIG. 5A illustrates a top view of the FinFET and FIG. 5B illustrates an end view of the FinFET along line 5B-5B. The illustrated FinFET 503 includes a first source/drain region 504, a second source/drain region 505, and a silicon fin 506 extending between the first and second source/drain regions. The silicon fin functions as a transistor body, where the channel between the first and second source/drain regions is horizontal. A gate insulator 507, such as silicon oxide, is formed over the fin, and a gate 508 is formed over the fin after the oxide is formed thereon. The fin of the illustrated conventional FinFET is formed over buried oxide 509. FIG. 5C illustrates a conventional etch technique for fabricating the fin for the FINFET. As illustrated in FIG. 5C, the fin width is defined by photolithography or e-beam lithography and etch. Thus, the fin width is initially a minimum feature size (1F). The width of the fin is subsequently reduced by oxidation or etch, as illustrated by arrows 510.

Summary

Aspects of the present subject matter use a sidewall spacer technique to etch ultrathin nanofins into a wafer, and fabricate nanofin transistors with surrounding gates using these etched nanofins. Various embodiments etch silicon nanofins in a silicon substrate. The silicon nanofins are used as the body regions of CMOS transistors where both the thickness of the body of the transistor and channel length have dimensions smaller than lithographic

dimensions. For example, some embodiments provide ultrathin nanofins with a thickness on the order of 20 nm to 50 nm.

One aspect of the present subject matter relates to a method for forming a transistor. According to an embodiment, a fin is formed from a crystalline substrate. A first source/drain region is formed in the substrate beneath the fin. A surrounding gate insulator is formed around the fin. A surrounding gate is formed around the fin and separated from the fin by the surrounding gate insulator. A second source/drain region is formed in a top portion of the fin. Various embodiments etch a hole in a layer over the substrate, form sidewall spacers in the hole, form a fin pattern from the sidewall spacers, and etch into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern.

An aspect relates to a transistor. A transistor embodiment includes a crystalline substrate with trenches etched therein to form a crystalline semiconductor fin from the substrate, a first source/drain region formed in the crystalline substrate at a bottom of the fin and a second source/drain region formed in a top portion of the fin to define a vertically-oriented channel region in the fin between the first and second source/drain regions. The transistor also includes a gate insulator formed around the fin, and a surrounding gate formed around and separated from the fin by the gate insulator. The fin has a cross-sectional dimension that is less than a minimum feature size.

These and other aspects, embodiments, advantages, and features will become apparent from the following description of the present subject matter and the referenced drawings.

Brief Description of the Drawings

FIG. 1 illustrates general trends and relationships for a variety of device parameters with scaling by a factor k.

FIG. 2 illustrates sub-threshold leakage in a conventional silicon MOSFET.

FIG. 3 illustrates a dual-gated MOSFET with a drain, a source, front and back gates separated from a semiconductor body by gate insulators, and an electric field generated by the drain.

FIG. 4 generally illustrates the improved sub-threshold characteristics of dual gate, double-gate, and surrounding gate MOSFETs in comparison to the sub-threshold characteristics of conventional bulk silicon MOSFETs.

FIGS. 5A-C illustrate a conventional FINFET.

FIGS. 6A-6L illustrate a process for forming a nanofin transistor, according to various embodiments of the present subject matter.

FIG. 7 illustrates a top view of a layout of nanofins for an array of nanofin transistors, according to various embodiments.

FIG. 8 illustrates a process to fabricate a nanofin transistor, according to various embodiments of the present subject matter.

FIG. 9 illustrates a process to form a fin from a crystalline substrate, according to various embodiments of the present subject matter.

FIG. 10 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter.

FIG. 11 illustrates a diagram for an electronic system having one or more nanofin transistors, according to various embodiments.

FIG. 12 depicts a diagram of an embodiment of a system having a controller and a memory.

Detailed Description

The following detailed description refers to the accompanying drawings which show, by way of illustration, specific aspects and embodiments in which the present subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present subject matter. The various embodiments of the present subject matter are not necessarily mutually exclusive as aspects of one embodiment can be combined

with aspects of another embodiment. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present subject matter. In the following description, the terms "wafer" and "substrate" are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art. The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side", "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Disclosed herein are nanofin transistors, and a fabrication technique in which nanofins are etched into a substrate or wafer and used to make single crystalline nanofin transistors. The following discussion refers to a silicon nanofin embodiment. Those of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to form nanofins using other semiconductors. Aspects of the present subject matter provide nanofin transistors with vertical channels, where there is a first source/drain region at the bottom of the fin and a second source/drain region at the top of the fin. FIGS. 6A-6L illustrate a process for forming a nanofin transistor, according to various embodiments of the present subject matter.

Silicon nitride is deposited on a silicon wafer, and the silicon nitride is covered with a layer of amorphous silicon (a-silicon). FIG. 6A illustrates a side view of the structure 611 after holes 612 are defined in the amorphous silicon 613 and sidewall spacers 614 are formed. The holes 612 extend to the silicon nitride layer 615, which lies over a substrate 616 such as a silicon wafer. Various embodiments form the sidewall spacers by oxidizing the amorphous silicon. FIG. 6B illustrates a side view of the structure 611, after the structure is covered with a thick layer of amorphous silicon 616. FIG. 6C illustrates the structure 611 after the structure is planarized, illustrated by the arrow, at least to a level to remove the oxide on top of the amorphous silicon. The structure can be planarized using a chemical mechanical polishing (CMP) process, for example. This leaves an elongated rectangular pattern, also referred to as a "racetrack" pattern, of oxide 614 exposed on the surface. The width of the pattern lines is determined by the oxide thickness rather than masking and lithography. For example, the oxide thickness can be within a range on the order of 20 nm to 50 nm, according to various embodiments.

FIG. 6D illustrates a mask over the racetrack pattern, which selectively covers portions of the oxide and exposes other portions of the oxide. The exposed oxide portions, illustrated by the shaded strips, are removed. An etch process, such as a potassium hydroxide (KOH) etch, is performed to remove the amorphous silicon. The oxide, or the portions of the oxide remaining after the mask and etch illustrated in FIG. 6D, protects the nitride during the etch. After the amorphous silicon is removed the nitride 615 can be etched, followed by a directional silicon etch that etches the wafer 616 to a predetermined depth below the nitride layer. The nitride pattern protects the local areas of silicon from the etch, resulting in silicon fins 617 of silicon protruding from the now lower surface of the silicon wafer, as illustrated in FIG. 6E. FIGS. 6F and 6G illustrate top and side views of the structure, after the tops of the fins and trenches at the bottom of the fins are implanted with a dopant. As illustrated in FIG. 6F, the dopant in the trench forms a conductive line 618 (e.g. source line). The dopant

also forms a source/drain region at the bottom or a bottom portion of the fin. Because the fins are extremely thin, the doping in the trench is able to diffuse completely under the fins. The strips can be in either the row or column direction.

FIG. 6H illustrates the structure 611 after a gate insulator 619 has been formed around the fin 617, and a gate material 620 is formed around and separated from the fin by the gate insulator. For example, an embodiment oxidizes the silicon fins using a thermal oxidation process. The gate material 620 may be polysilicon or metal, according to various embodiments.

FIGS. 6I and 6J illustrate a top view and a cross-section view along line 6J-6J, respectively, of a first array embodiment. The structure 611 is backfilled with an insulator 621 (e.g. oxide) and trenches are created on the sides of the fins. Gate wiring material 622, such as polysilicon or metal, can be deposited and directionally etched to leave on the sidewalls only and contacting the surrounding gates 620 for the fins. The gate material and gate wiring material can be etched to recess it below the tops of the fins. The whole structure can be again backfilled with oxide and planarized to leave only oxide on the surface. Contact openings and drain doping regions can then be etched to the top of the pillars and drain regions implanted and metal contacts to the drain regions made by conventional techniques. In this case, the metal wiring could run in the "x-direction" and the buried source wiring could run perpendicular to the plane of the paper in the illustration.

FIGS. 6K and 6L illustrate a top view and a cross-section view along 6L-6L, respectively, of a second array embodiment. The structure 611 is backfilled with an insulator 621 (e.g. oxide) and trenches are created along the side of the fins 617, in the "y-direction". Gate wiring material 622, such as polysilicon or metal, can be deposited and directionally etched to leave on the sidewalls only and contacting the gates on the fins. The gate material and gate wiring material can be etched to recess it below the tops of the fins. The whole structure can be backfilled with an insulator (e.g. oxide) and planarized to leave only oxide on the

surface. Contact openings and drain doping regions can then be etched to the top of the pillars and drain regions implanted and metal contacts to the drain regions made by conventional techniques. In this case, the metal wiring could run perpendicular to the plane of the paper in the illustration and the buried source wiring could run in the "x-direction".

In both the first and second array embodiments, the buried source/drains can be implanted before the formation of the surrounding gate insulator and surrounding gate. FIG. 6L illustrates one of the completed fin structures with drain/source regions 623 and 624, recessed gates 620, and source/drain region wiring 618. These nanofin FET's can have a large W/L ratio and will conduct more current than nanowire FET's.

FIG. 7 illustrates a top view of a layout of nanofins for an array of nanofin transistors, according to various embodiments. The figure illustrates two "racetracks" of sidewall spacers 714, and further illustrates the portions of the sidewall spacers removed by an etch. The holes used to form the sidewall spacer tracks were formed with a minimum feature size (1F). The mask strips 725 have a width of a minimum feature size (1F) and are separated by a minimum feature size (1F). In the illustrated layout, the columns of the nanofins have an approximately 2F center-to-center spacing, and the rows of the nanofins have an approximately 1F center-to-center spacing. Also, as illustrated in FIG. 7, since the nanofins are formed from sidewall spacers on the walls of the holes, the center-to-center spacing between first and second rows will be slightly less than 1F size by an amount corresponding to the thickness of the nanofins (1F - ΔT), and the center-to-center spacing between second and third rows will be slightly more than 1F by an amount corresponding to the thickness of the nanofins (1F + ΔT). In general, the center-to-center spacing between first and second rows will be slightly less than a feature size interval (NF) by an amount corresponding to the thickness of the nanofins (NF - ΔT), and the center-to-center spacing between second and third rows will be slightly more than a feature size interval (NF) by an amount corresponding to the thickness of the nanofins (NF + ΔT).

FIG. 8 illustrates a process to fabricate a nanofin transistor, according to various embodiments of the present subject matter. At 826, a fin is formed from a crystalline substrate. For example, the fins can be etched from a wafer, such as a silicon wafer. At 827, a first source/drain region is formed in the substrate at the bottom of the fins. Because the fin is thin, the dopant is able to diffuse underneath the entire footprint of the fin. At 828, a surrounding gate insulator is formed around the fin; and at 829, surrounding gate is formed around and separated from the fin by surrounding the gate insulators. The resulting structure is backfilled with an insulator at 830. Trench(es) are etched and gate line(s) are formed adjacent to and in contact with the surrounding gate, as illustrated at 831. Some embodiments form two gate lines in contact with opposite sides of the surrounding gate. The gate lines can be oriented to contact the surrounding gate on a long side of the nanofin structure, or can be oriented to contact the surrounding gate on a short side of the nanofin structure. That is, the gate line(s) can be formed in the column or row directions. At 832, a second source/drain region is formed in a top portion of the fins, and contacts for the second source/drain regions are formed at 833.

FIG. 9 illustrates a process to form a fin from a crystalline substrate, such as illustrated at 826 in FIG. 8, according to various embodiments of the present subject matter. A layer is formed over the crystalline substrate at 934, and holes are etched or otherwise formed in the layer at 935. In various embodiments, the layer formed over the crystalline substrate is a layer of amorphous silicon, with a layer of silicon nitride sandwiched between the crystalline substrate and the amorphous silicon, and a hole is etched to the layer of silicon nitride. At 936, sidewall spacers are formed in the hole against a wall of the layer that defines the periphery of the hole. Various embodiments oxide the amorphous silicon layer to form the sidewall spacers. The hole is backfilled with the material of the first layer (e.g. a-silicon), and the structure is planarized at 937. In the embodiment illustrated in FIGS. 6B and 6C, the planarization removes the oxide on the top surface of the amorphous silicon, leaving a "racetrack" or rectangular pattern of

oxide sidewall spacers. At 938, a fin pattern is formed from the sidewall spacers, such as may be realized using a mask and etch process, for example. In some embodiments, the resulting fin pattern has a first cross-section thickness in a first direction that corresponds to a minimum feature size, and a second cross-section thickness in a second direction orthogonal to the first that corresponds to the thickness of the oxide sidewalls and is significantly less than the minimum feature size. At 939, the layer (e.g. a-silicon) is removed, leaving the fin pattern of sidewall spacers. The crystalline substrate is etched at 940 using a mask corresponding to the fin pattern of sidewall spacers. Various embodiments etch the silicon nitride layer into fin pattern, and then use the silicon nitride layer to mask the crystalline substrate with the fin pattern when the substrate is etched. At 941, the mask layer (e.g. silicon nitride) is removed to expose the top of the etched fins.

FIG. 10 is a simplified block diagram of a high-level organization of various embodiments of a memory device according to various embodiments of the present subject matter. The illustrated memory device 1042 includes a memory array 1043 and read/write control circuitry 1044 to perform operations on the memory array via communication line(s) or channel(s) 1045. The illustrated memory device 1042 may be a memory card or a memory module such as a single inline memory module (SIMM) and dual inline memory module (DIMM). One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, that semiconductor components in the memory array and / or the control circuitry are able to be fabricated using etched nanofin transistors, as described above. The structure and fabrication methods for these devices have been described above.

The memory array 1043 includes a number of memory cells 1046. The memory cells in the array are arranged in rows and columns. In various embodiments, word lines 1047 connect the memory cells in the rows, and bit lines 1048 connect the memory cells in the columns. The read/write control circuitry 1044 includes word line select circuitry 1049 which functions to select a

desired row, bit line select circuitry 1050 which functions to select a desired column, and read circuitry 1051, which functions to detect a memory state for a selected memory cell in the memory array 1043.

FIG. 11 illustrates a diagram for an electronic system 1152 having one or more nanofin transistors, according to various embodiments. Electronic system 1152 includes a controller 1153, a bus 1154, and an electronic device 1155, where the bus 1154 provides communication channels between the controller 1153 and the electronic device 1155. In various embodiments, the controller and/or electronic device include nanofin transistors as previously discussed herein. The illustrated electronic system 1152 may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

FIG. 12 depicts a diagram of an embodiment of a system 1256 having a controller 1257 and a memory 1258. The controller and/or memory may include nanofin transistors according to various embodiments. The illustrated system 1256 also includes an electronic apparatus 1259 and a bus 1260 to provide communication channel(s) between the controller and the electronic apparatus, and between the controller and the memory. The bus may include an address, a data bus, and a control bus, each independently configured; or may use common communication channels to provide address, data, and/or control, the use of which is regulated by the controller. In an embodiment, the electronic apparatus 1259 may be additional memory configured similar to memory 1258. An embodiment may include a peripheral device or devices 1261 coupled to the bus 1260. Peripheral devices may include displays, additional storage memory, or other control devices that may operate in conjunction with the controller and/or the memory. In an embodiment, the controller is a processor. Any of the controller 1257, the memory 1258, the electronic apparatus 1259, and the peripheral devices 1261 may include nanofin transistors according to various embodiments. The system 1256 may include, but is not limited to, information handling devices, telecommunication systems, and computers. Applications

containing nanofin transistors as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

The memory may be realized as a memory device containing nanofin transistors according to various embodiments. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM). Various emerging memory technologies are capable of using transistors with the compressively-strained channels.

This disclosure includes several processes, circuit diagrams, and cell structures. The present subject matter is not limited to a particular process order or logical arrangement. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover adaptations or variations of the present subject matter. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing and understanding the above description. The scope of the present subject matter should be determined

with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method for forming a transistor, comprising:

forming a fin from a crystalline substrate, wherein forming the fin includes:

depositing a material on the crystalline substrate;

forming a mask pattern and using the mask pattern with a minimum feature length to etch the material to define at least two holes in the material, wherein the material provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F);

forming sidewall spacers on each of the sidewalls that surround and define the at least two holes;

forming a fin pattern from the sidewall spacers, wherein forming the fin pattern includes forming an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus the thickness of the fin (ΔT); and

using the fin pattern as a mask to etch the fin from the crystalline substrate,

wherein the fin has a cross-sectional thickness in a first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length,

wherein the first direction is substantially parallel to a surface of the substrate and the second direction is substantially parallel to the surface of the substrate;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate insulator around the fin;

forming a surrounding gate around the fin and separated from the fin by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the fin.

2. The method of claim 1, wherein forming the fin from the crystalline substrate includes forming the fin from a crystalline silicon substrate.

3. The method of claim 1, wherein forming the first source/drain region in the substrate

beneath the fin includes implanting a dopant in a trench adjacent to the substrate and diffusing the dopant underneath the fin.

4. The method of claim 3, wherein diffusing includes diffusing the dopant into a bottom portion of the fin.

5. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

6. The method of claim 1, wherein forming the surrounding gate includes forming a polysilicon gate.

7. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

8. The method of claim 1, further comprising forming a gate contact adjacent to and in contact with the surrounding gate.

9. The method of claim 1, further comprising forming at least one gate line adjacent to and in contact with the surrounding gate.

10. The method of claim 9, wherein forming the at least one gate line adjacent to and in contact with the surrounding gate includes forming a first gate line adjacent to and in contact with a first side of the surrounding gate and a second gate line adjacent to and in contact with a second side of the surrounding gate, the first and second sides being positioned on opposing sides of the fin.

11. The method of claim 9, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming the at least one gate line adjacent to and in contact with the surrounding gate includes forming a gate line to contact the surrounding gate on the long side.

12. The method of claim 9, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming at least one gate line adjacent to and in contact with the

surrounding gate includes forming a gate line to contact the surrounding gate on the short side.

13. The method of claim 1, wherein forming the surrounding gate includes forming a polysilicon surrounding gate.

14. A method for forming a transistor, comprising:

etching a fin from a crystalline silicon substrate, wherein etching the fin from the crystalline substrate includes:

depositing a material on the crystalline substrate;

forming a mask pattern and using the mask pattern with a minimum feature length to etch the material to define at least two holes in the material, wherein the material provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F); and

forming sidewall spacers on each of the sidewalls that surround and define the at least two holes;

forming a fin pattern from the sidewall spacers, wherein forming the fin pattern includes forming an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus the thickness of the fin (ΔT);

using the fin pattern as a mask to etch the fin,

wherein the fin has a cross-sectional thickness in a first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, and

wherein the first direction is substantially parallel to a surface of the substrate and the second direction is substantially parallel to the surface of the substrate;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate oxide around the fin;

forming a polysilicon surrounding gate around the fin and separated from the fin by the surrounding gate oxide; and

forming a second source/drain region in a top portion of the fin.

15. The method of claim 14, wherein forming the surrounding gate oxide includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

16. The method of claim 14, wherein etching the fin from the crystalline silicon substrate includes:

etching a hole in a layer over the substrate;

forming sidewall spacers in the hole;

forming a fin pattern from the sidewall spacers; and

etching into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern.

17. A method for forming an array of transistors, comprising:

forming a nitride layer on a silicon wafer;

forming an amorphous silicon layer on the nitride layer;

patterning and etching at least two holes in the amorphous silicon layer, wherein patterning includes using a mask pattern with a minimum feature length to pattern the at least two holes and etching includes using the mask pattern to etch the at least two holes, wherein the amorphous silicon layer provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F);

oxidizing the amorphous silicon layer, which results in oxide sidewall spacers on each of the sidewalls of the amorphous silicon layer that surround and define the at least two holes;

backfilling the at least two holes with amorphous silicon;

planarizing to expose oxide sidewalls;

patterning and etching the oxide sidewalls into a fin pattern, wherein the fin pattern provides an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus a thickness of the fin (ΔT);

removing the amorphous silicon;

etching the nitride layer, leaving a fin pattern of nitride beneath the fin pattern of oxide sidewalls;

etching the silicon wafer, using the fin pattern of nitride as a mask, to etch silicon fins from the silicon wafer, wherein each of the silicon fins has a cross-sectional thickness in a

first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, wherein the first direction is substantially parallel to a surface of the silicon wafer and the second direction is substantially parallel to the surface of the silicon wafer;

implanting dopant and diffusing the dopant to form a conduction line beneath the etched silicon fins, the dopant providing first source/drain regions for the silicon fins;

forming a surrounding gate insulator on the silicon fins;

forming surrounding gates, wherein each surrounding gate is formed around and separated from one of the silicon fins by the surrounding gate insulator;

forming gate lines adjacent to and in contact with the surrounding gates for adjacent transistors in the array; and

forming second source/drain regions for the silicon fins.

18. The method of claim 17, wherein forming the surrounding gate insulator includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

19. The method of claim 17, wherein forming the surrounding gates includes forming polysilicon gates.