FIG. 1A

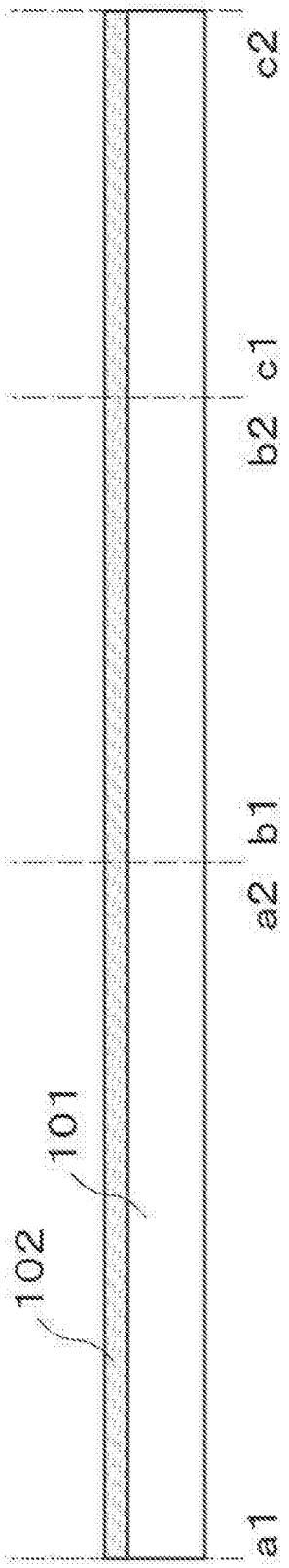


FIG. 1B

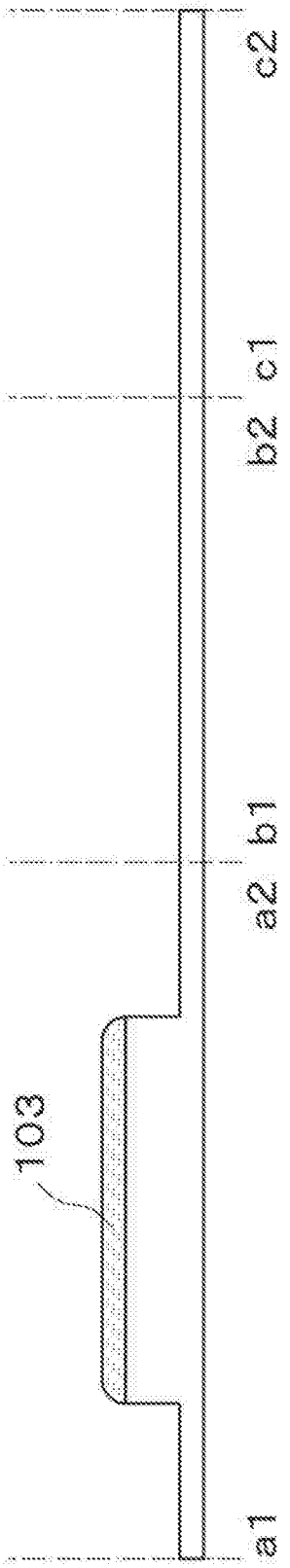


FIG. 1C

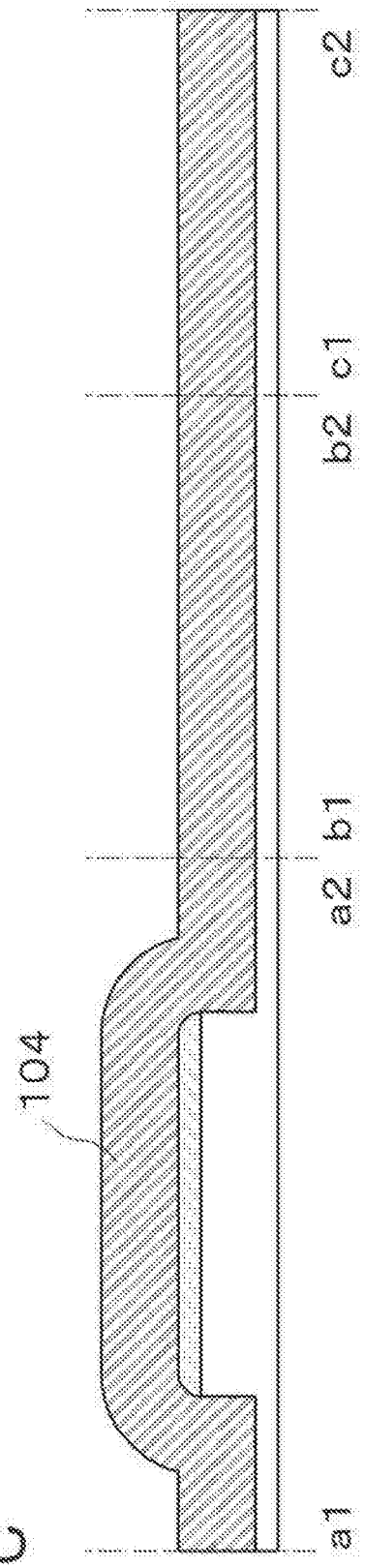


FIG. 2A

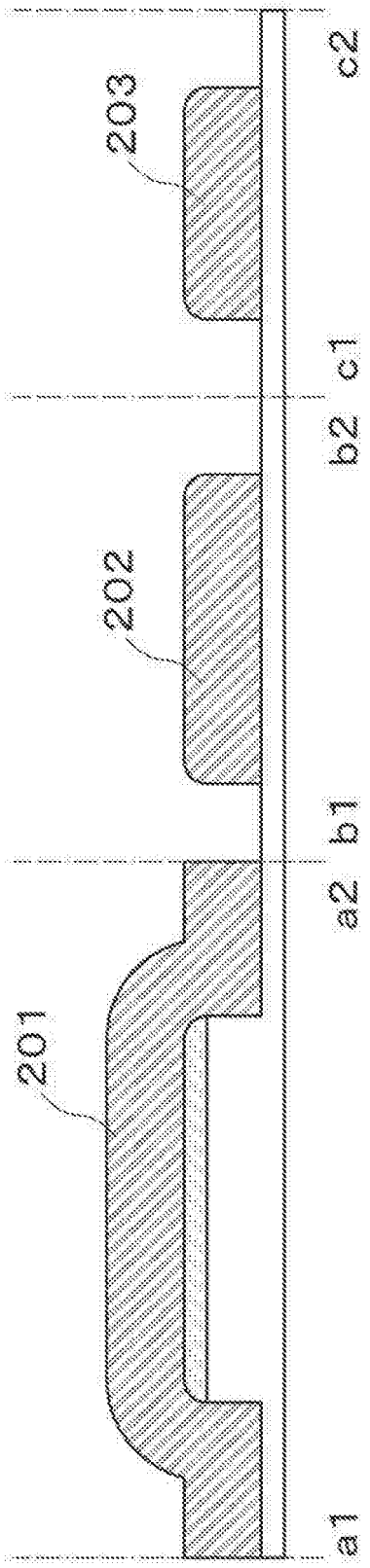
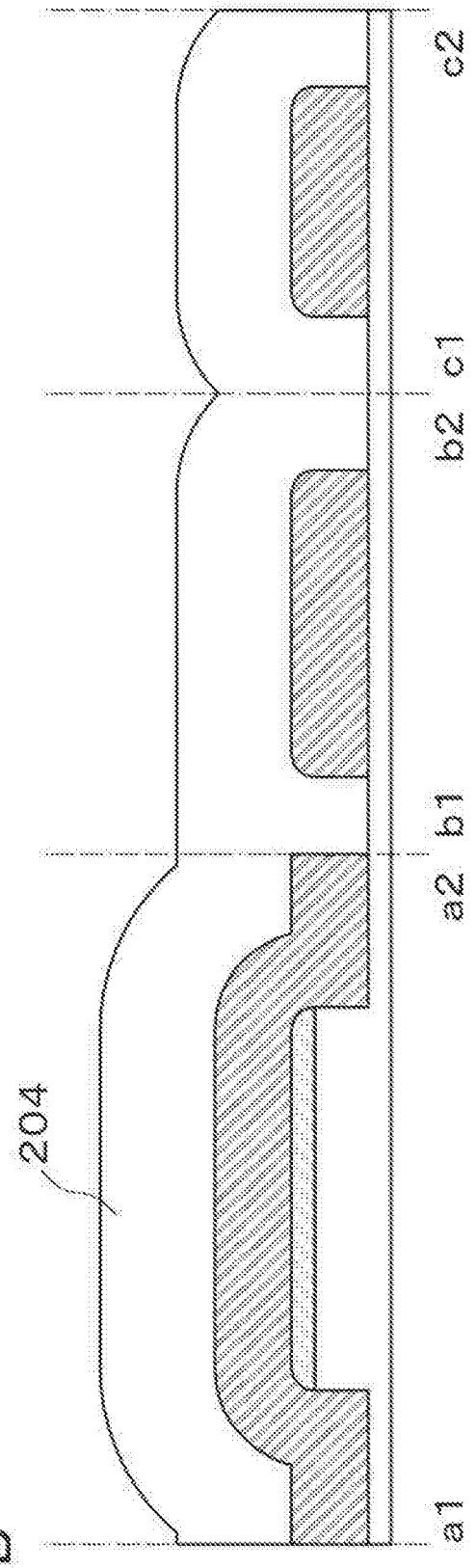


FIG. 2B



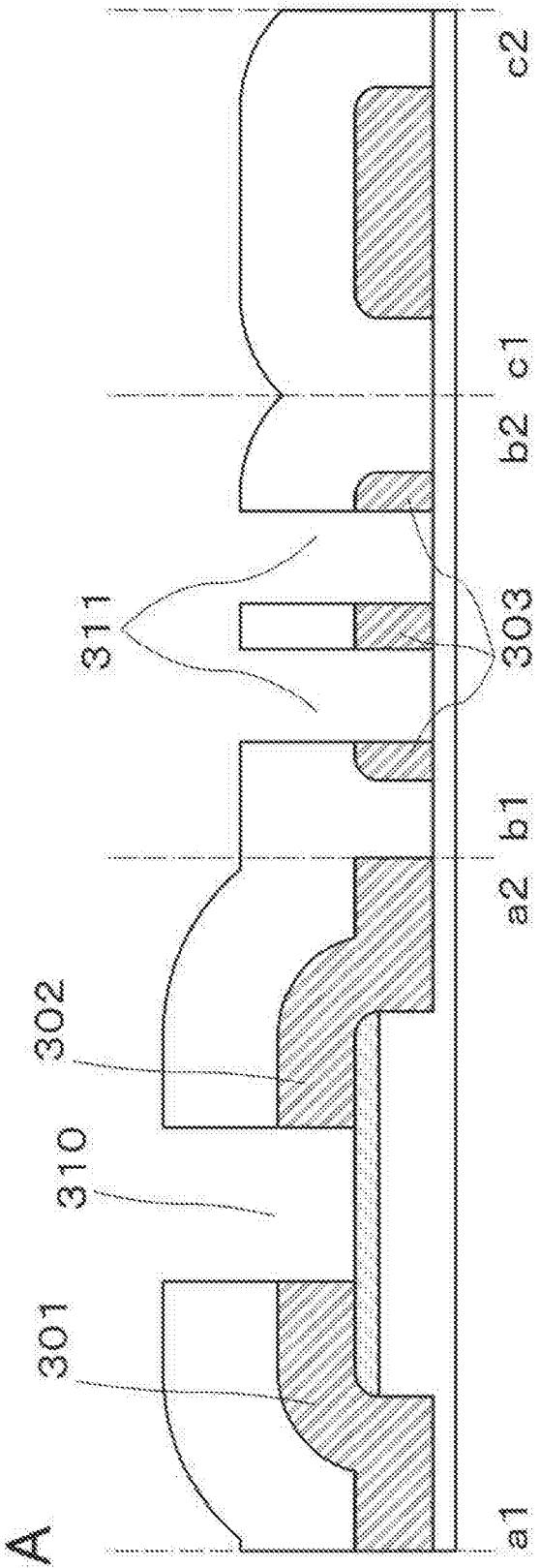


FIG. 3A

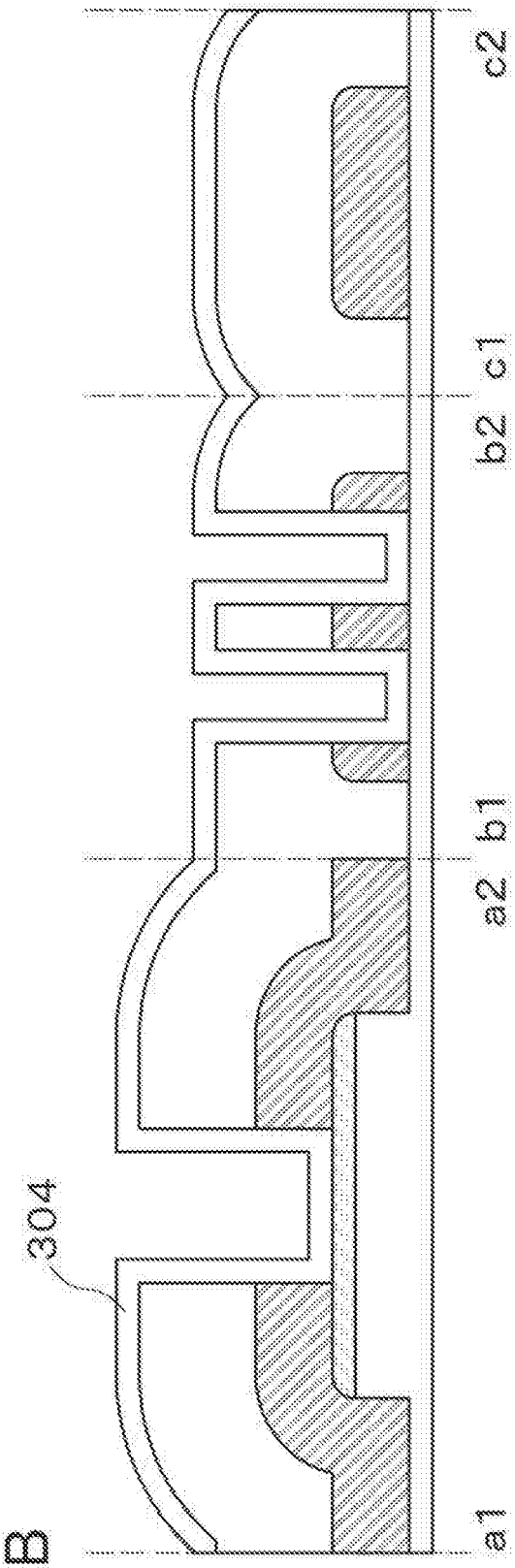


FIG. 3B

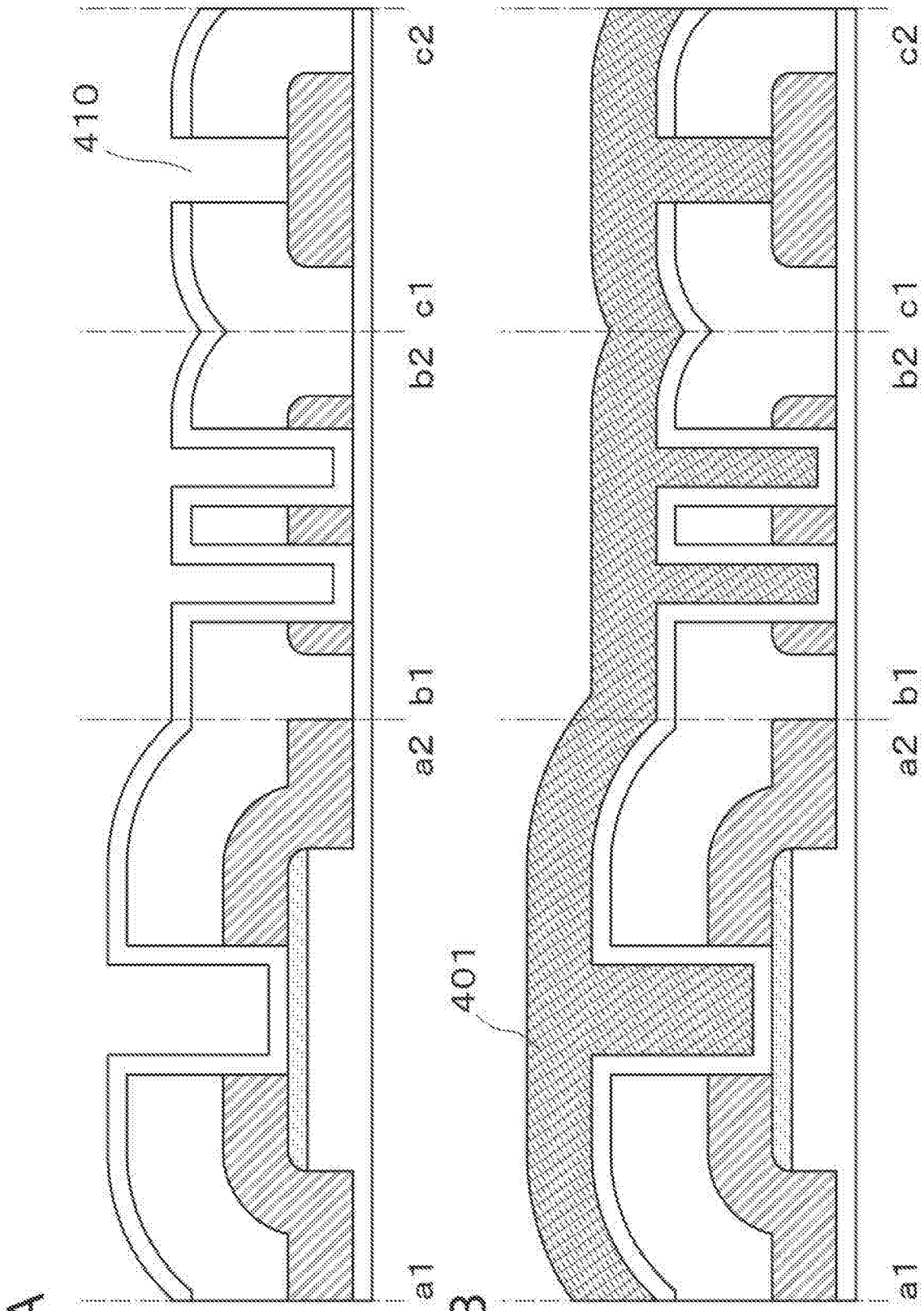


FIG. 4A

FIG. 4B

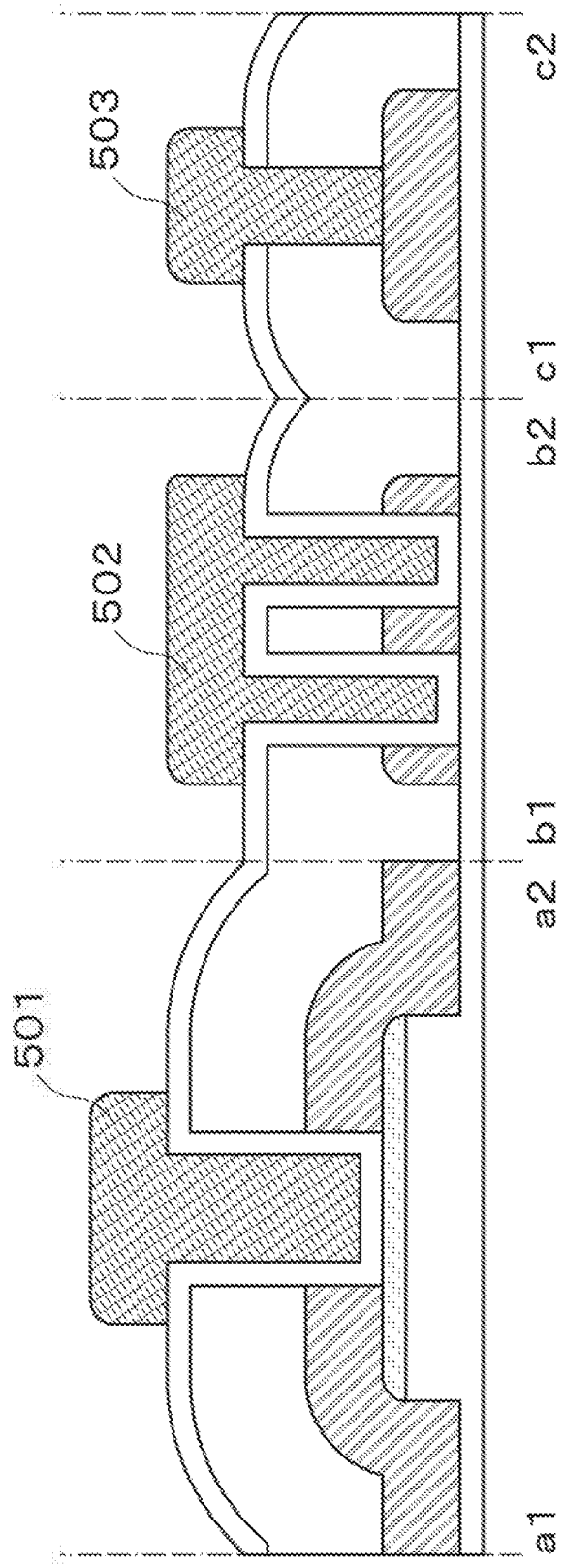


FIG. 5

FIG. 6A

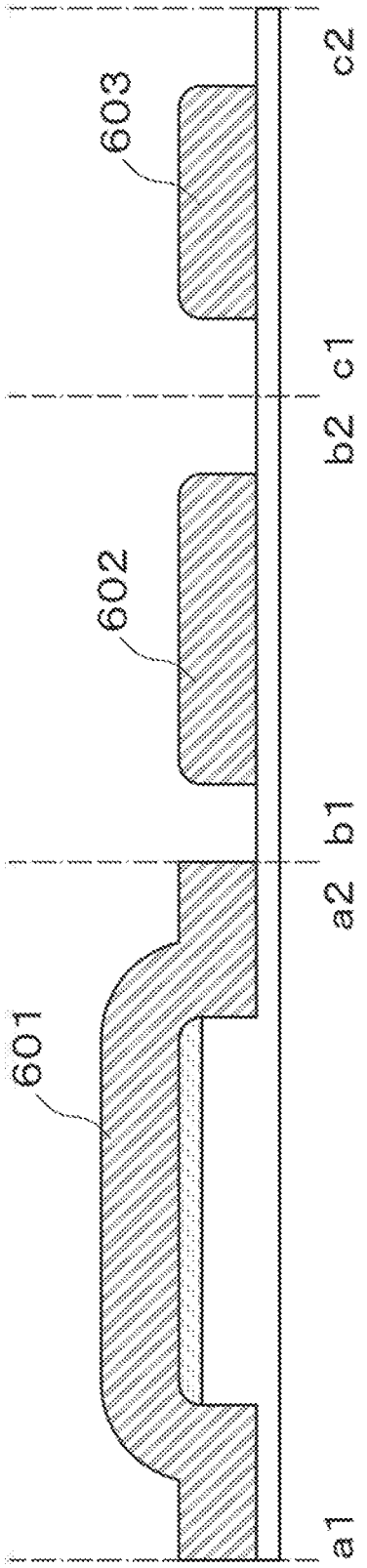
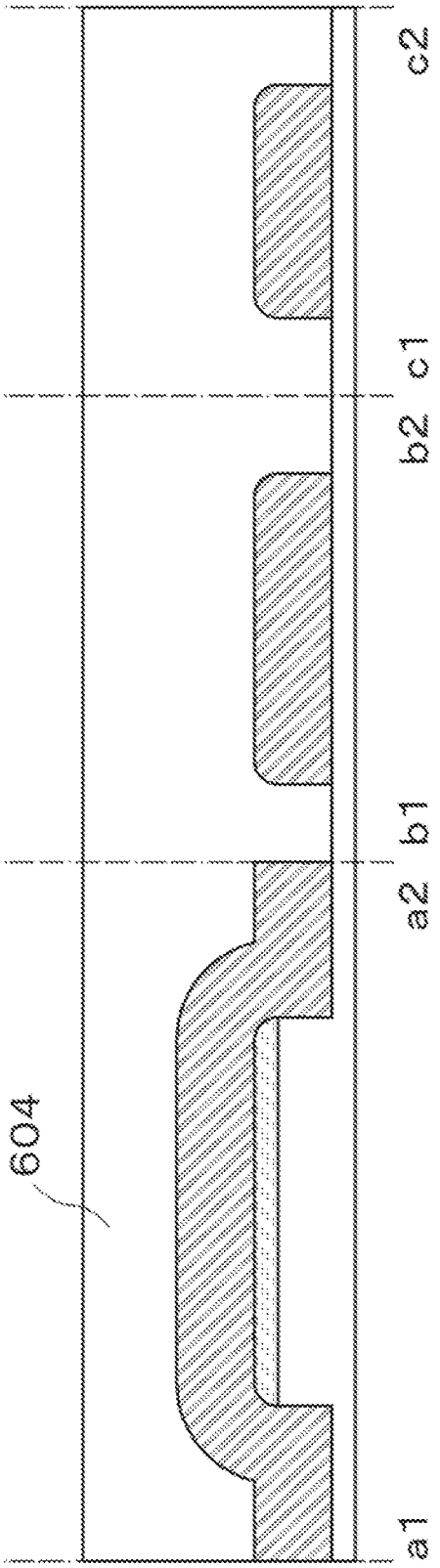


FIG. 6B



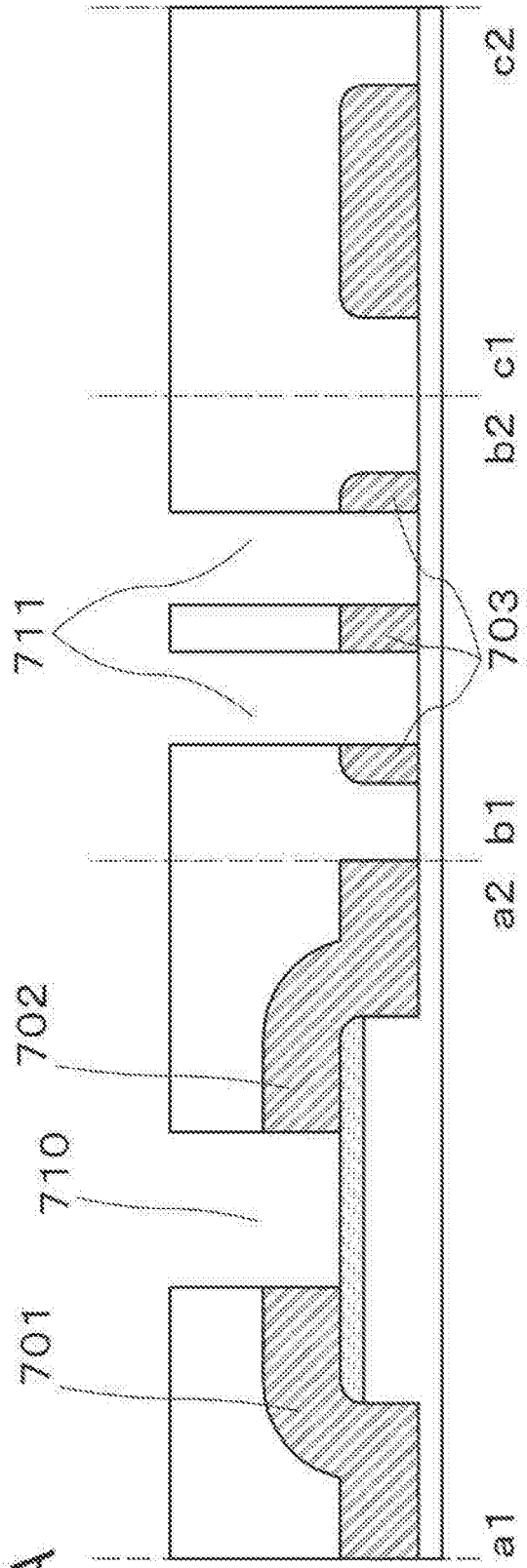


FIG. 7A

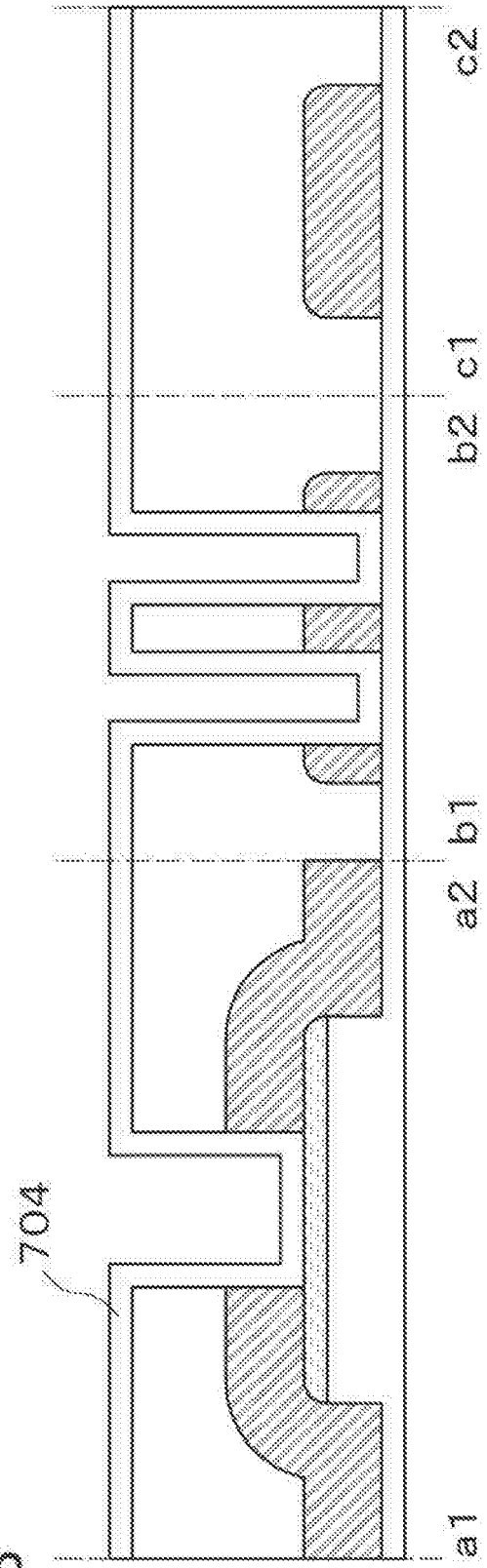


FIG. 7B

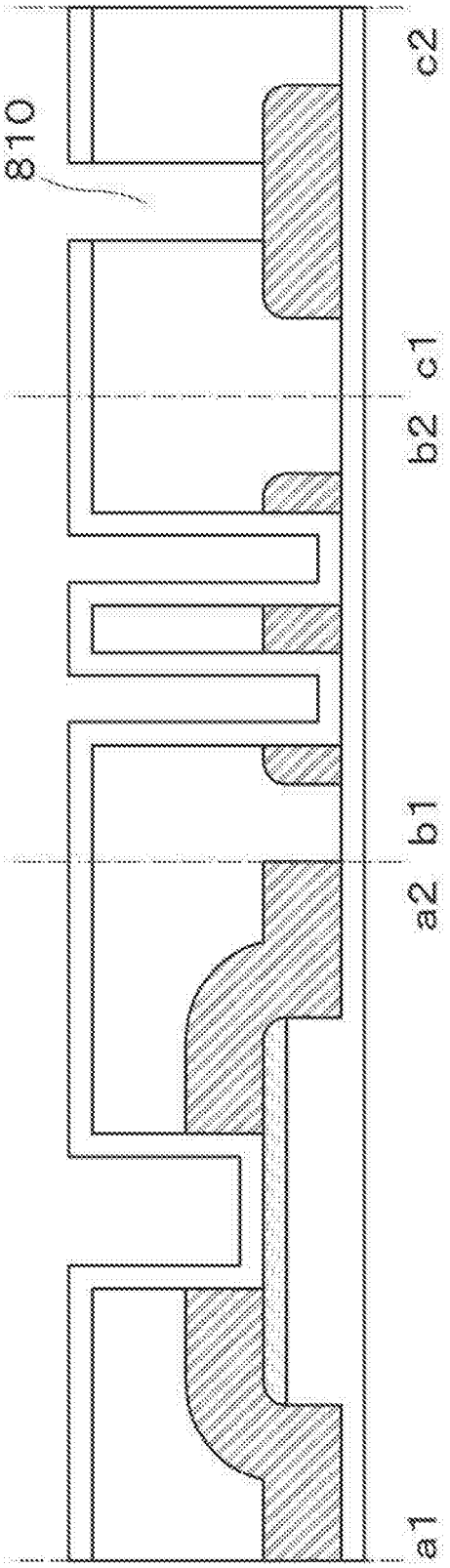


FIG. 8A

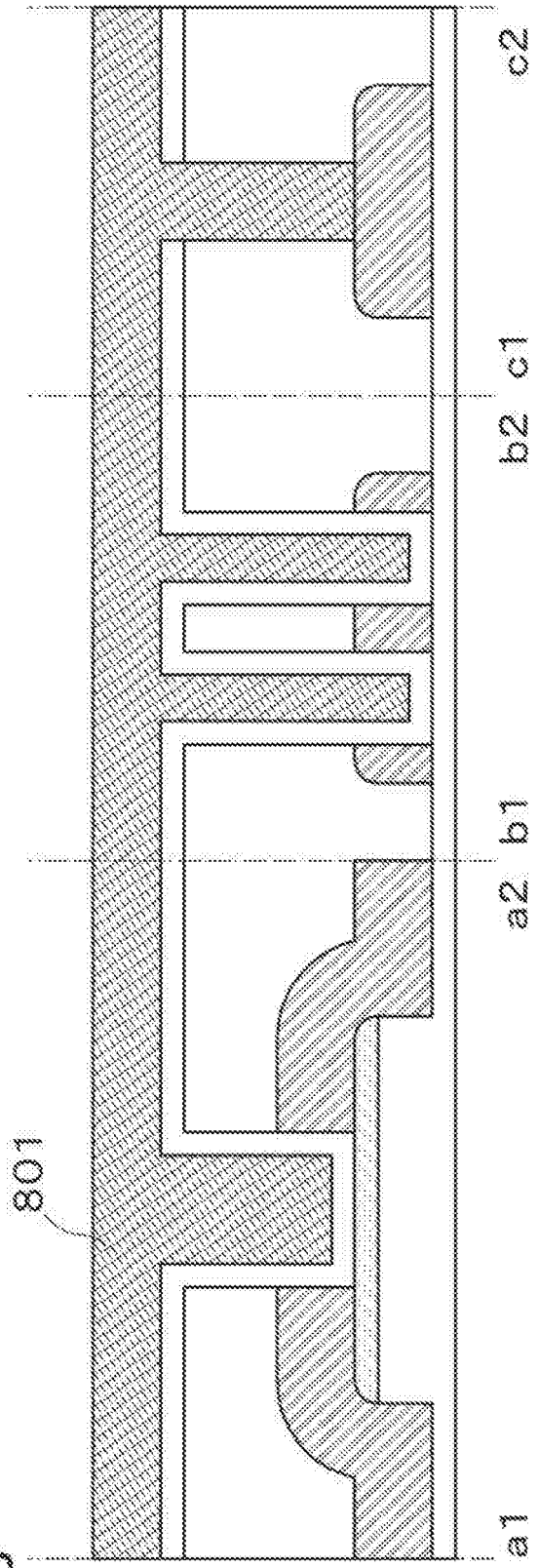


FIG. 8B

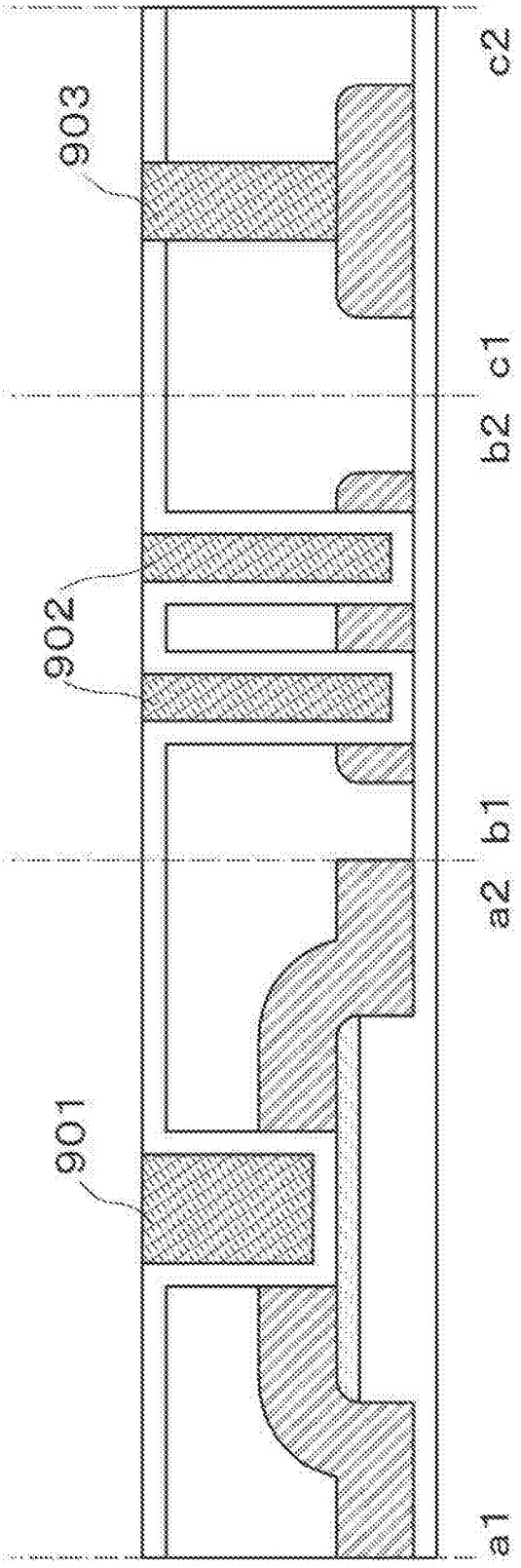


FIG. 9

FIG. 10A

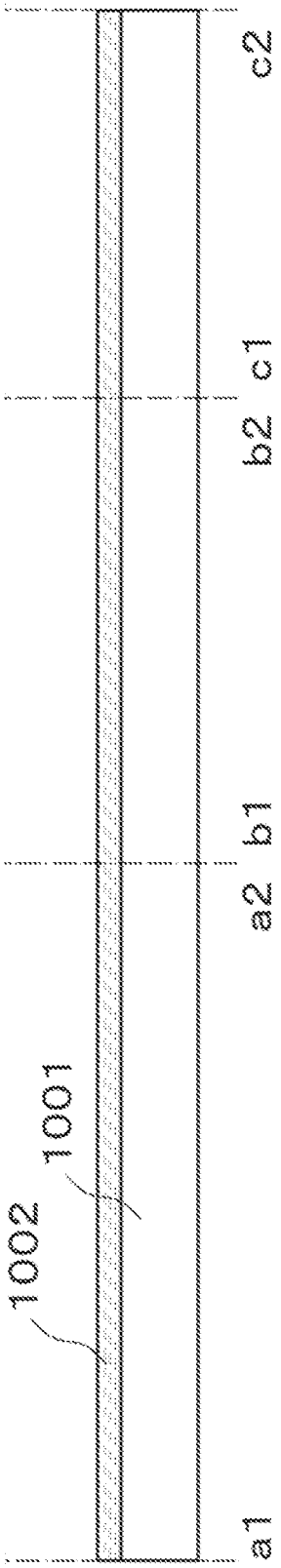


FIG. 10B

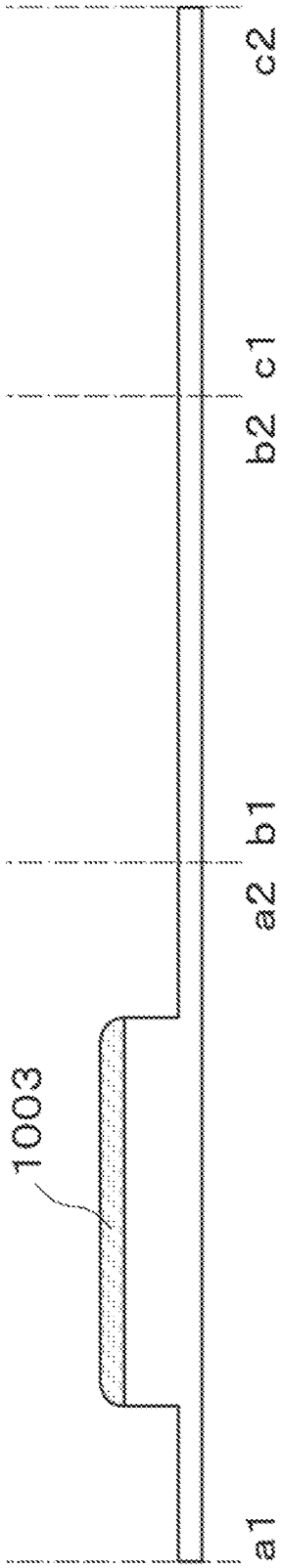
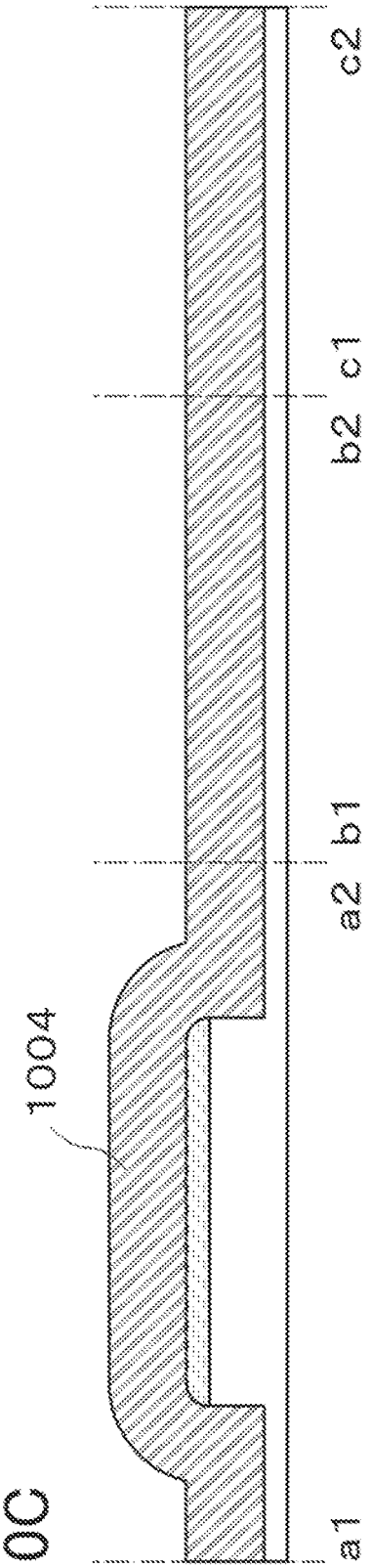


FIG. 10C



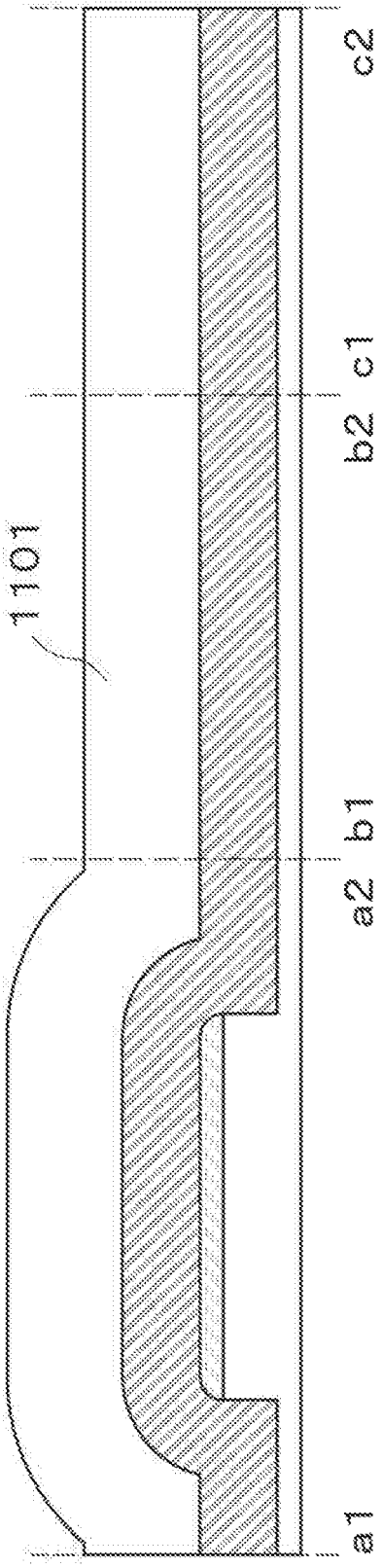


FIG. 11A

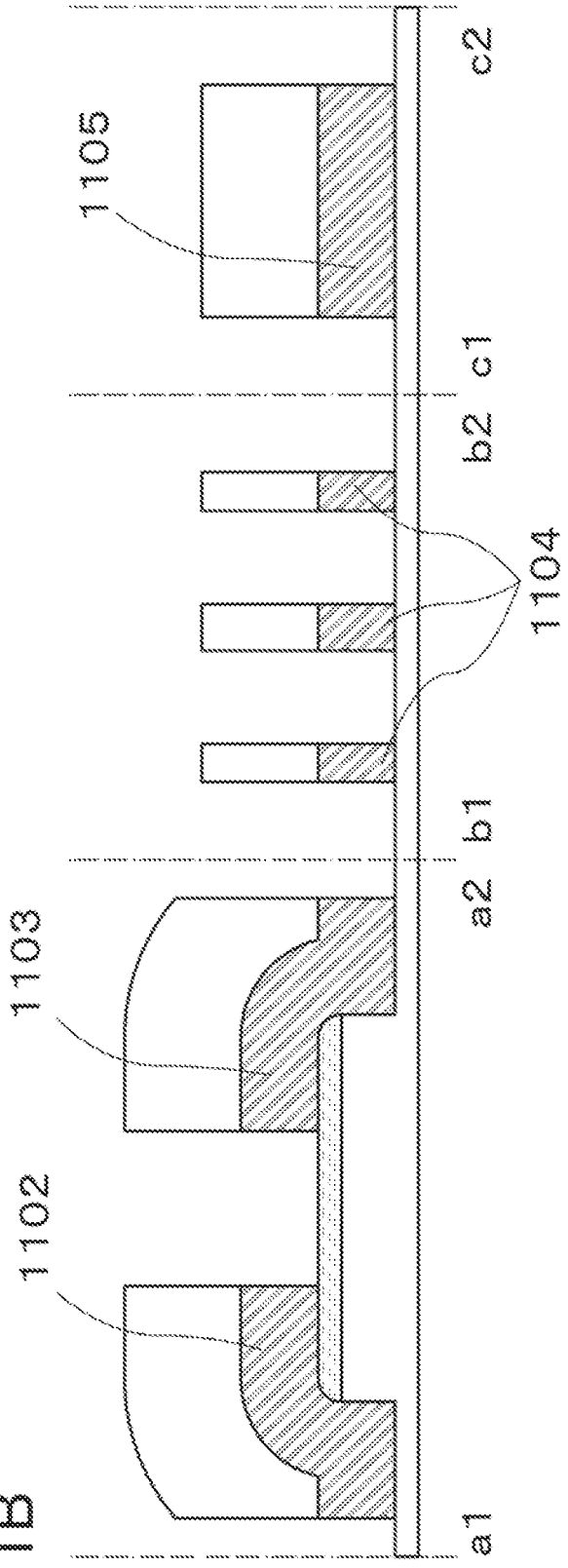


FIG. 11B

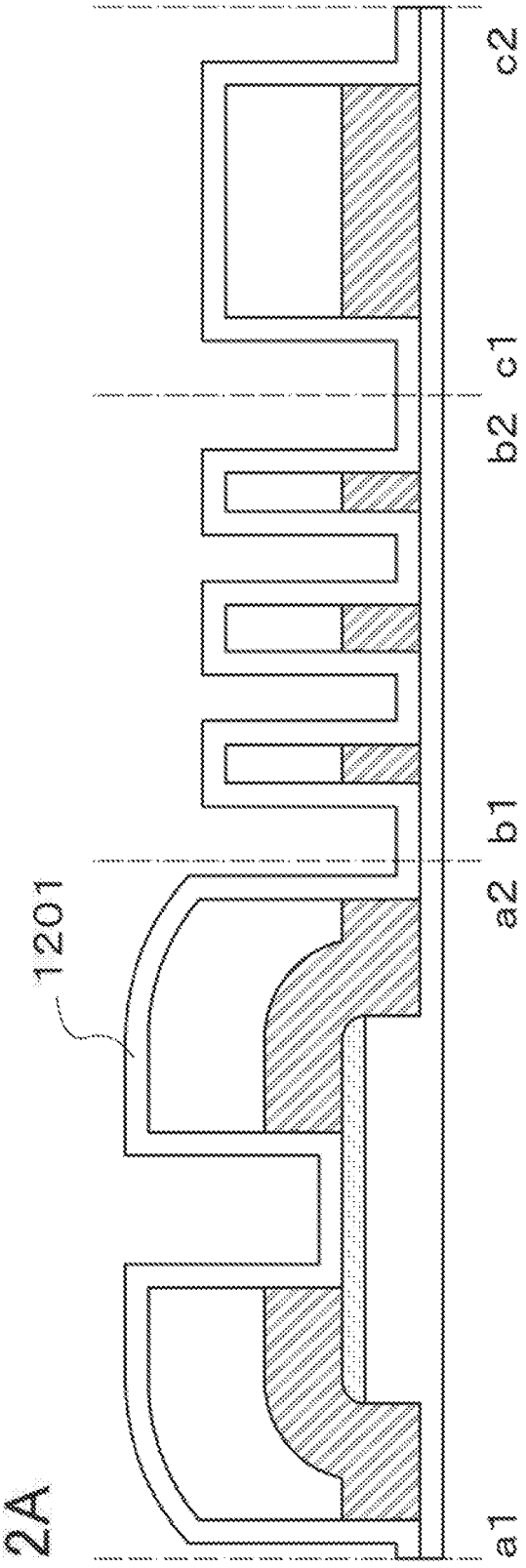


FIG. 12A

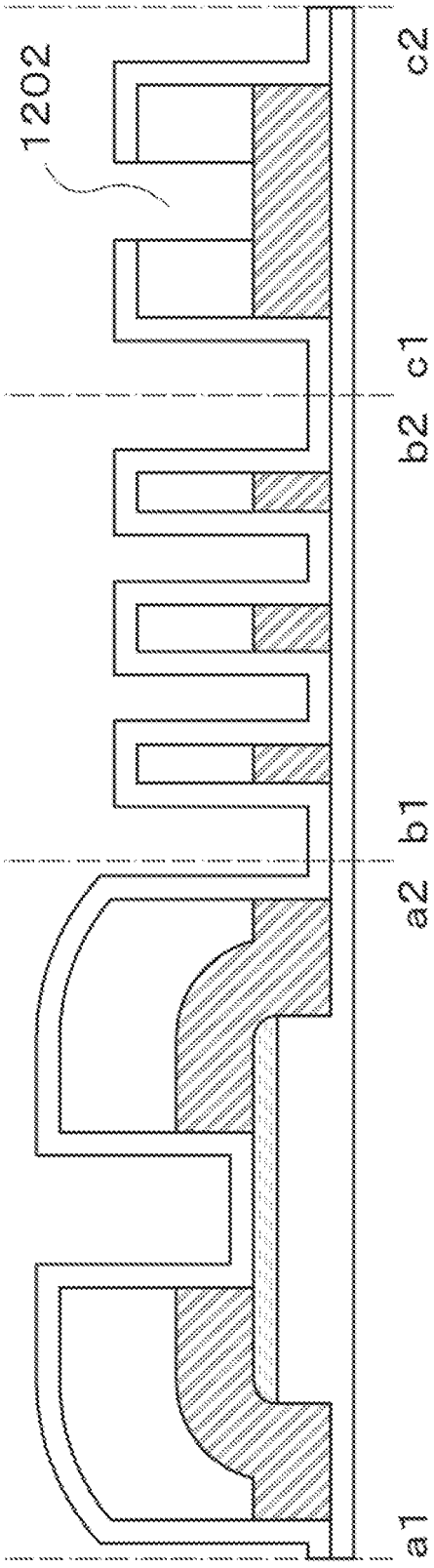


FIG. 12B

FIG. 13A

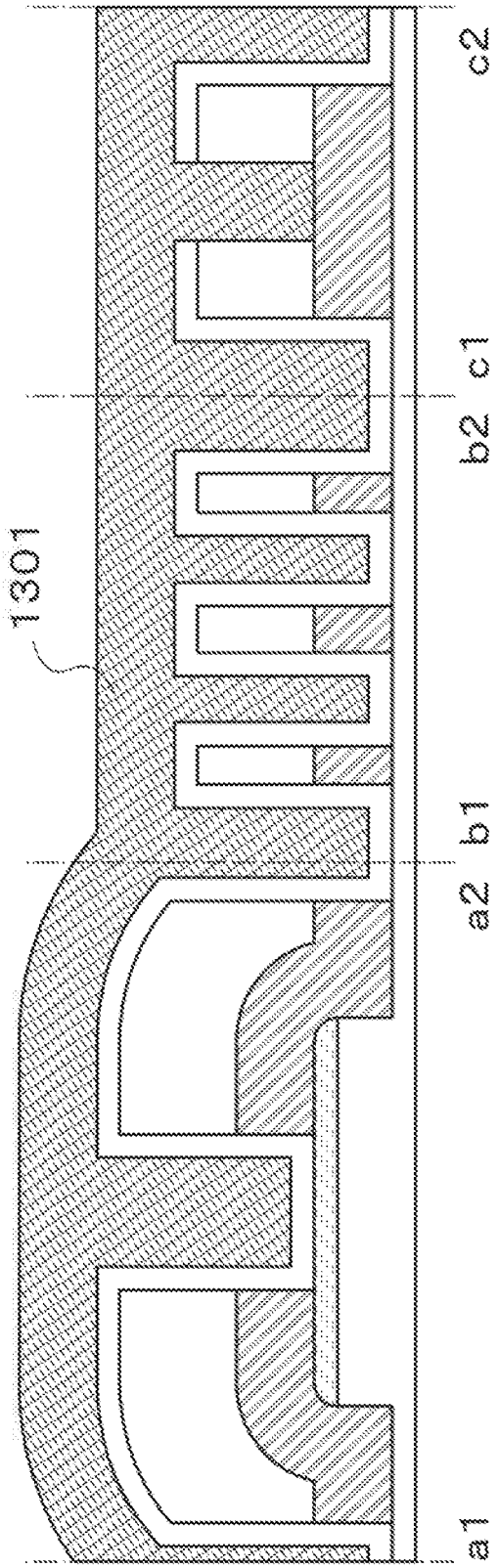


FIG. 13B

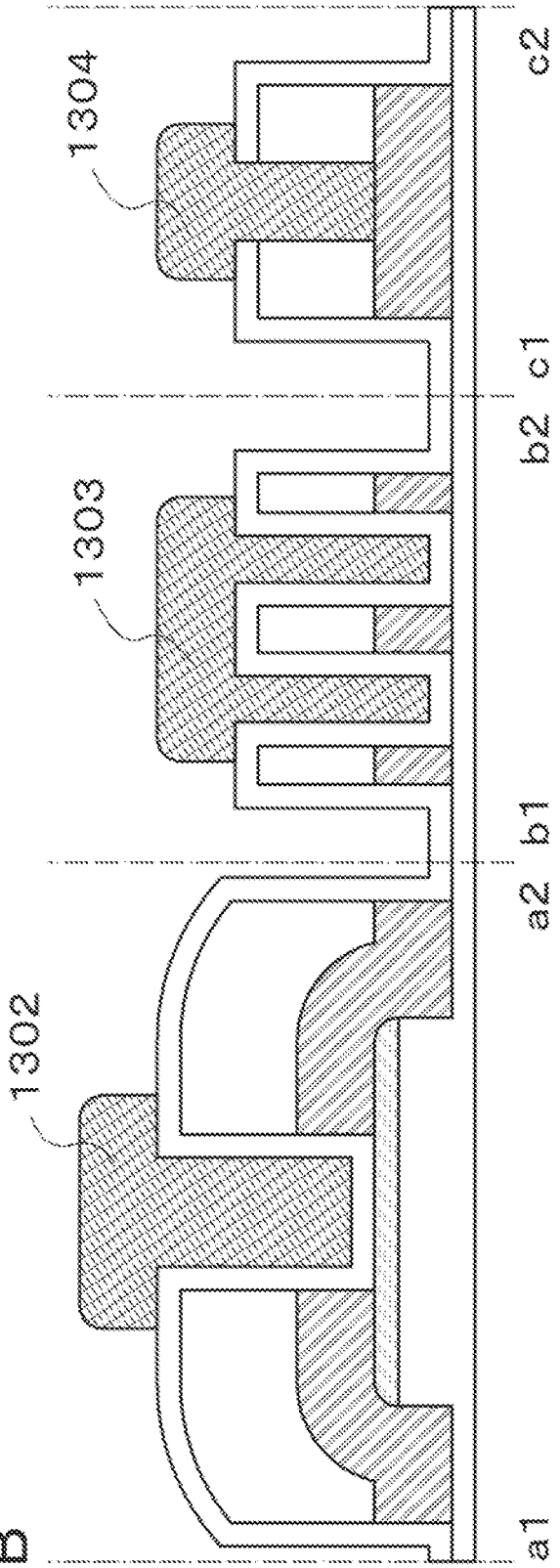


FIG. 14A

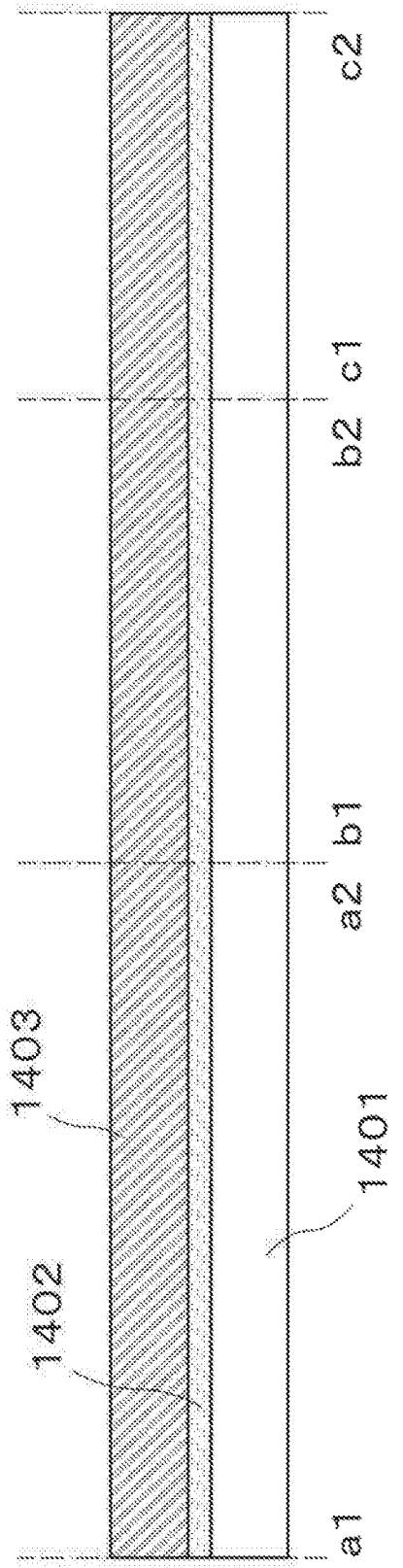
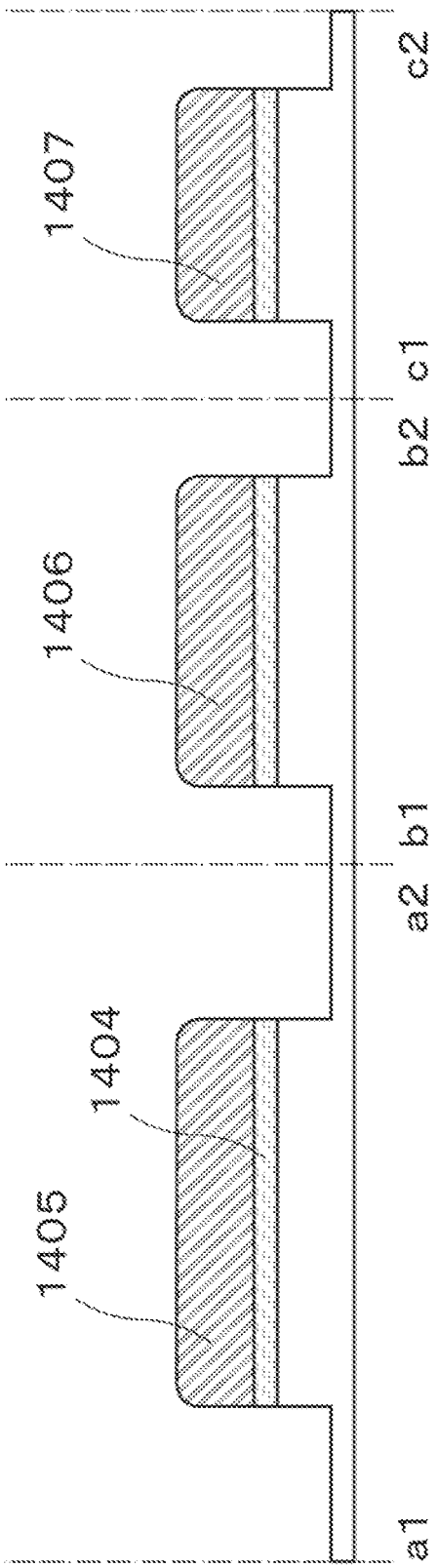


FIG. 14B



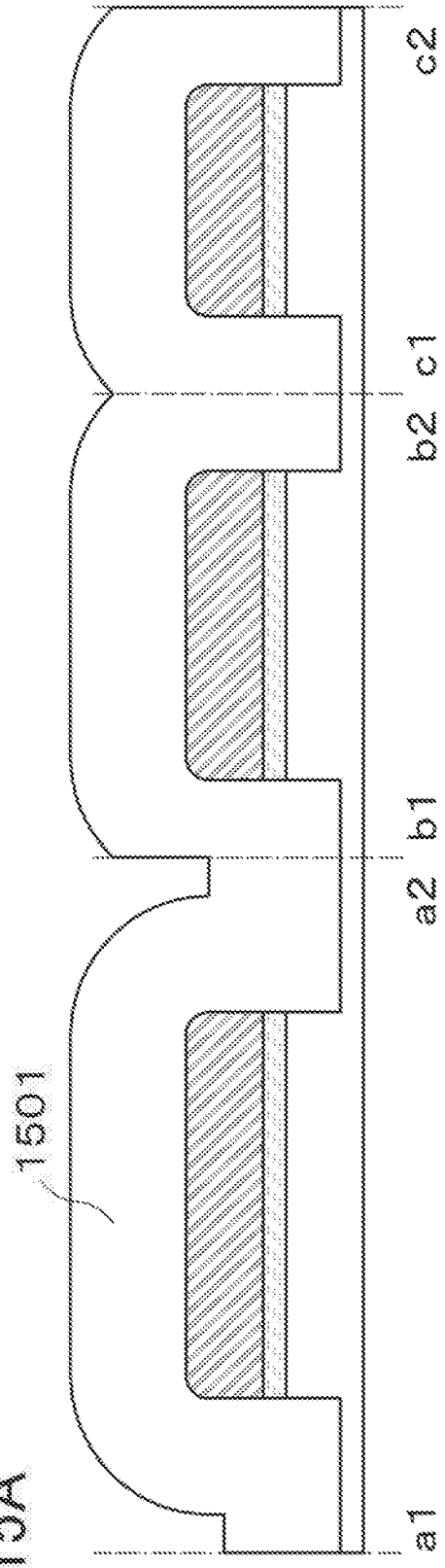


FIG. 15A

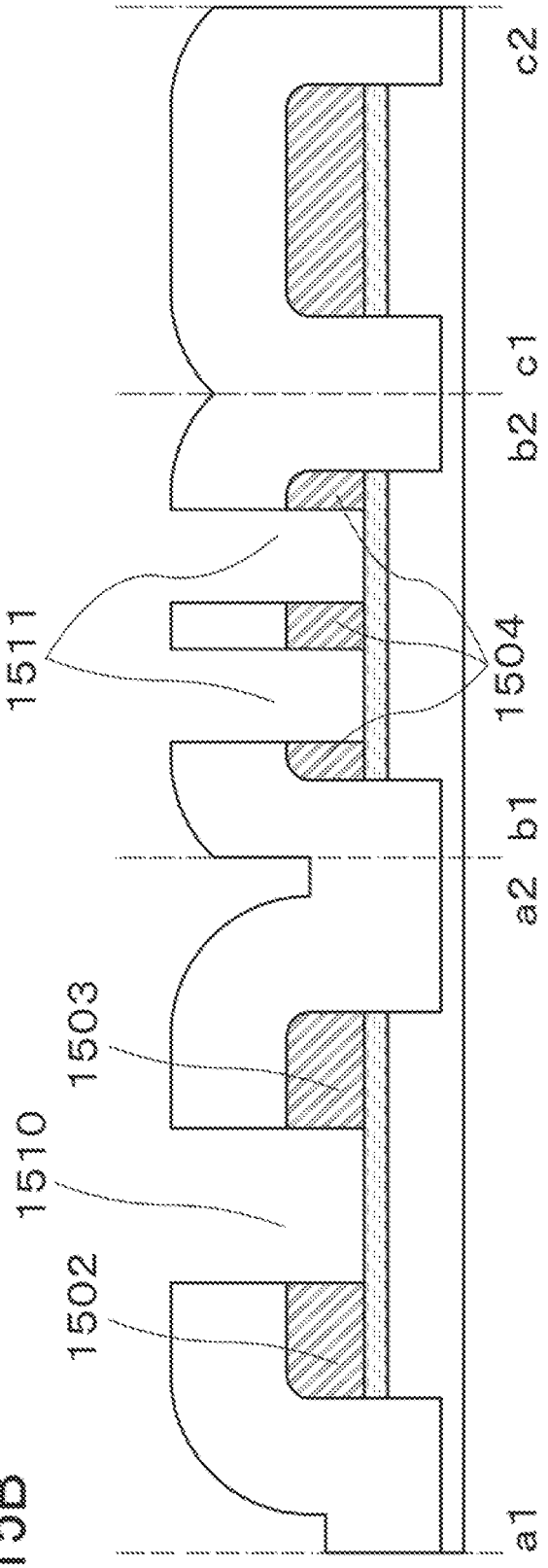


FIG. 15B

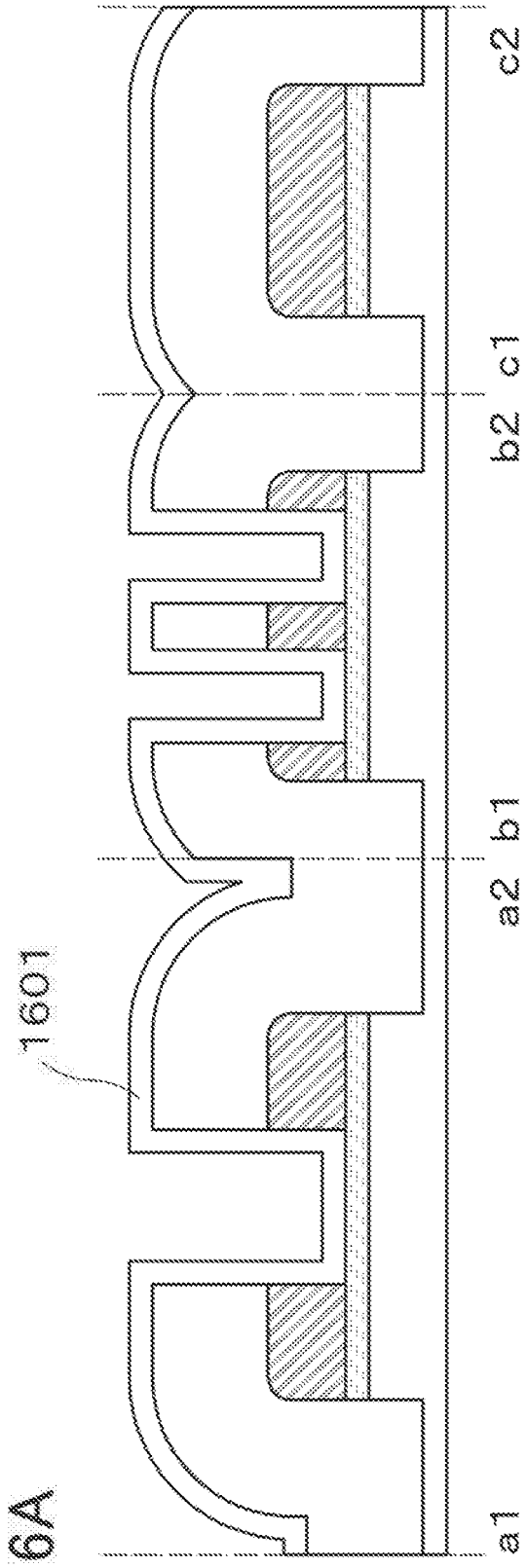


FIG. 16A

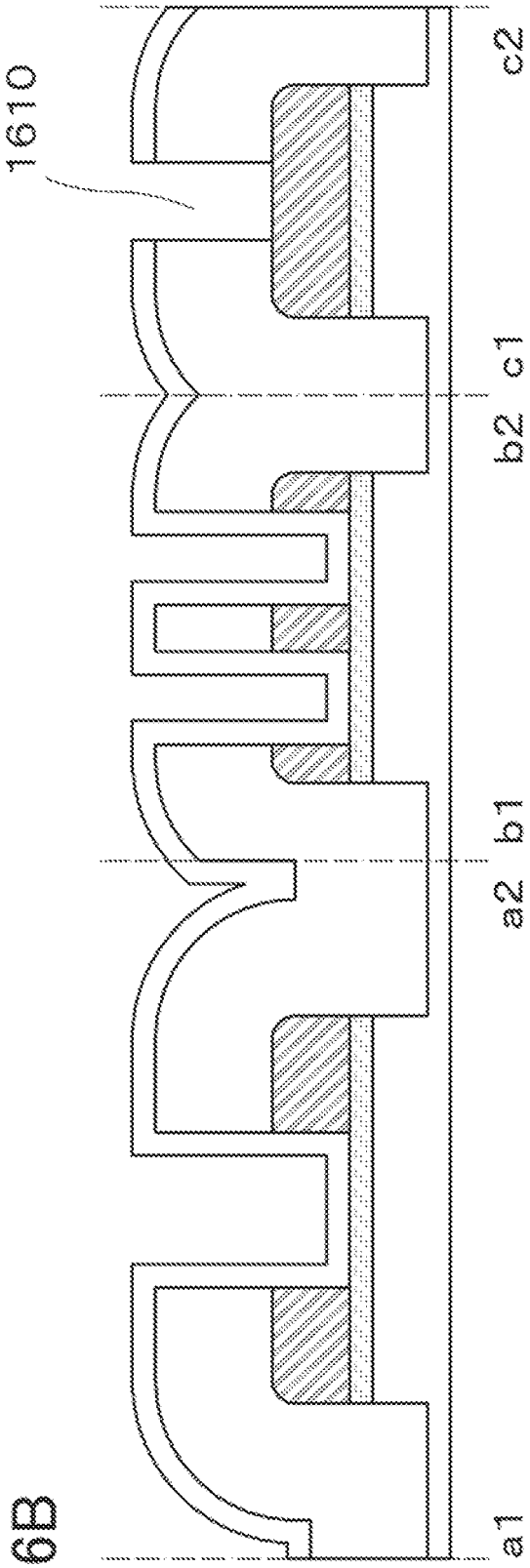


FIG. 16B

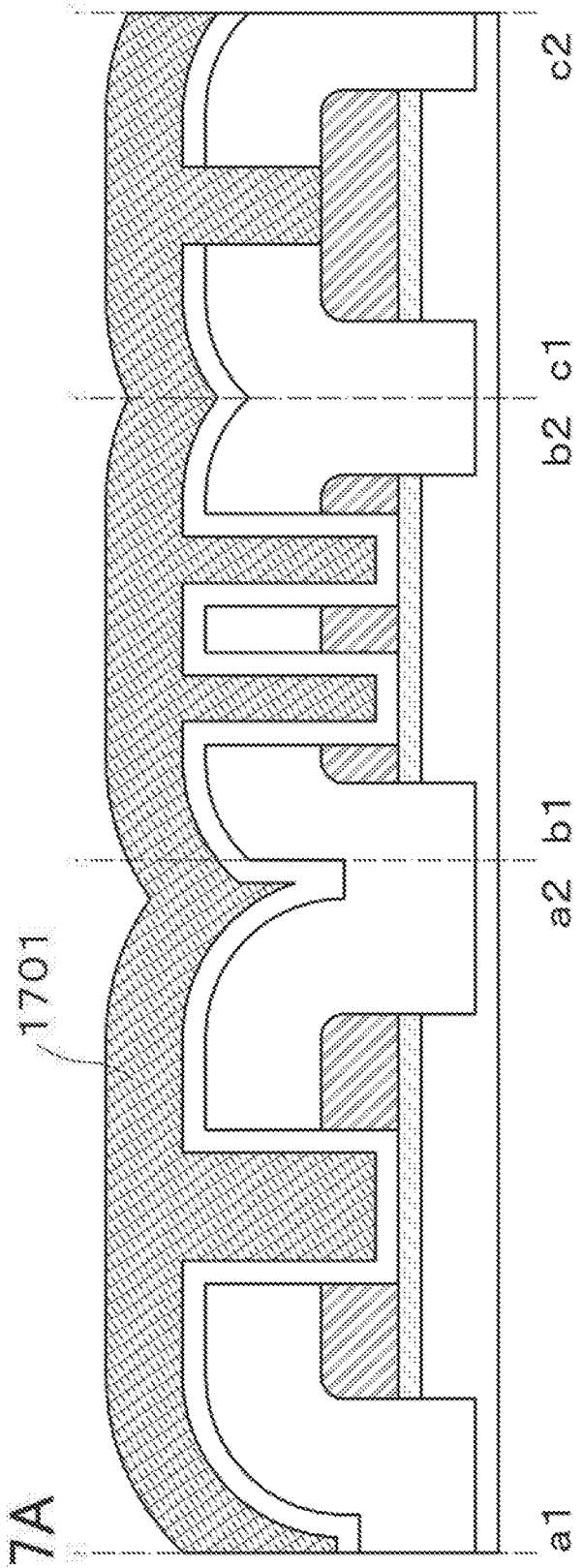


FIG. 17A

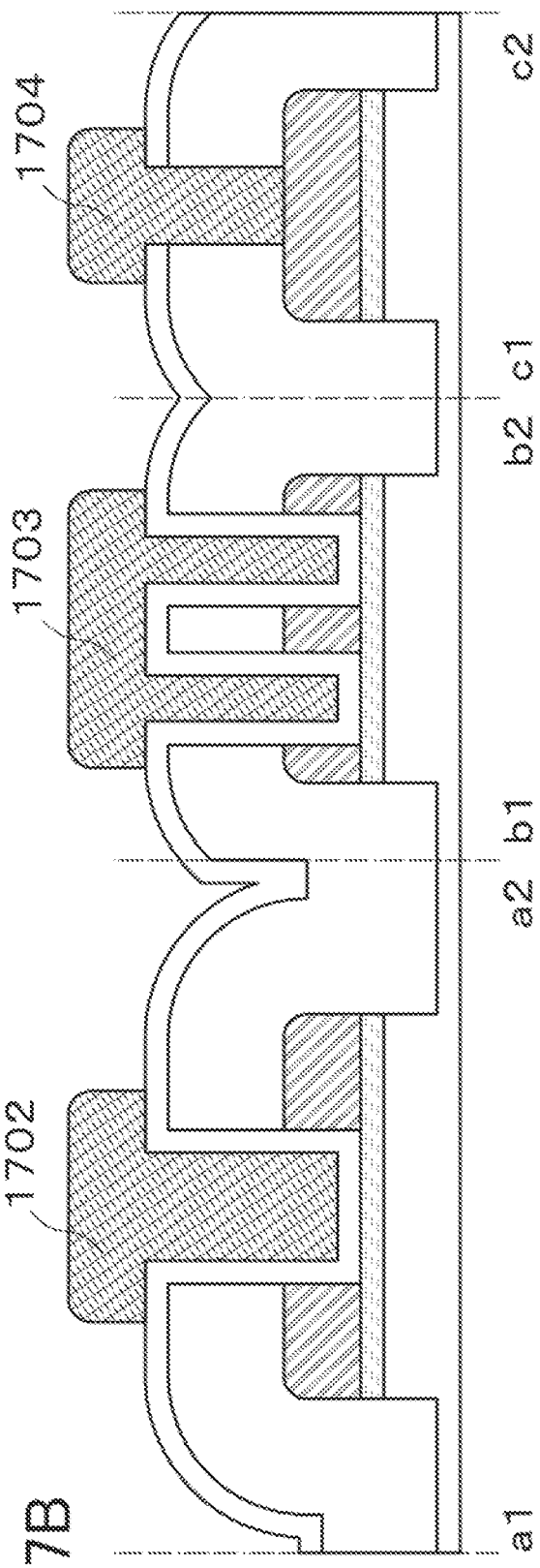


FIG. 17B

FIG. 18A

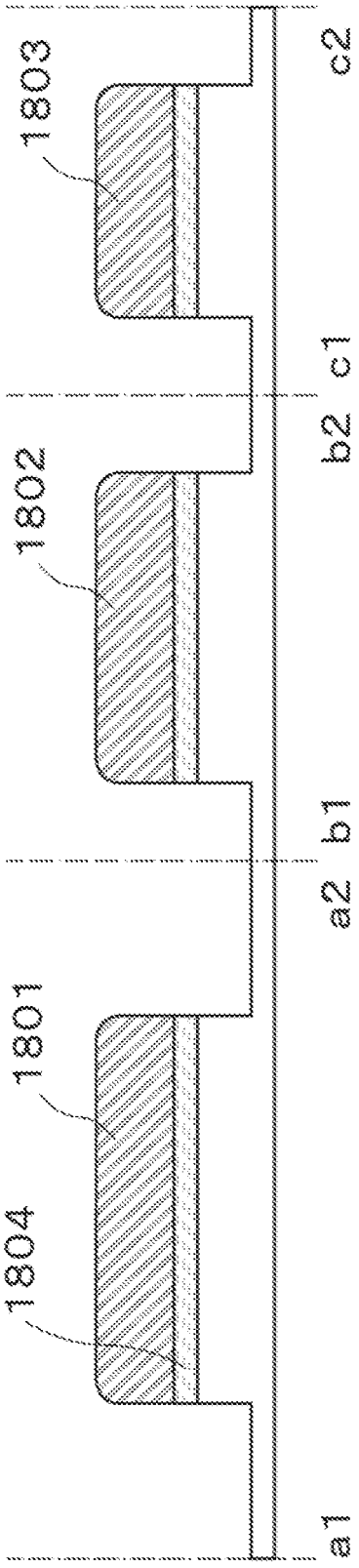
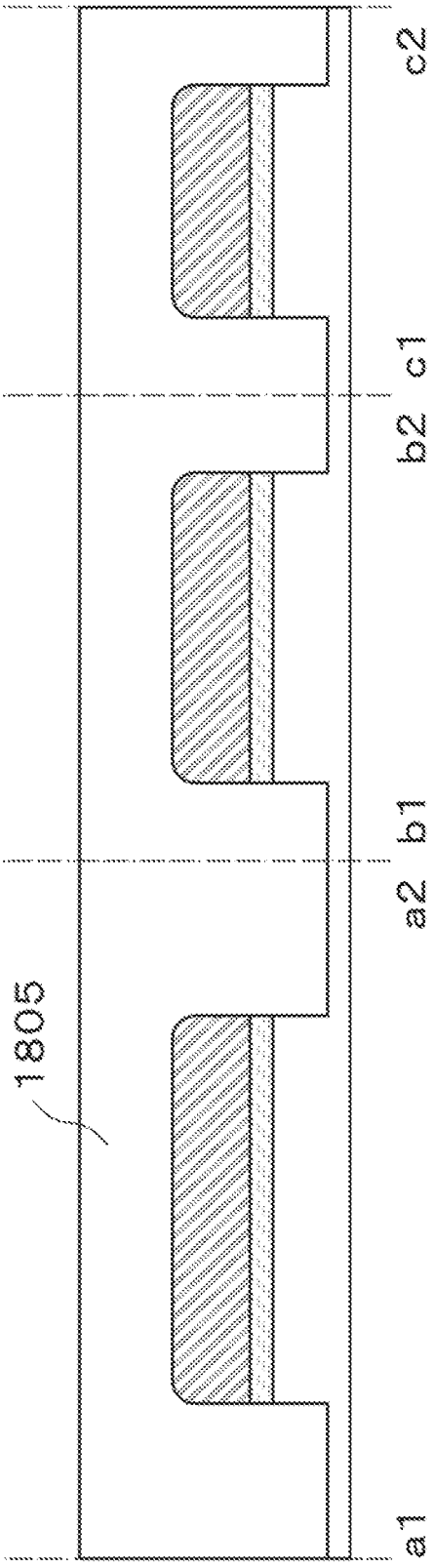


FIG. 18B



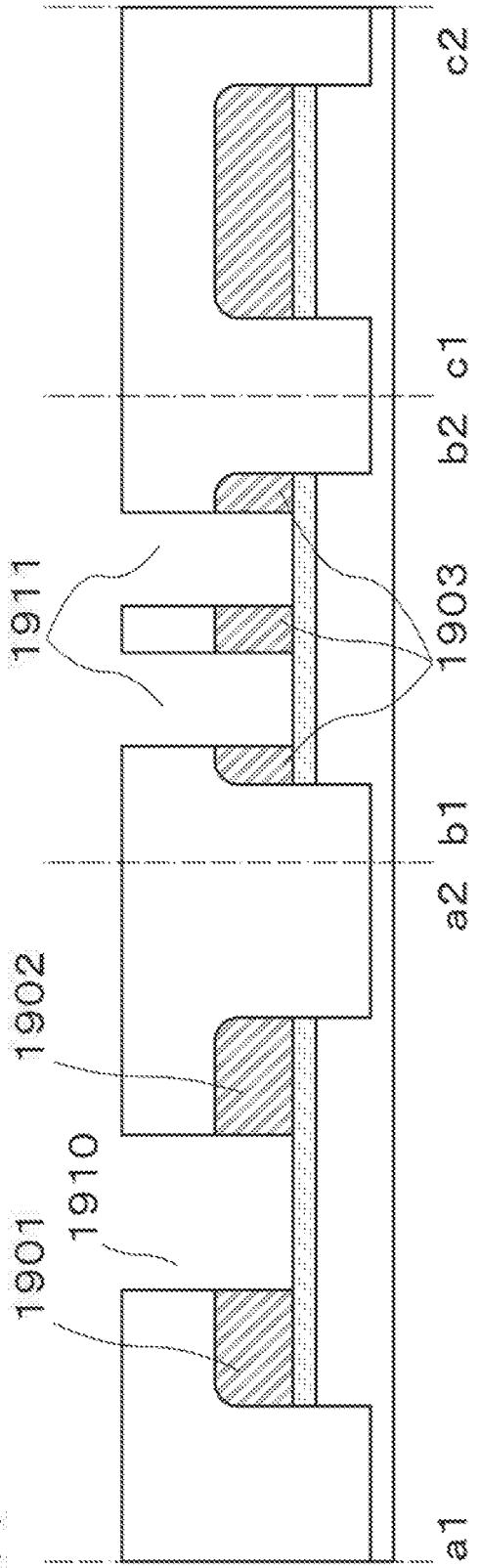


FIG. 19A

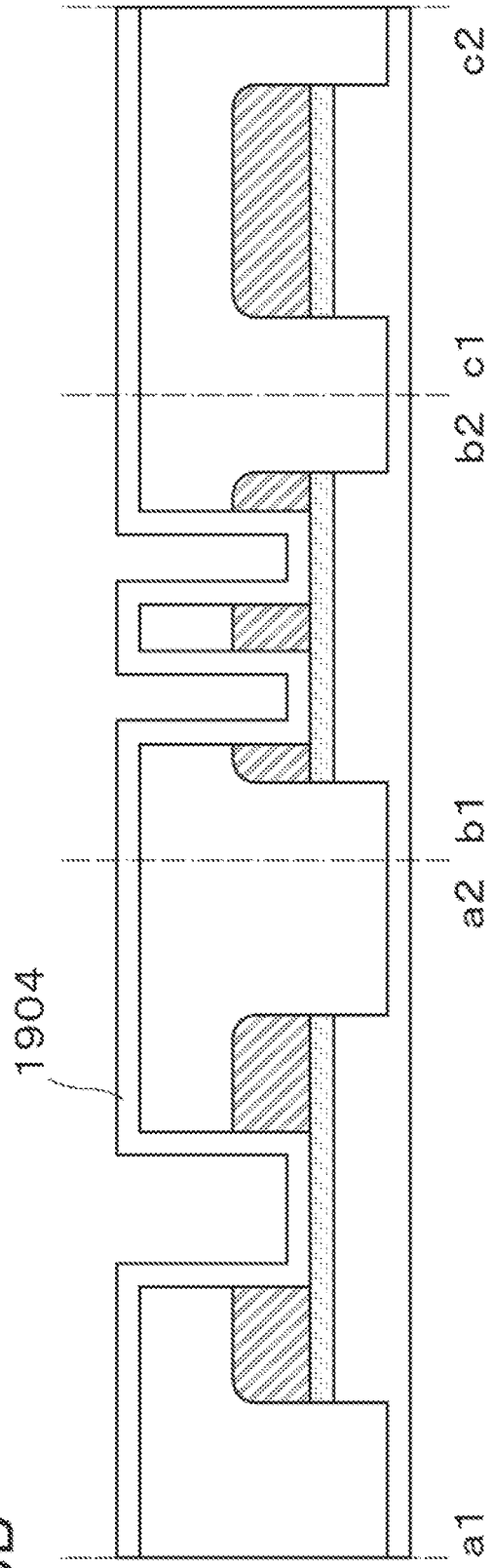


FIG. 19B

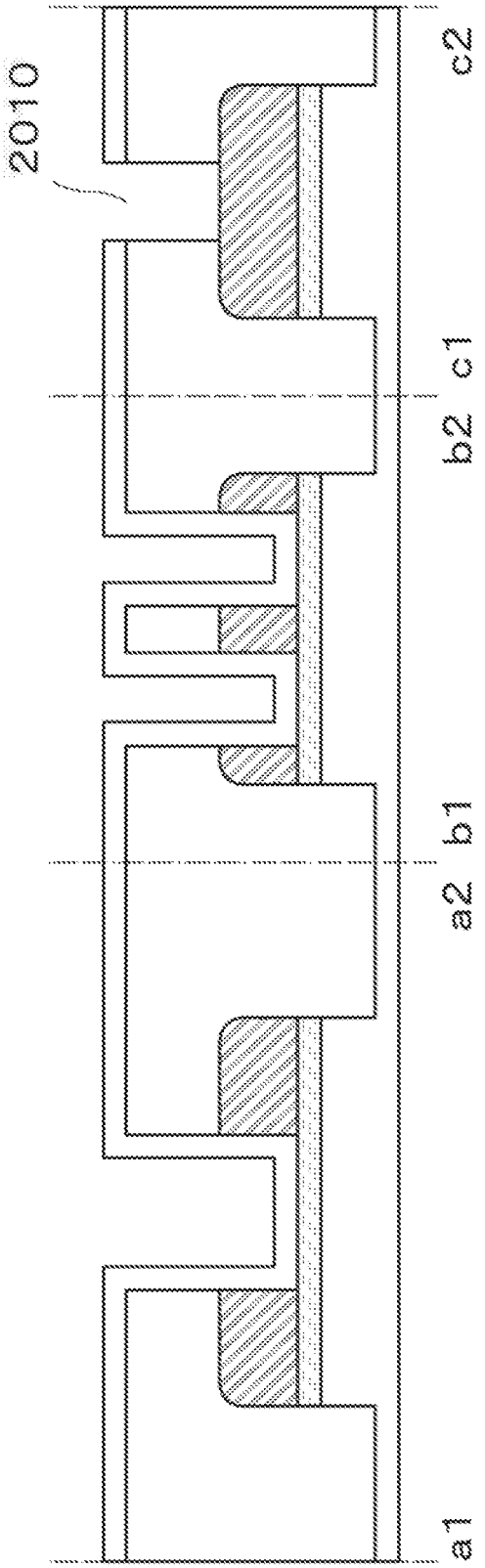


FIG. 20A

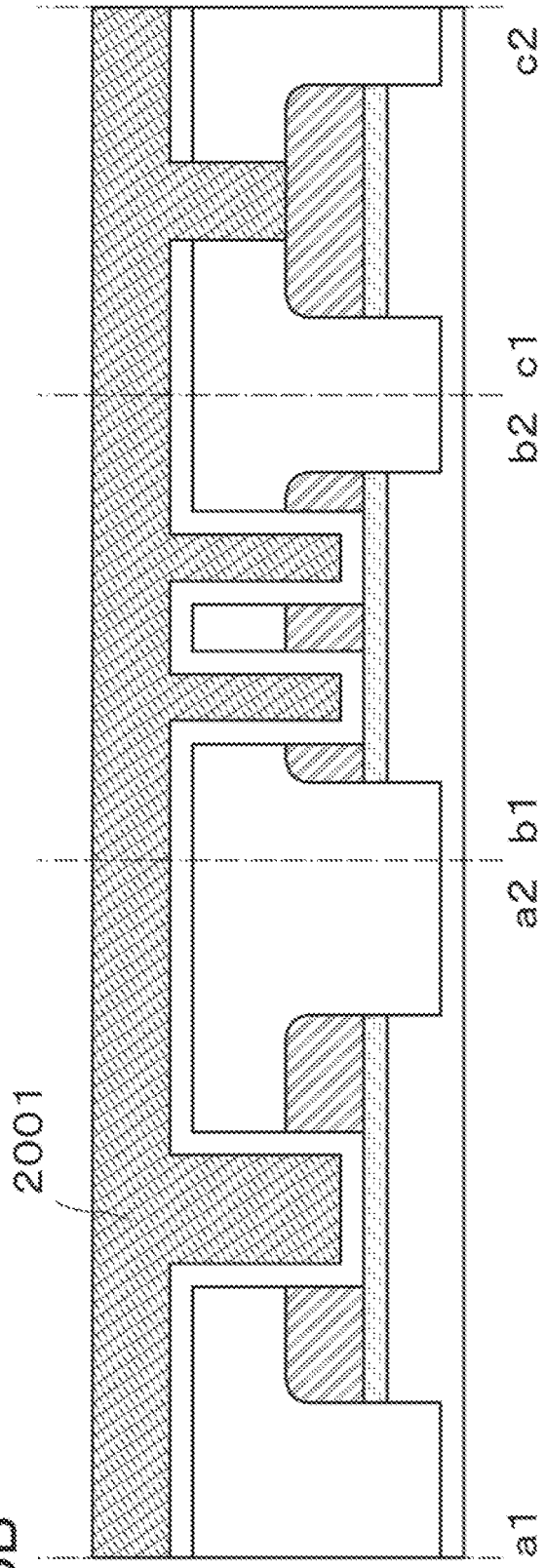


FIG. 20B

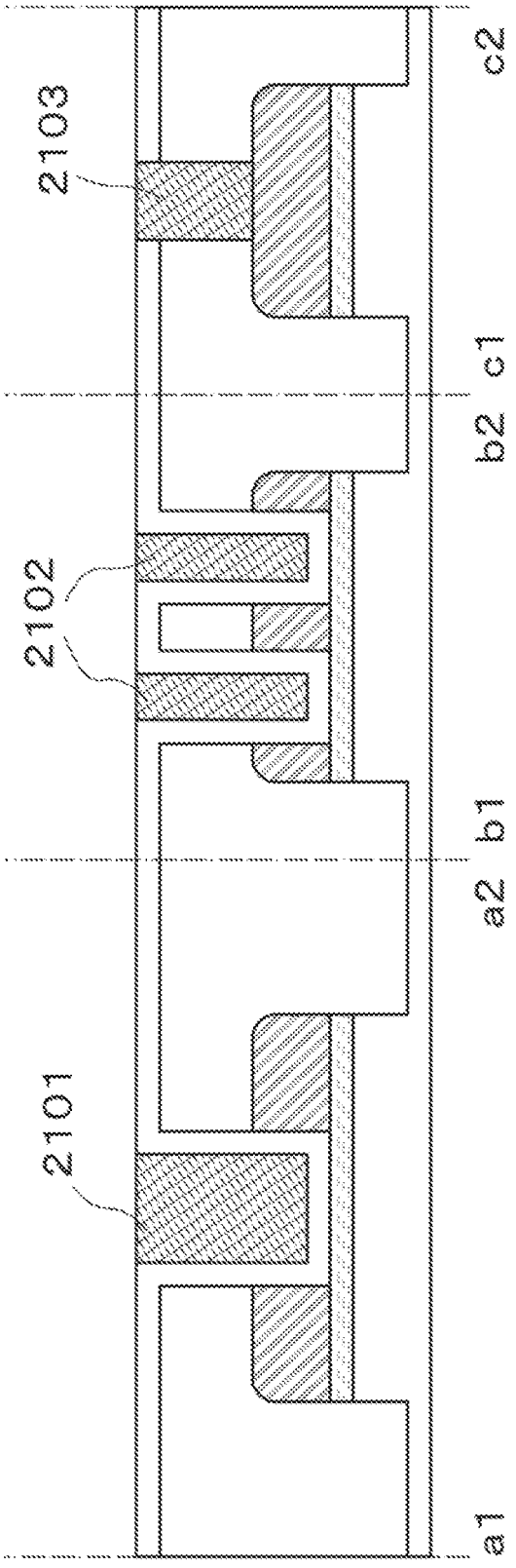


FIG. 21

FIG. 22A

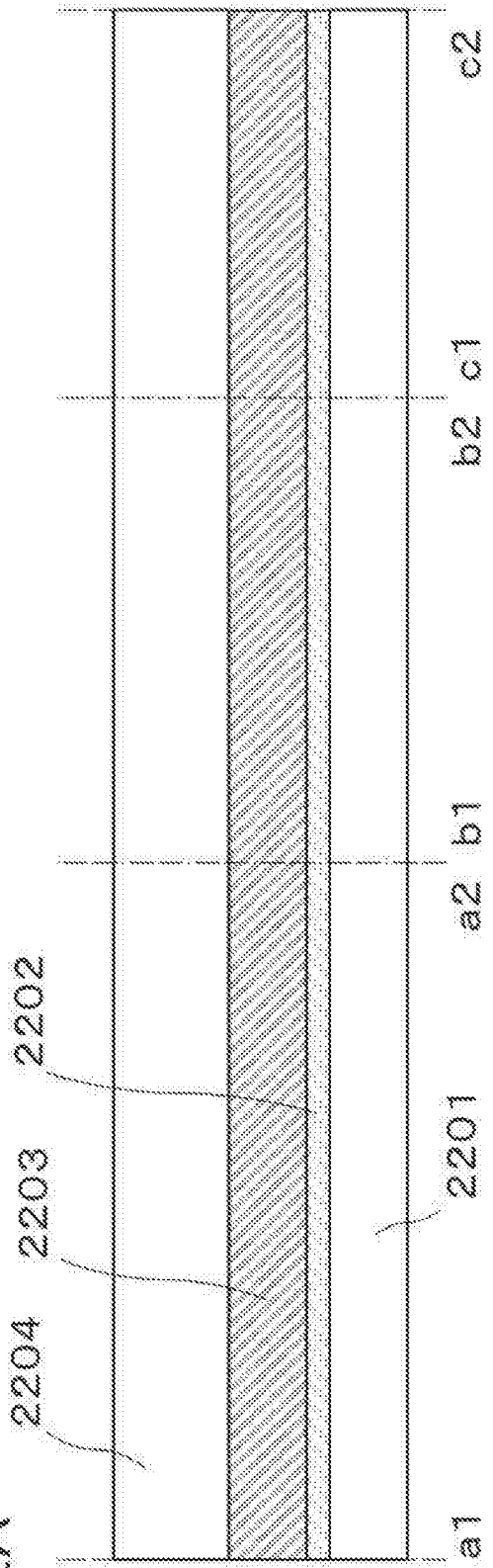
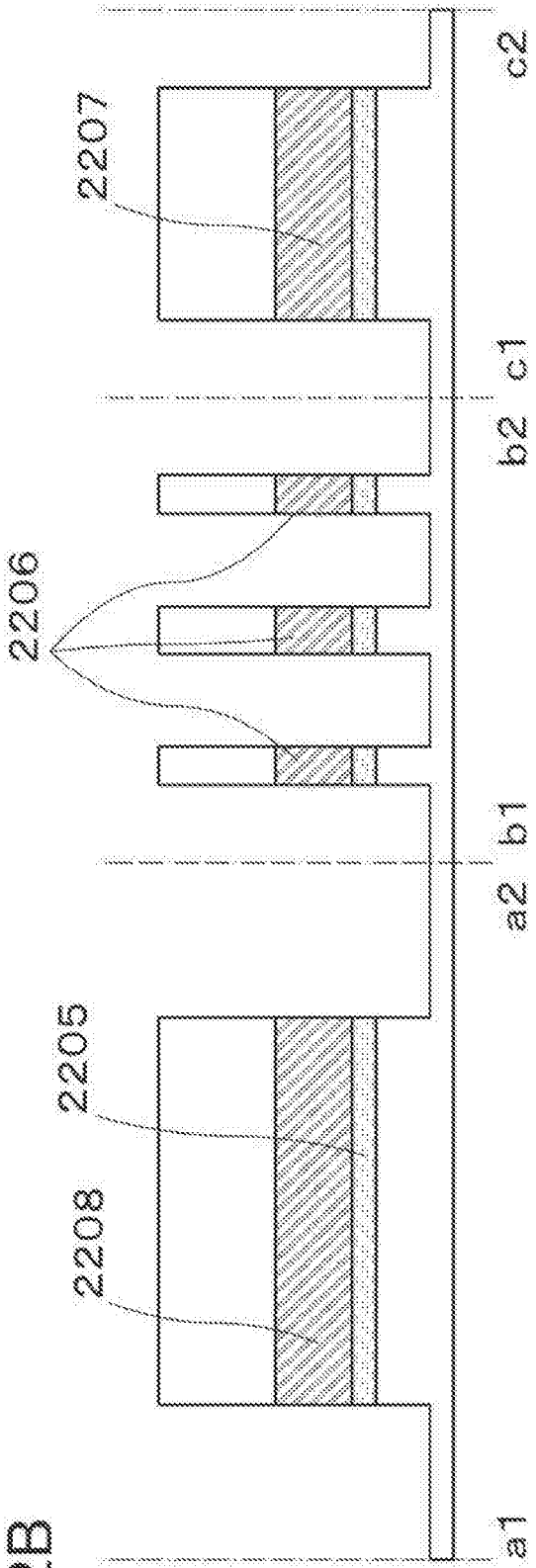


FIG. 22B



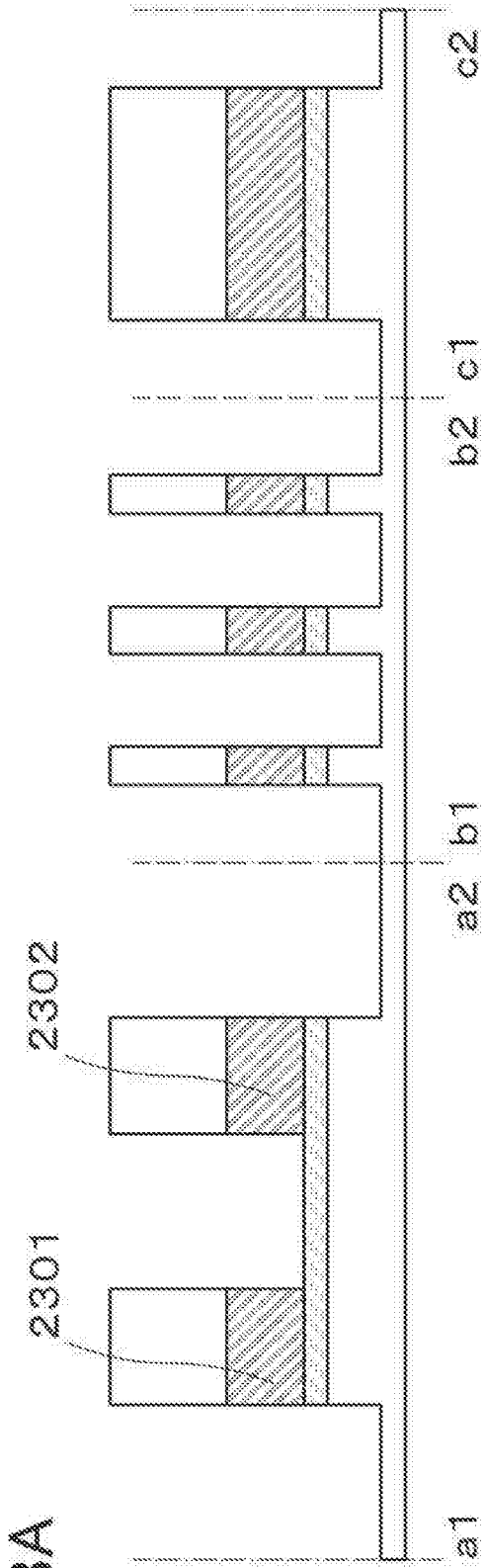


FIG. 23A

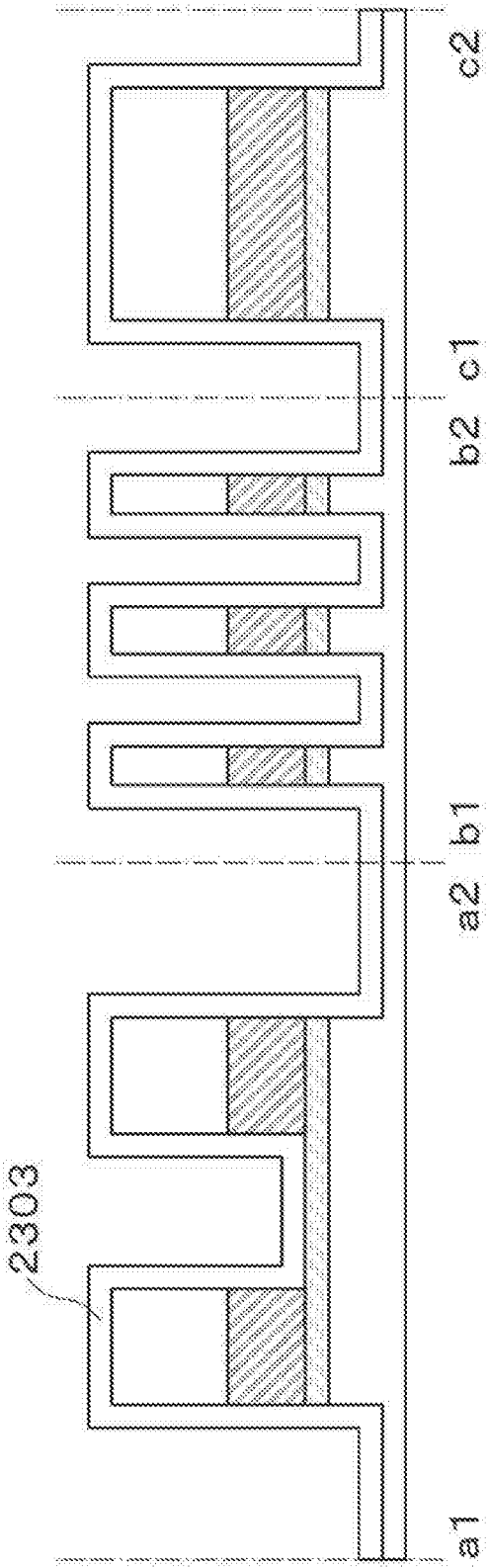


FIG. 23B

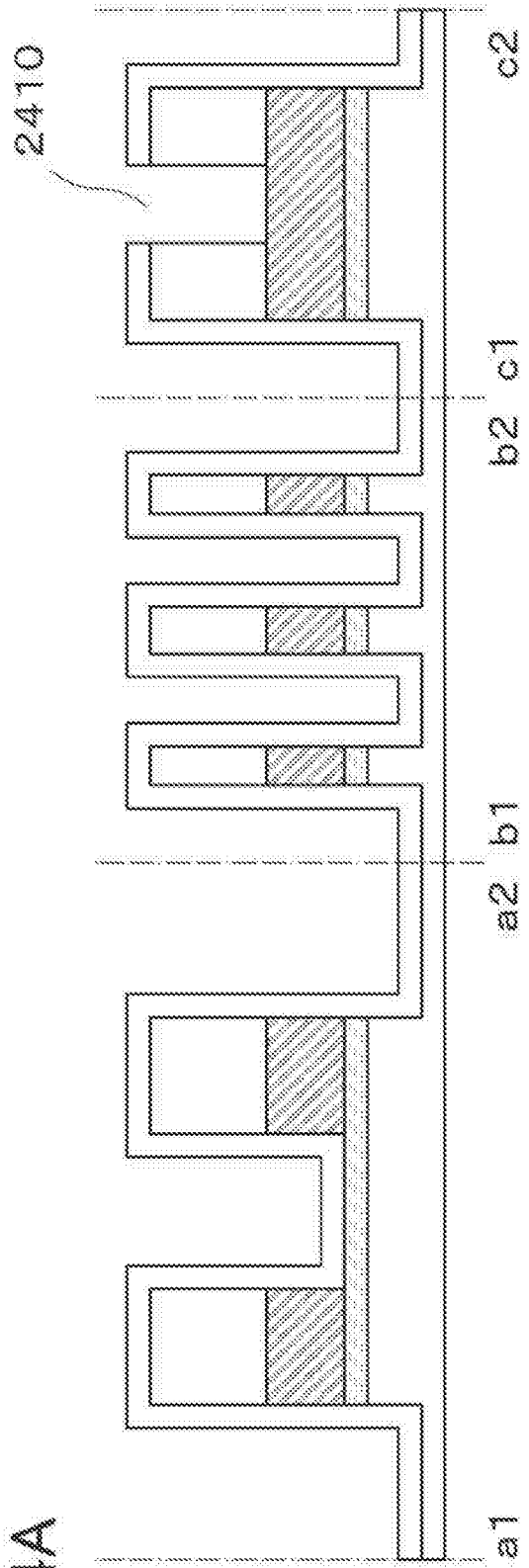


FIG. 24A

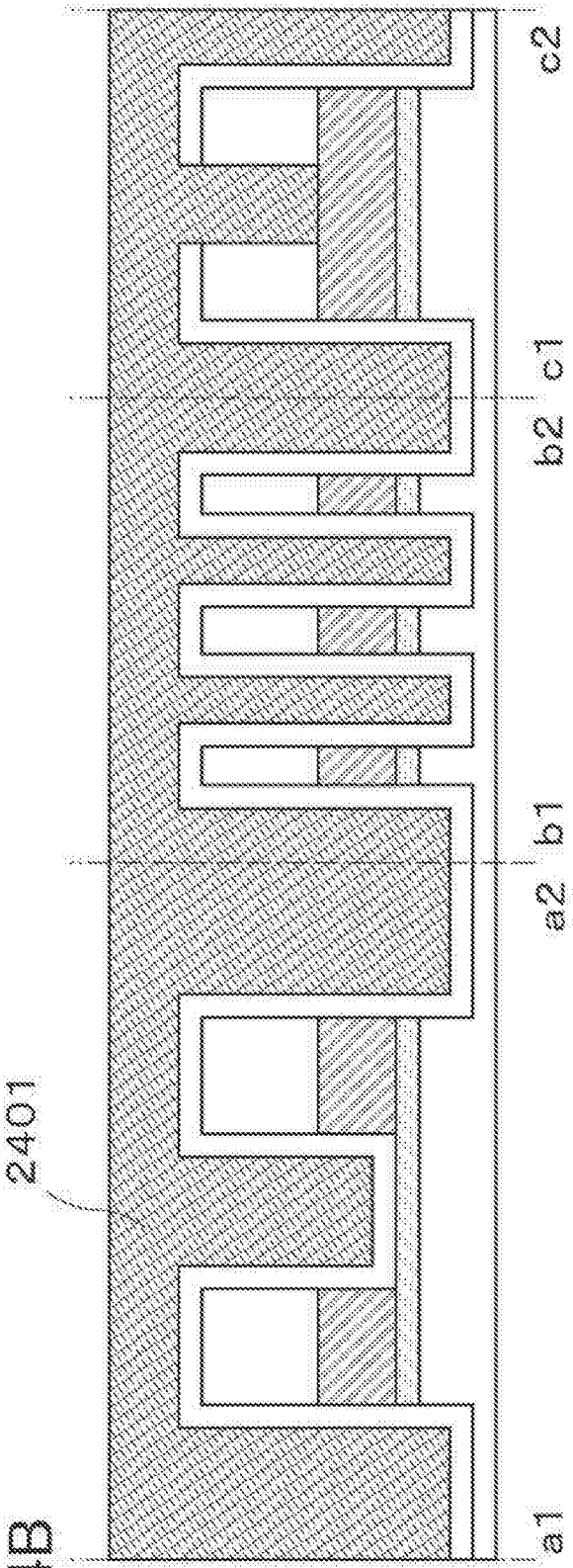


FIG. 24B

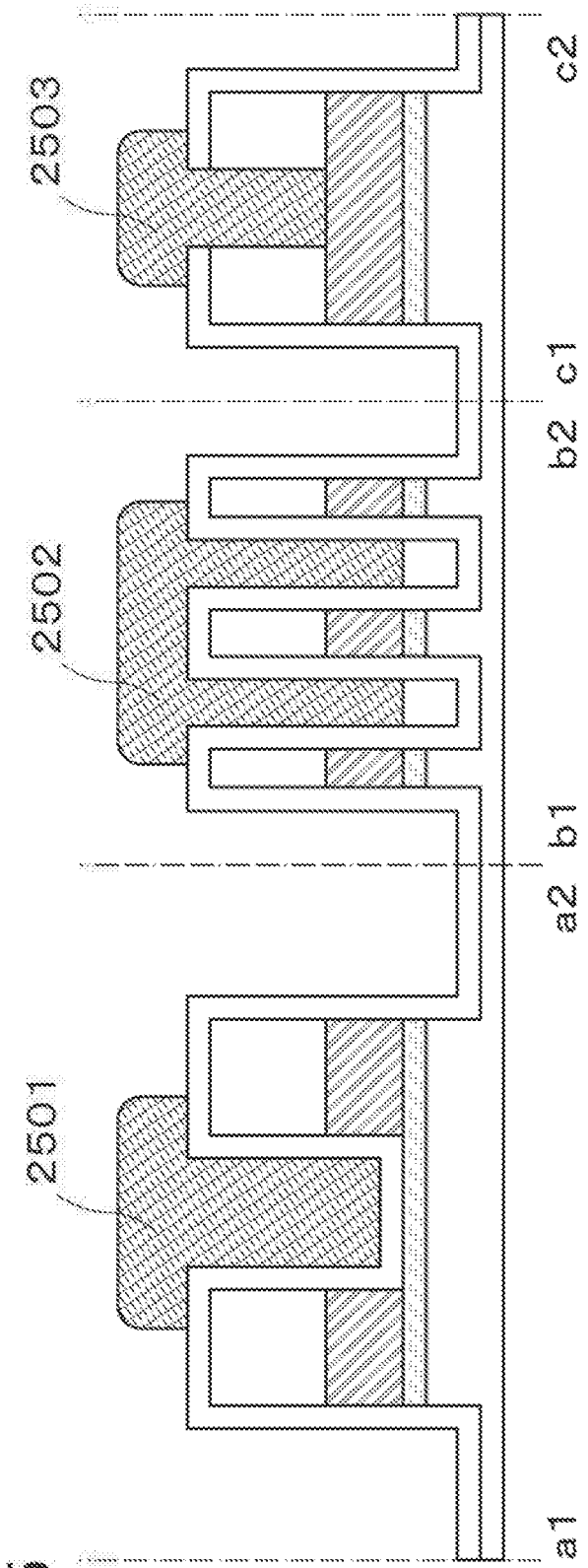


FIG. 25

FIG. 26A

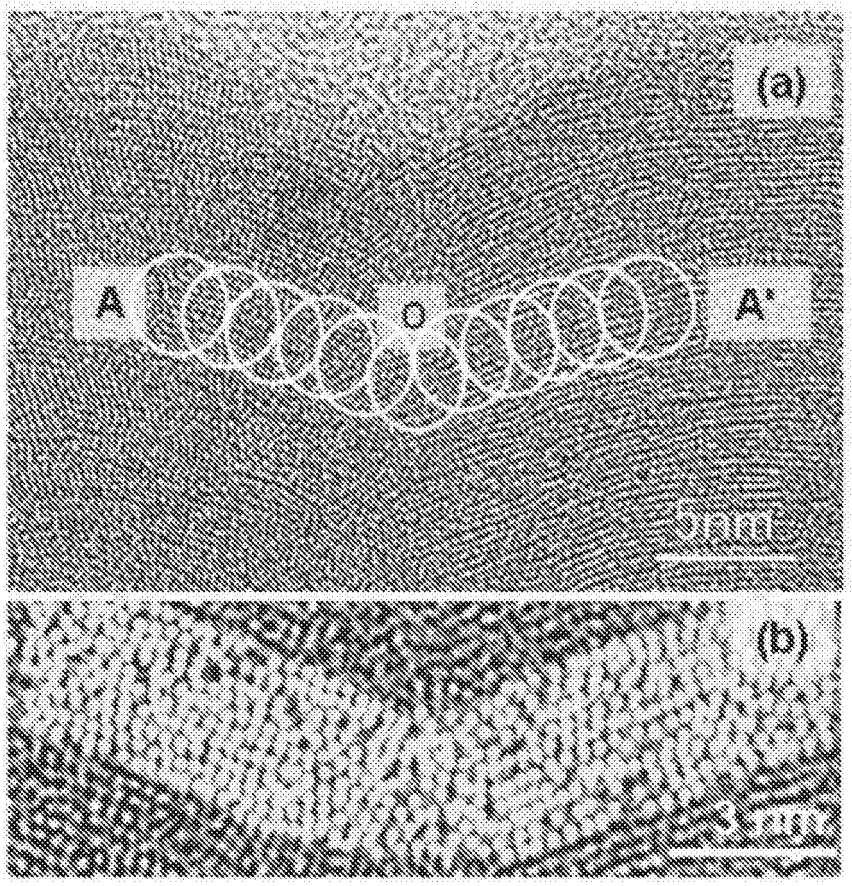


FIG. 26B

FIG. 26C

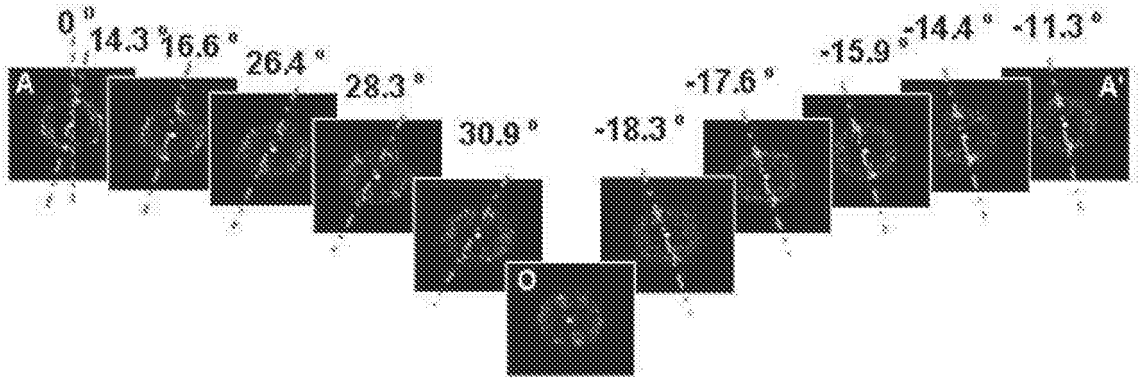
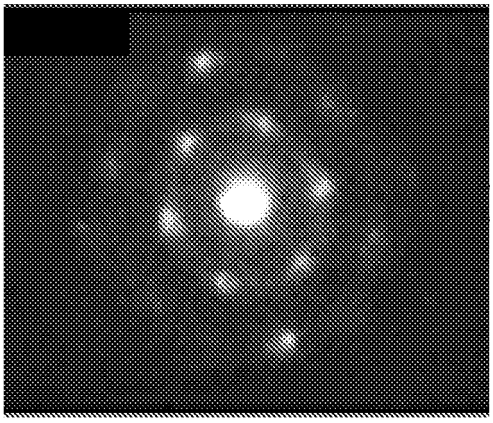
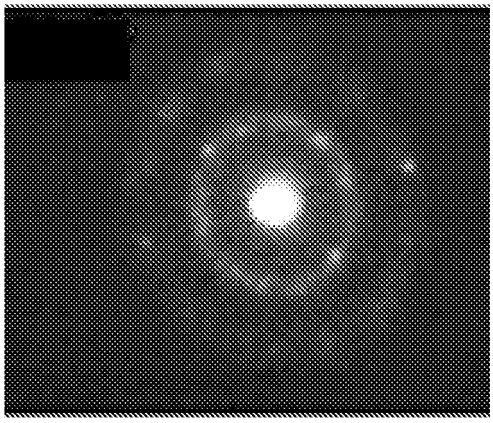


FIG. 27A



CAAC-OS

FIG. 27B



nc-OS

FIG. 27C

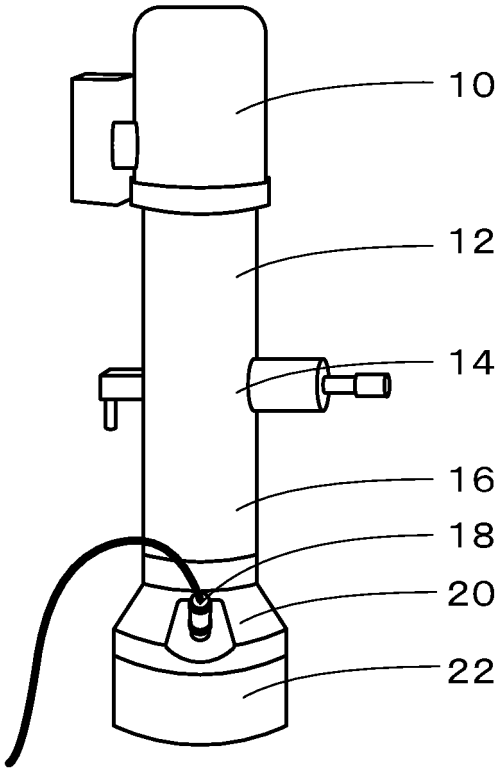


FIG. 27D

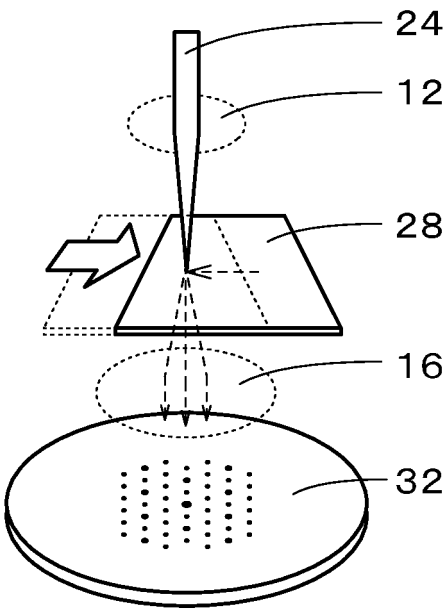


FIG. 28A

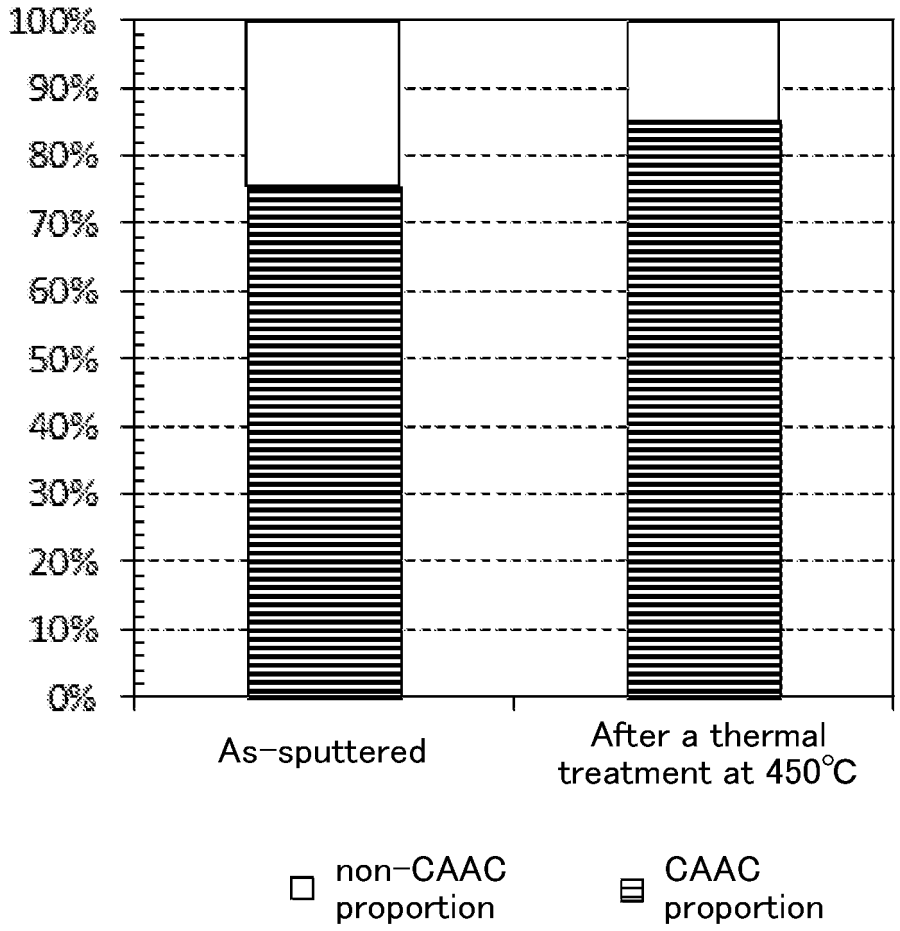
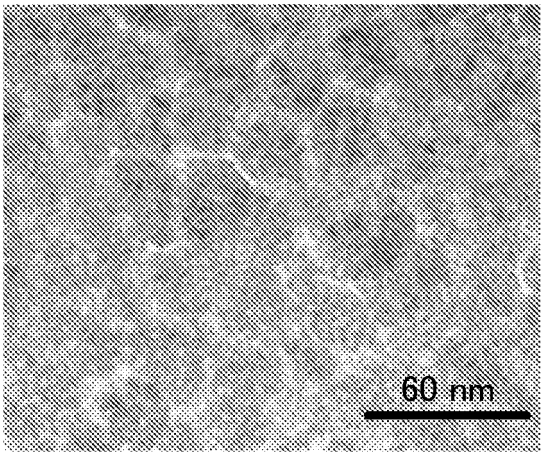
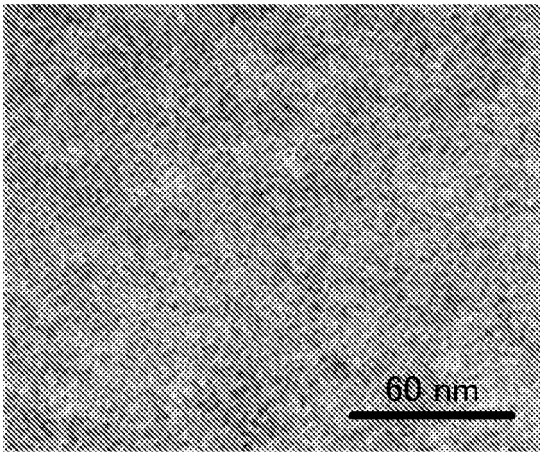


FIG. 28B



As-sputtered

FIG. 28C



After a thermal treatment at 450°C

FIG. 29A

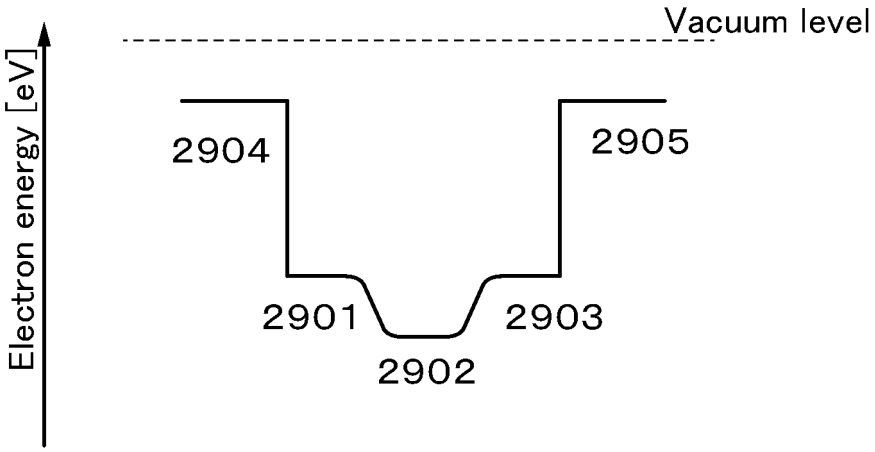


FIG. 29B

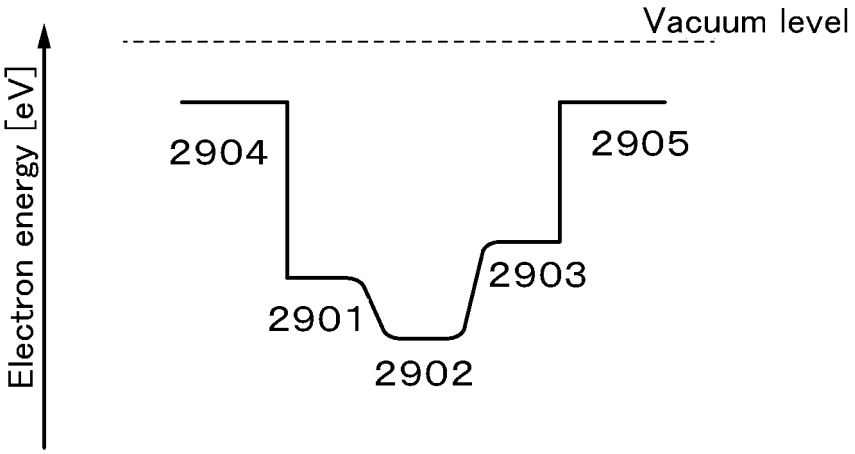
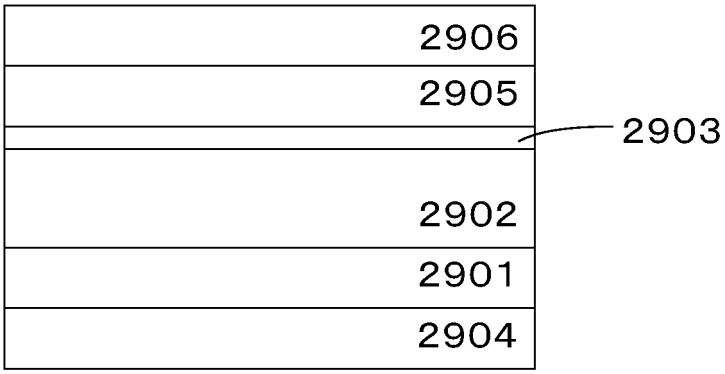


FIG. 29C



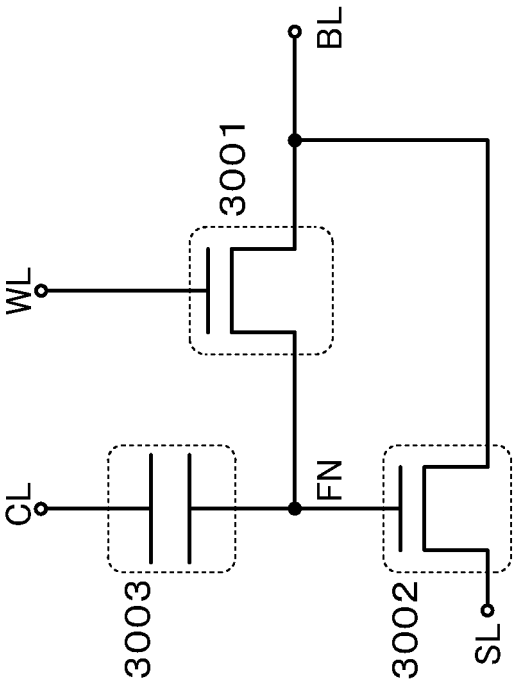


FIG. 30A

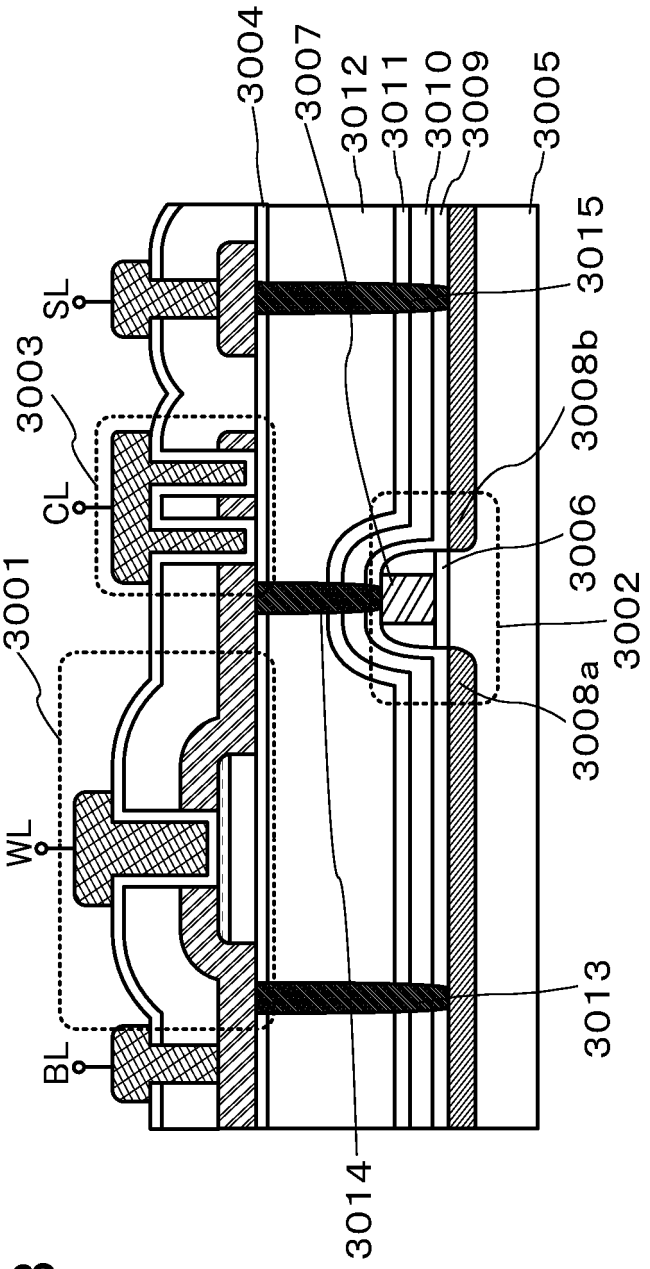


FIG. 30B

FIG. 31

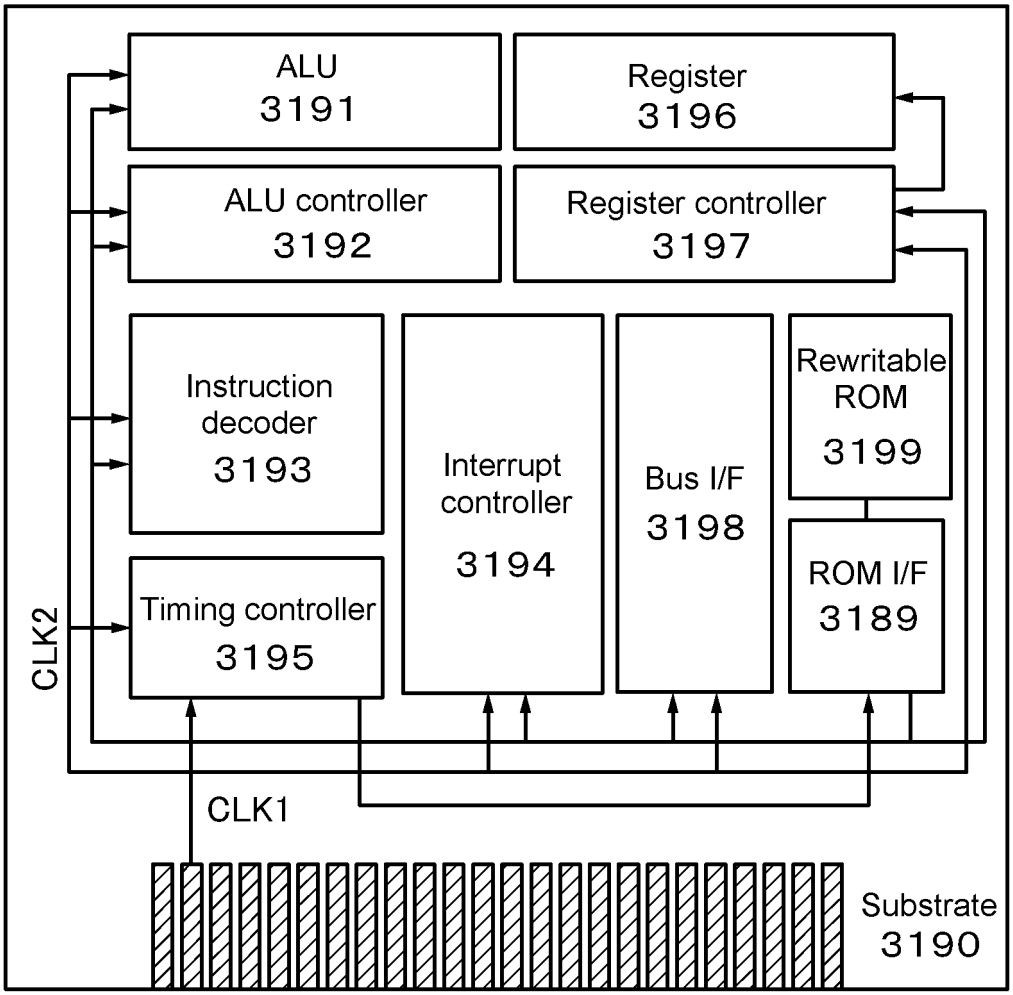

ALU
3191
Register
3196
ALU controller
3192
Register controller
3197
Instruction decoder
3193
Interrupt controller
3194
Bus I/F
3198
Rewritable ROM
3199
ROM I/F
3189
Timing controller
3195
CLK2
CLK1
Substrate
3190

FIG. 32

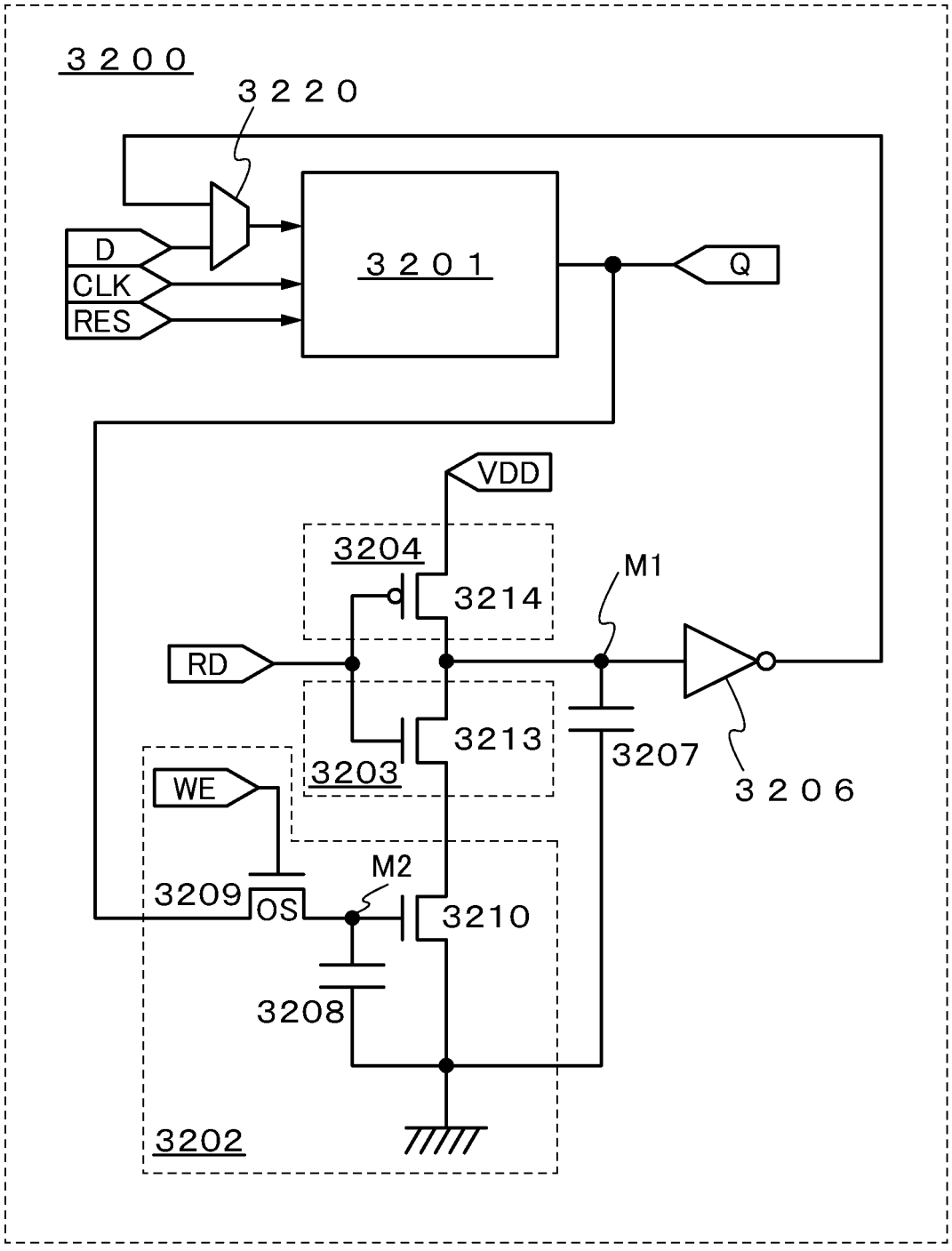

3200
3220
3201
D
CLK
RES
Q
VDD
3204
3214
M1
RD
3213
3203
3207
3206
WE
M2
3209
OS
3210
3208
3202

FIG. 33A

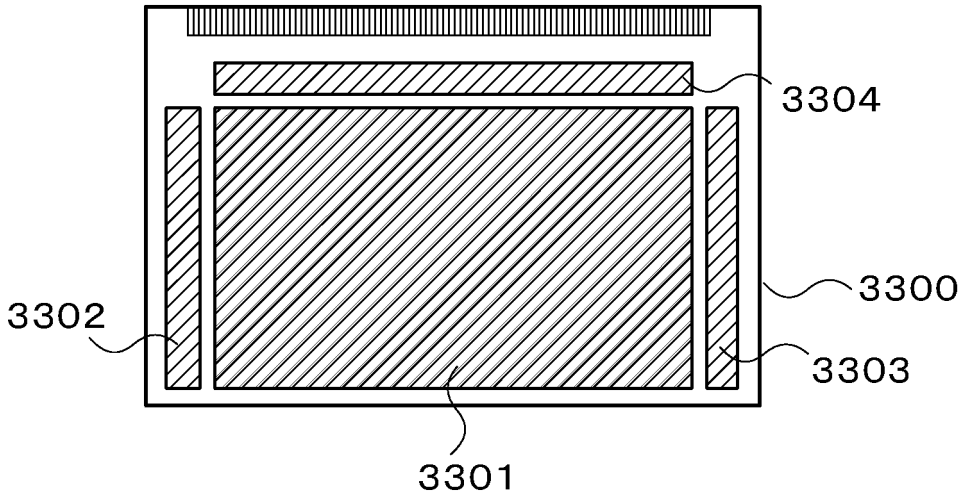


FIG. 33B

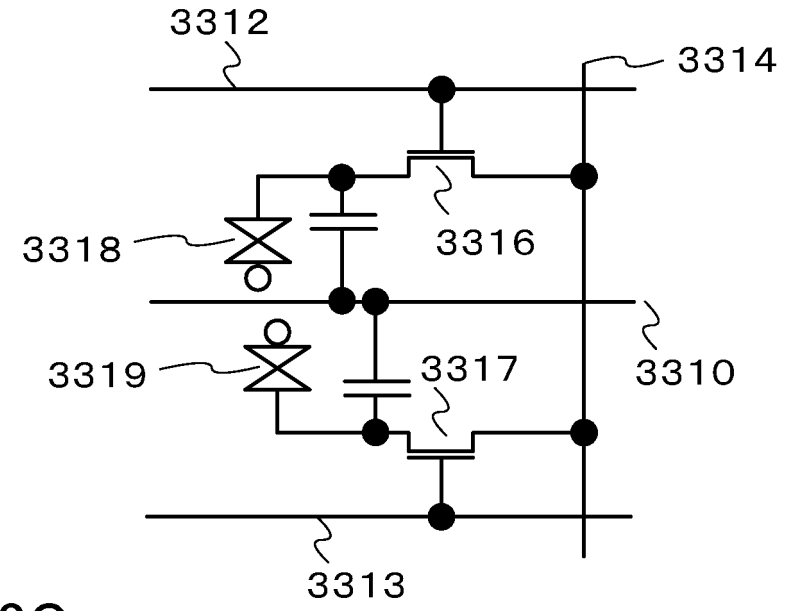


FIG. 33C

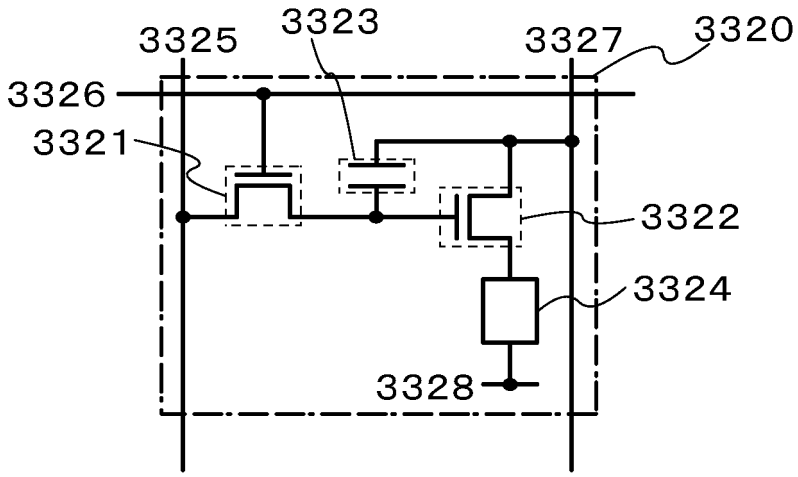


FIG. 34A

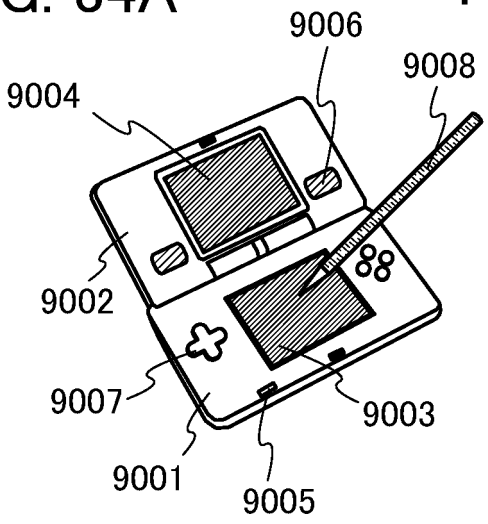


FIG. 34B

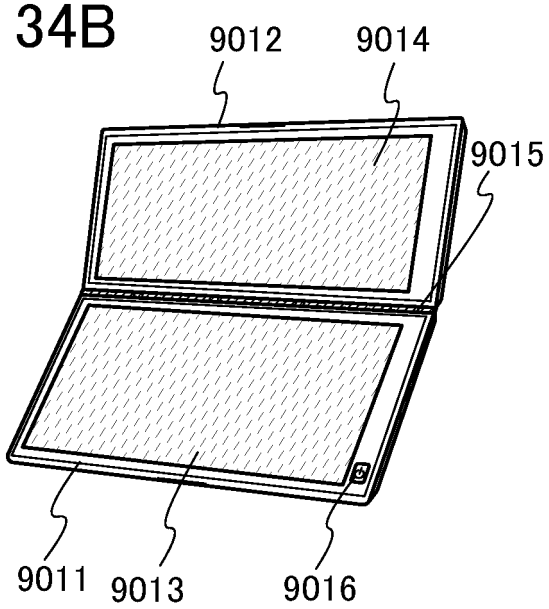


FIG. 34C

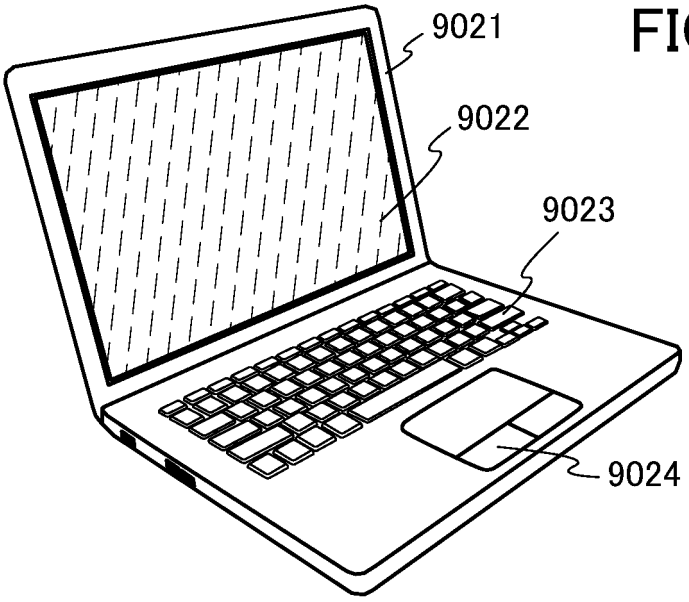


FIG. 34D

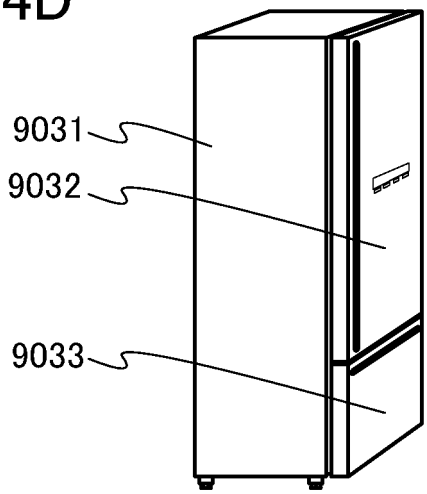


FIG. 34E

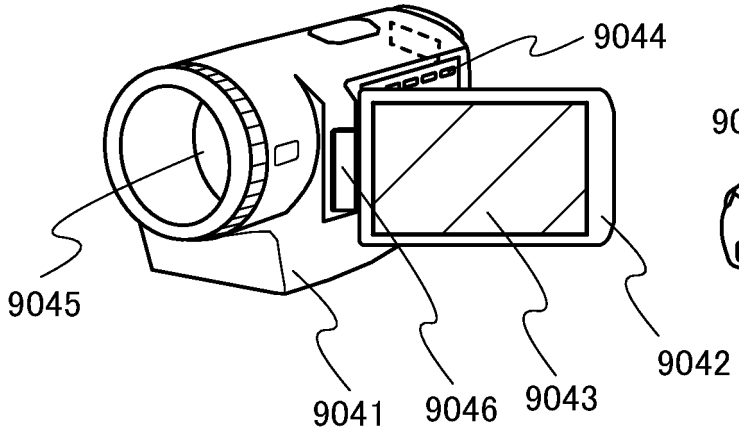
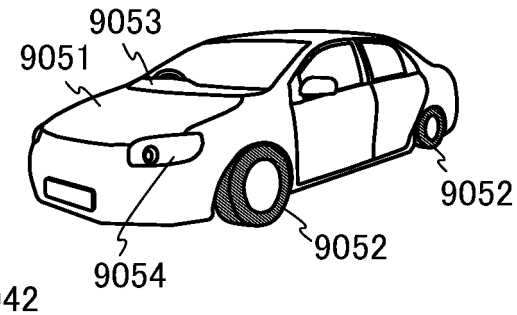



FIG. 34F