WHAT IS CLAIMED IS:

1. A decoder, the decoder comprising circuitry configured to:

receive a coded bitstream, the bitstream including a sequence parameter set, a plurality of headers, each header including a global motion enabled flag and an affine enabled flag, a picture parameter set, and a coded picture, the coded picture including a first coded region with global motion and a second coded region with local motion;

construct a motion vector candidate list in accordance with information in the sequence parameter set;

decode the first coded region using one or more motion vectors obtained based on information contained in the motion vector candidate list, and using at least one of translational motion compensation, 4-parameter affine motion compensation, and 6-parameter affine based motion compensation, wherein decoding is performed as a function of the global motion enabled flag and the affine enabled flag; and

decode the second coded region using local motion vectors for individual blocks in the second region.

2. The decoder of claim 1, the decoder configured to add a single global motion vector candidate to the motion vector candidate list.

3. The decoder of claim 1, the decoder configured to add two global motion vector candidates to the motion vector candidate list.

4. The decoder of claim 1, the decoder configured to add three global motion vector candidates to the motion vector candidate list.

5. The decoder of claim 1, wherein the global motion vector candidate includes a control point motion vector.

6. The decoder of claim 5, wherein the control point motion vector is a translational motion vector.

7. The decoder of claim 5, wherein the control point motion vector is a vector of a four parameter affine motion model.

8. The decoder of claim 5, wherein the control point motion vector is a vector of a six parameter affine motion model.

9. The decoder of claim 1, wherein the current block is a coding tree unit.

10. The decoder of claim 1, wherein the current block is a coding unit.