

(19) World Intellectual Property Organization
International Bureau



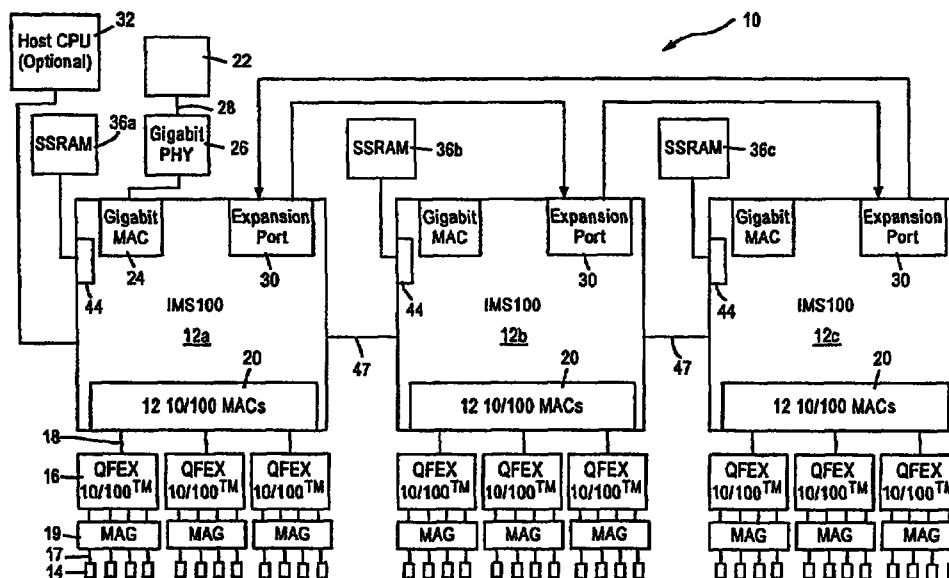
(43) International Publication Date
26 July 2001 (26.07.2001)

PCT

(10) International Publication Number
WO 01/54355 A1

- (51) International Patent Classification⁷: H04L 12/44, 12/56
- (21) International Application Number: PCT/US00/20033
- (22) International Filing Date: 21 July 2000 (21.07.2000)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/177,345 24 January 2000 (24.01.2000) US
09/562,924 2 May 2000 (02.05.2000) US
- (71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One Amd Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).
- (72) Inventors: SANG, Jinqlih, (Charlie); 42006 Via San Luis Rey, Fremont, CA 94539 (US). MERCHANT, Shashank; 1063 Morse Avenue #11-305, Sunnyvale, CA 94089 (US).
- (74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).
- (81) Designated States (national): CN, JP, KR, SG.
- (84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
- Published:
— with international search report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: APPARATUS AND METHOD FOR SHARING MEMORY USING A SINGLE RING DATA BUS CONNECTION CONFIGURATION



(57) Abstract: Multiple network switches are configured having memory interfaces that transfer segmented packet data to each other via a unidirectional data bus ring connecting the network switches in a single ring or "daisy chain" arrangement. The memory interfaces are also configured for transferring the segmented packet data to respective local buffer memories for temporary storage. The memory interfaces transfer the data units according to a prescribed sequence, optimizing memory bandwidth by requiring only one read and one write operation to and from the local buffer memory for each segmented packet data being received and transmitted through the switches.

WO 01/54355 A1