

ABSTRACT:**Receiver.**

Receiver comprising an RF section, a mixer stage and a signal processing stage, said mixer stage receiving a mixing frequency from a frequency synthesis circuit which comprises a phase-locked loop provided with a phase detection device having a current output, a loop filter comprising a π -shaped RC network having an input shunt path and an output shunt path which are connected to both ends of a series resistor incorporated in a series path and to ground and comprise first and second capacitances, respectively, and with a voltage-controlled oscillator, a reference frequency being applied to said phase detection device.

In order to prevent the use of active filter circuits in the phase-locked loop of such a receiver according to the invention, the second capacitance is chosen to be at least twice as large as the first capacitance, the series resistance is chosen to be smaller than the output impedance of the phase detection device and the output shunt path of the loop filter is provided with an RC phase shift member for reducing the phase shift of the second capacitance in the output shunt path.

Fig. 1.

This Sheet Has Been Replaced



4-8250088