

CLAIMS

1. A computer-implemented method for calibrating read voltages for a block of memory, comprising:
determining a current operating state of the block, wherein the block includes more than one word-line therein, wherein more than one read voltage is associated with each of the word-lines; and
for each of the word-lines in the block:
selecting one of the read voltages associated with the given word-line as a reference read voltage,
calculating an absolute shift value for the reference read voltage,
determining a relative shift value for each of the remaining read voltages associated with the given word-line, wherein the relative shift values are determined with respect to the reference read voltage,
and
adjusting each of the read voltages associated with the given word-line using the absolute shift value and each of the respective relative shift values.
2. The computer-implemented method of claim 1, wherein the relative shift values are determined for the remaining read voltages using a predetermined voltage mapping which corresponds to the current operating state of the block.
3. The computer-implemented method of claim 2, wherein determining the relative shift value for each of the remaining read voltages associated with the given word-line includes:
matching the current operating state of the block with a corresponding one of a number of predetermined operating states; and
extracting the relative shift values from the predetermined voltage mapping which is assigned to the matching predetermined operating state.
4. The computer-implemented method of claim 1, wherein the current operating state of the block is determined using one or more statistics which correspond to the block, wherein the one or more statistics used to determine the current operating

state of the block are selected from the group consisting of: a cycle count, a read disturb count, and a retention time.

5. The computer-implemented method of claim 1, wherein the memory is non-volatile random access memory (NVRAM).
6. The computer-implemented method of claim 5, wherein the NVRAM includes three-dimensional triple-level-cell NAND Flash.
7. The computer-implemented method of claim 5, wherein the NVRAM includes three-dimensional quad-level-cell NAND Flash.
8. A computer program product for calibrating read voltages for a block of memory, the computer program product comprising a computer readable storage medium having program instructions embodied therewith, the program instructions readable and/or executable by a processor to cause the processor to:
 - determine, by the processor, a current operating state of the block, wherein the block includes more than one word-line therein, wherein more than one read voltage is associated with each of the word-lines; and
 - for each of the word-lines in the block:
 - select, by the processor, one of the read voltages associated with the given word-line as a reference read voltage,
 - calculate, by the processor, an absolute shift value for the reference read voltage,
 - determine, by the processor, a relative shift value for each of the remaining read voltages associated with the given word-line, wherein the relative shift values are determined with respect to the reference read voltage, and
 - adjust, by the processor, each of the read voltages associated with the given word-line using the absolute shift value and each of the respective relative shift values.

9. The computer program product of claim 8, wherein the relative shift values are determined for the remaining read voltages using a predetermined voltage mapping which corresponds to the current operating state of the block.
10. The computer program product of claim 9, wherein determining the relative shift value for each of the remaining read voltages associated with the given word-line includes:
matching the current operating state of the block with a corresponding one of a
number of predetermined operating states; and
extracting the relative shift values from the predetermined voltage mapping which
is assigned to the matching predetermined operating state.
11. The computer program product of claim 8, wherein the current operating state of the block is determined using one or more statistics which correspond to the block, wherein the one or more statistics used to determine the current operating state of the block are selected from the group consisting of: a cycle count, a read disturb count, and a retention time.
12. The computer program product of claim 8, wherein the memory is non-volatile random access memory (NVRAM).
13. The computer program product of claim 12, wherein the NVRAM includes three-dimensional triple-level-cell NAND Flash.
14. The computer program product of claim 12, wherein the NVRAM includes three-dimensional quad-level-cell NAND Flash.
15. A system, comprising:
a plurality of non-volatile random access memory (NVRAM) blocks configured to store data;
a processor; and
logic integrated with and/or executable by the processor, the logic being configured to, for each of the blocks:

determine, by the processor, a current operating state of the given block, wherein the given block includes more than one word-line therein, wherein more than one read voltage is associated with each of the word-lines; and for each of the word-lines in the given block:

select, by the processor, one of the read voltages associated with the given word-line as a reference read voltage,

calculate, by the processor, an absolute shift value for the reference read voltage,

determine, by the processor, a relative shift value for each of the remaining read voltages associated with the given word-line, wherein the relative shift values are determined with respect to the reference read voltage, and

adjust, by the processor, each of the read voltages associated with the given word-line using the absolute shift value and each of the respective relative shift values.

16. The system of claim 15, wherein the relative shift values are determined for the remaining read voltages using a predetermined voltage mapping which corresponds to the current operating state of the block.
17. The system of claim 16, wherein determining the relative shift value for each of the remaining read voltages associated with the given word-line includes:
matching the current operating state of the block with a corresponding one of a number of predetermined operating states; and
extracting the relative shift values from the predetermined voltage mapping which is assigned to the matching predetermined operating state.
18. The system of claim 15, wherein the current operating state of the block is determined using one or more statistics which correspond to the block, wherein the one or more statistics used to determine the current operating state of the block are selected from the group consisting of: a cycle count, a read disturb count, and a retention time.

19. The system of claim 15, wherein at least some of the NVRAM blocks are included in three-dimensional triple-level-cell NAND Flash.
20. The system of claim 15, wherein at least some of the NVRAM blocks are included in three-dimensional quad-level-cell NAND Flash.
21. A computer-implemented method for calibrating read voltages for a block of memory, comprising:
 - determining a current operating state of the block, wherein the block includes more than one type of page therein, wherein at least one read voltage is associated with each of the page types;
 - for each word-line in the block:
 - dividing the read voltages into groups based on the respective page types;
 - and
 - for each group of read voltages in the given word-line:
 - selecting one of the read voltages in the given group as a reference read voltage,
 - calculating an absolute shift value for the reference read voltage,
 - determining a relative shift value for each of the remaining read voltages in the given group, wherein the relative shift values are determined with respect to the reference read voltage,
 - and
 - adjusting each of the read voltages in the given group using the absolute shift value and each of the respective relative shift values.
22. The computer-implemented method of claim 21, wherein each of the read voltages in a given group correspond to a same page type.
23. The computer-implemented method of claim 21, wherein the relative shift values are determined for the remaining read voltages in the given group using a predetermined voltage mapping which corresponds to the current operating state of the block and the type of pages in the given group.

24. The computer-implemented method of claim 23, wherein determining the relative shift value for each of the remaining read voltages in the given group includes: matching the current operating state of the block and the type of pages in the given group with a corresponding one of a number of predetermined operating states; and extracting the relative shift values from the predetermined voltage mapping which is assigned to the matching predetermined operating state and which corresponds to the type of pages in the given group.
25. The computer-implemented method of claim 21, wherein the current operating state of the block is determined using one or more statistics which correspond to the block, wherein the one or more statistics used to determine the current operating state of the block are selected from the group consisting of: a cycle count, a read disturb count, and a retention time.