

The invention relates to a serial interface in accordance with the introductory part of claim 1. Such a serial interface is known from "Electronics and Communications in Japan", Vol. 49, No. 5, May 1966, pages 27 to 34; H. Inose et al: "Data concentration and distribution system with capabilities of message storage and speed conversion".

In the case of the serial transmission of digital signals which are arranged into a predetermined frame structure it is known to use, for the data processing, a data processor which carries out calculations in a program-controlled manner. These calculations are interrupted during the acquisition of new data or the output of calculated data. If the data that are to be accepted arrive temporally staggered as bits combining into data words, the necessary interruptions for the acceptance of the data can add up to such a total time that in the case of extensive calculations there is no longer sufficient time to perform them.

The problem underlying the invention is, therefore, to design a serial interface in accordance with the introductory part of claim 1 in such a way that the time needed for the acquisition of the data is considerably reduced and thus a longer coherent time is obtained for calculations of the processor.

This problem is solved, in the case of the serial interface in accordance with the introductory part of claim 1, by the features expressed in the characterising part.

The data, which yield a data record that is to be processed coherently by the processor, are stored temporally in succession in the shift register. Acceptance of the data into the processor is effected only when all the correlated data are present, namely in a temporally coherent interval. If acceptance of the data is so time-scaled that it can be fitted into the interval between two consecutive data, the data stream is not disturbed by this procedure.

The time-scaling takes place in that the shift register between the instants of the arrival of two consecutive data is clocked with a higher clock frequency than in the case of the normal data transport. In this respect, at the same time the data output of the shift register is connected to its input. By way of the loop formed in this way the data of an entire data word run through the shift register once and then again occupy the same storage cells as previously. The data transfer itself takes place in this phase by way of the output of the storage cell lying nearest to the data input of the shift register.

Further developments and advantageous embodiments will become apparent from the further claims, the description and the drawings, in which an exemplified embodiment is illustrated. In the drawings:

Fig. 1 shows a circuit diagram embodying the invention, as a component of a receiver for digital satellite broadcast;

Fig. 2 shows a pulse diagram to explain the circuit shown in Fig. 1.

Fig. 3 shows an extended time sector of the pulse diagram from Fig. 1.

The interface shown in Fig. 1 and designated as a whole by 1 lies between a data line 2 and a data processor 3. Data - hereinunder called DA - are transmitted at a frequency of 32 kHz on the data line. It is a matter, in this respect, of the special service bit in the main frame A in accordance with the specifications of the sound radio broadcasting procedure in TV-SAT, as are described 'inter alia' in DE-OS 33 08 025.

An evaluation circuit, not shown in more detail, selects the DA from the data stream, stores them temporarily and passes them, upon the arrival of the next DA, to the data line 2. A first clock signal with a frequency of 32 kHz - hereinunder called T32N - accepts with its negative edge the DA appearing on the data line 2 through a data input SE into a shift register 4. With further clock signals T32N the written-in data are shifted on from storage cell to storage cell and, after the eighth storage cell, read-out by way of a data output Q8. In the data stream in each case eight coherent DA form data words, which the data processor 3 is to further process. The correlated DA are in each case identified by an interrupt signal INTR, which is issued after the eighth DA.

In order to be able to accept the eight DA into the data processor 3, in the second part of that clock period of T32N which is contemporaneous with INTR a second clock signal with a frequency which is 16-times higher is applied to the clock input T of the shift register 4 and to a clock input of the data processor 3. The second clock signal is obtained from a clock signal T1024N, made available by the evaluation circuit, with a frequency of 1024 kHz by dividing-down to 512 kHz. However, the clock signal edges of T1024N do not possess, for all the data sequences contained in the frame structure mentioned at the beginning hereof, the correct clock signal edge related to T32N, since upon its generation no common divider is present between a data block relocation of 77 bits and a frequency division of five to one. In order to be able to use T1024N generally as clock source for the second clock signal, additionally a program-code synchronisation signal PCSY is taken into account and is linked by a logic element 5 with T1024N to form TFFN. The latter is then supplied to a flip-flop 6 serving as divider.

As a result of the interrupt signal INTR, which is linked by a logic element 7 with T32N, a reset instruction RFF for

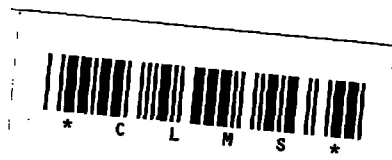
the flip-flop 6 is cancelled and the data processor 3 is freed for the acceptance of data by an acceptance signal UDP derived from the INTR. At the output Q of the flip-flop 6 there now appears the clock signal T512N, which passes to the clock input of the data processor 3 as TDP and by way of a logic element 8 to the clock input of the shift register 4 as TSR512.

By way of a logic element 9 alternatively data on the incoming data line 2a can be supplied to the data input SE of a shift register 4 or to the data output Q8 or respectively to the outgoing data line 2b. The allocation procures a "Program Mode Serial Decoupling" signal - called PASA - serving as auxiliary signal. This PASA possesses the same frequency as T32N, but leads temporally by for instance approximately 200 nsec, which is advantageous when writing DA into the shift register 4 after a preceding transmission of DA to the data processor.

During the second half of the period of PASA, in which this signal is logic H and the shift register 4 is clocked with TSR512, the data that are to be accepted pass by way of the output Q1 of the shift register (4) as DDP to the data input of the data processor and moreover run through the entire shift register 4 once. After that the data again stand in the same storage cells in which they stood prior to commencement of the described procedure. Then the data processor 3, by changing the logic state of INTR, is again shifted into the state which makes the data processing in accordance with the intended program possible and blocks the flip-flop 6.

In good time prior to the writing of new data DA into the shift register the signal PASA changes its logic state, so that, as a result of the negative edge of T32N arriving shortly after that, the first DA of the next data word can be accepted again. As a result of the temporal shift of PASA and T32N it is thus possible to place the transmission of the data to the data processor 3 into the second part of the clock period of T32N without having to interrupt the clock signal.

During the following seven clock periods of T32N the data processor 3 is in a position to process the accepted data in a coherent program flow, until a new data record of eight DA has been written into the shift register 4 and the described procedure of the data acceptance into the data processor is repeated.



CLAIMS

1. A serial data interface between a data line (2) transmitting a continuous digital data stream and a digital data processor (3), the interface having a shift register which is arranged serially in the data line, characterised in that the data line (2) comprises an incoming data line (2a) and an outgoing data line (2b), in that an output (Q1) of the storage cell lying nearest to the data input (SE) of the shift register (4) is connected to the input of the digital data processor (3) and in that by means of a control circuit in a first mode of operation at a first clock frequency (T32N) the data line (2), and in a second mode of operation at a second higher clock frequency (T512N) the data input (Q8) of the shift register, is connected to the data input (SE) of the shift register (4) and the data processor (3) is switched to data acceptance.
2. An interface according to claim 1, characterised in that the incoming data line (2a), the data output (Q8) and a control line are connected by way of a logic element (9) to the data input (SE) of the shift register.
3. An interface according to claim 1 or 2, characterised in that the control circuit comprises an evaluation circuit for a first clock signal (T32N) obtained from the serial data stream and for a higher-frequency clock signal (T512N) obtained from a data stream or a frequency multiplier.
4. An interface according to any one of claims 1 or 2, characterised in that an auxiliary signal (PASA) which is of identical frequency to the first clock signal (T32N) but which leads temporally is obtained through the evaluation circuit.
5. An interface according to claim 3 or 4, characterised in that the serial data stream (DSA) is formed by the special service bit in the main frame in accordance with the frame structure of the Digital Satellite Broadcast in the TV-SAT.
6. An interface according to any one of claims 3 to 5, characterised in that the higher-frequency clock signal (T512N) is formed or obtained by a clock signal, accompanying the sample values in the main frame, in accordance with the frame structure of the Digital Satellite Broadcast in the TV-SAT.
7. An interface according to any one of claims 3 to 6, characterised in that a clock line conducting the clock signal (T32N) of the first clock frequency and a clock line conducting the clock signal (T512N) of the second clock frequency are connected by way of a logic element (8) to a clock input (T) of the shift register.
8. An interface according to any one of claims 3 to 7, characterised in that the second clock frequency (T512N) is



higher than the first one (T32N) at least by the factor which corresponds to twice the number of the individual data, e.g. individual bits, forming a data word.

9. An interface according to claim 8, characterised in that a gate (7) controlled by the first clock signal (T32N) is provided, through which the second clock signal (T512N) is applied only during the second part of the clock period of the first clock signal (T32N).

10. An interface according to any one of claims 3 to 8, characterised in that the initial and/or end cycle of the second mode of operation is shortened for the acceptance of data into the shift register (4) and into the data processor (3).



(Translation of legends to the drawings)

Fig. 1

Eing. = input

Ausg. = output

Daten Proz. = data processor