9900928-6
1005 copy 6

Title: **Self-Aligned Unlanded Via Metallization**

Background of the Invention.

1. Field of the Invention.

The present invention relates to the formation of wiring structures in integrated circuit devices. More particularly, the present invention relates to the formation of vias and interconnects extending through vias to buried wiring lines or pads.

2. Description of the Related Art.

Many highly integrated semiconductor circuits utilize multilevel wiring line structures for interconnecting regions within devices and for interconnecting one or more devices within the integrated circuit. In forming such structures, it is conventional to form a first level wiring line, deposit an intermetal dielectric layer over the wiring line, form a via through the intermetal dielectric layer to expose a portion of the first level wiring line, and then deposit metal into the via to form a vertically extending interconnect or "plug." A second level of wiring lines is then formed on the intermetal dielectric layer, with one of the second level wiring lines in contact with the plug, connecting the first level wiring line to other conductors in the circuit. Conventional methods of forming vias through intermetal dielectrics, along with the methods conventionally used for forming

metal plugs as vertical interconnects between wiring levels, can produce unacceptably resistive interconnections, resulting in unsatisfactory interconnect structures.

A conventional multilevel wiring line structure and a method of making the structure are illustrated in FIGS. 1-3. FIG. 1 shows a semiconductor circuit at an intermediate step in the manufacturing process with a layer of insulating material 12 covering a semiconductor substrate 10. A first level wiring line 14 is provided on the layer of insulating material 12, with the wiring line typically making contact with one or more devices formed in or on the semiconductor substrate at a remote location (not shown). An intermetal dielectric layer 16 covers the first level wiring line 14 and portions of the layer of insulating material 12 not covered by first level wiring structures. FIG. 2 shows the FIG. 1 device after a via 18 is formed through the intermetal dielectric layer 16 down to the surface of the first level wiring line 14. The via is formed by anisotropic etching. Often, vias are formed near the ends or edges of wiring lines or contact pads. Either by design or due to alignment and manufacturing errors, it is possible that a portion of the via may be formed over an edge of the first level wiring line 14, forming a so-called "unlanded via." When unlanded vias are formed, and particularly when the via etch process uses a metal surface of wiring line 14 as an etch stop, the via etch may extend along a sidewall of the first level wiring line into intermetal dielectric layer 16, forming a cavity 20 adjacent the wiring line 14.

FIG. 3 illustrates the FIG. 2 structure after further manufacturing steps that form a metal plug 24 within the via to make contact with the first level wiring line 14. In a typical configuration, the first level wiring line 14 may be aluminum, copper, an alloy of aluminum with silicon or copper, or other inexpensively manufactured conducting material. The metal plug 24 is often formed from tungsten, but other materials including aluminum or copper might be used. It is conventionally understood that forming a metal plug 24 will fill in any cavity 20 alongside a wiring line within an unlanded via. In practice, interconnect structures of the type illustrated in FIG. 3 may exhibit varying

levels of resistivity, both on a run-to-run basis and within a single wafer. Both high resistances and varying resistances are unacceptable for interconnect structures because they damage device performance and produce lower yields.

Summary of the Preferred Embodiments.

It is therefore an object of the present invention to provide a method of making metal interconnect structures that have a more uniform and predictable level of resistivity.

An embodiment of the present invention provides a method of forming an interconnect structure in a semiconductor device. A conductive layer is formed adjacent a first insulating layer above a semiconductor substrate, with the conductive layer and the first insulating layer having coplanar upper surfaces. An etch stop layer, different from the first insulating layer, is deposited on the upper surfaces of the conductive layer and the first insulating layer. A second insulating layer, different from the etch stop layer, is deposited on the etch stop layer and a via is formed which exposes a portion of the etch stop layer at least partially above the conductive layer. The etch stop layer is removed within the via and the via is filled with a conductive material.

In accordance with another aspect of the present invention, an interconnect for a semiconductor device is formed by providing an insulating layer having an edge and an upper surface disposed above a portion of the semiconductor substrate. A metal layer is provided alongside the edge of the insulating layer, where the metal layer has an upper surface and is electrically connected to the semiconductor substrate. An etch stop layer is deposited on the upper surfaces of the insulating layer and the metal layer and then a dielectric layer is deposited over the etch stop layer. A via is formed through the dielectric layer to expose the etch stop layer and then the etch stop layer is removed within the via to expose at least a portion of the metal layer. A metal plug is formed within the via, connecting the metal layer to a conductor formed above the dielectric layer.

Yet another aspect of the present invention forms an interconnect for a semiconductor device by providing an insulating layer over a semiconductor substrate

and then forming a pattern of depressions in the insulating layer. The metal layer is planarized to form a pattern of metal wiring lines within the insulating layer corresponding to the pattern of depressions. An etch stop layer is deposited on surfaces of the insulating layer and the metal layer and a dielectric layer is deposited over the etch stop layer. A via is etched through the dielectric layer to expose the etch stop layer and the etch stop layer is removed within the via to expose at least a portion of the metal layer. A metal plug is formed within the via.

Brief Description of the Drawings.

FIGS. 1-3 illustrate a conventional interconnect to a first level wiring line, along with a method of making the structure.

FIG. 4 illustrates a difficulty that arises when using tungsten plug technology with an unlanded via structure.

FIGS. 5-11 illustrate steps in the formation of multilayer wiring structures in accordance with the present invention.

Detailed Description of the Preferred Embodiments.

The present invention provides a method of forming interconnects between different level wiring lines. Preferred embodiments of the invention find particular application in contacting a lower level wiring line through an unlanded via, that is, a via that lies only partially over the first level wiring line. Such unlanded vias may be formed by design or may be formed inadvertently, particularly in reduced geometry devices. Overetching of unlanded vias forms gaps alongside of metal wiring lines, which can increase the resistance of contacts made through the vias in an unpredictable manner. The present invention reduces the possibility that gaps formed by overetching unlanded vias affect the resistivity of the contacts made through those vias. In addition, preferred embodiments of the present method find particular applicability when tungsten plug technology or a similar technology is used for filling vias. As is discussed in greater detail below, the use of chemical vapor deposition to form plugs, and more particularly to

form tungsten plugs, within unlanded vias may be prone to forming poisoned vias having high or unpredictable resistances. Use of preferred embodiments of the present invention facilitate the more reliable formation of tungsten plugs within unlanded vias.

Briefly, preferred embodiments of the present invention provide an etch stop layer over a first level wiring line and over an adjacent first insulating layer. A second insulating layer is typically deposited on the etch stop layer above the first level wiring line and the first insulating layer. Contact to the first level wiring line is made by etching a via through the second insulating layer, using the etch stop layer to limit the vertical extent of the via etching process. The etch stop layer is removed within the via, a vertically extending interconnect or plug is formed within the via, and a second level wiring line is formed in contact with the interconnect plug.

In a more detailed embodiment, the present invention forms a multilevel interconnect structure on a first insulating layer over a semiconductor substrate by forming depressions on the surface of the first insulating layer. Excess portions of the metal layer are removed from the surface of the first insulating by chemical mechanical polishing, planarizing the surface of the metal layer with the first insulating layer, and thereby forming a pattern of first level wiring lines. An etch stop layer of a material, preferably different from the first insulating layer, is deposited on the first level wiring lines and over the first insulating layer. A second insulating layer, preferably of a material different from the layer of etch stop material, is deposited over the etch stop layer. A via is formed through the second insulating layer and the etch stop layer is removed from within the via. When the via is unlanded, removal of the etch stop layer within the via will expose both a portion of a first level wiring line and a portion of the first insulating layer. Because an etch stop layer is used in preferred embodiments of the invention, the preferred via etch process can form a via without forming a gap alongside the wiring line. As discussed further below, this aspect of the invention has particular advantages in some embodiments of the invention. After the via is opened, a glue or adhesion layer is deposited within the via, a plug of tungsten or another conductor is formed within the via, and then a second level wiring line is formed in contact with the tungsten plug.

Aspects of the present invention, including some illustrated in this more detailed embodiment, avoid at least some via poisoning mechanisms, thereby forming interconnects that more reliably have low resistance levels. One of the via poisoning mechanisms which is addressed by aspects of the present invention is illustrated in FIG. 4. FIG. 4 shows a first level wiring line 14 formed on an insulating layer 12 covering a semiconductor substrate 10. An unlanded via is formed through insulating layer 16 in an etching process like that described above with reference to FIG. 2, resulting in the formation of the unlanded via shown, along with a cavity 20 adjacent the metal wiring line 14. To facilitate the adhesion of a tungsten plug to the via, an adhesion or glue layer 22 is typically formed within the via. A tungsten plug 24 is then formed within the via by selective chemical vapor deposition using a source gas such as WF_6.

Several problems arise with a structure like that illustrated in FIG. 4. First, it is typical to use a plasma etchant derived from a gas including carbon and fluorine such as CF_4 or C_2F_6 in etching the via, so that the via etch process will typically result in the formation or deposition of polymers as a byproduct of the etching reactions. Often, these polymers are trapped in the cavity 20 formed adjacent the metal wiring line, and remain within the cavity 20 even after cleaning with a solvent such as ACT 935 (produced by Ashland Chemicals). The polymer residue within the cavity 20 is a source of contamination for each of the subsequent processing steps in the formation of the interconnect. For example, deposition of the glue layer, which might consist of the physical vapor deposition (*e.g.*, by sputtering) of titanium or titanium nitride, has poor step coverage over the contaminated cavity 20. Thus, the typical result of depositing a glue layer 22 within an unlanded via includes the formation of a partially closed cavity having contaminants such as polymers trapped inside. The subsequent chemical vapor deposition of tungsten from a WF_6 source gas appears to interact with the polymer residue trapped within the cavity 20, possibly resulting in the formation of a tungsten plug having a poor quality interface with the underlying first level wiring line 14. These residues may also interfere with the formation of good contacts between the tungsten plug and the overlying second level wiring line.

The present invention addresses these difficulties, in essence, by avoiding formation of a cavity 20 during an unlanded via etch to a first level wiring line. Preferred embodiments of the present invention are now discussed with reference to FIGS. 5-11. These figures illustrate steps in the formation of a particular configuration of an interconnect structure. While these embodiments illustrate particularly preferred embodiments of the invention, aspects of the present invention find application in other configurations of interconnects or using other constituent materials. In addition, while the following discussion identifies first and second level wiring lines, it should be understood that these are labels only and that the present invention may be applied to higher level wiring lines or for forming connections between non-adjacent (*e.g.*, first and third or other) levels of wiring lines.

The present invention can be incorporated into a variety of different methods for forming wiring and interconnect structures. One method of forming a pattern of appropriate first level wiring lines provides a metal layer over a semiconductor device and then patterns the metal layer into wiring lines using conventional lithography. A layer of insulating material is then deposited over the pattern of metal wiring lines and then chemical mechanical polishing or an etch back process is performed to remove portions of the insulating layer above the first level wiring lines. The polishing or etching process provides a pattern of metal wiring lines with insulating regions separating the metal wiring lines, with the surfaces of the wiring lines being substantially coplanar with the surface of the insulating regions. The steps illustrated in FIGS. 7-11 may then be performed in the manner described below.

A different, and presently more preferred, method of forming wiring lines in accordance with the present invention utilizes a damascene process. FIG. 5 shows a substrate 10 that preferably has a plurality of semiconductor devices formed therein (not shown). Typically, a layer of passivating or insulating material 12 is present on the surface of the integrated circuit device, although it is possible that the first level wiring lines are in direct contact with at least parts of the substrate or with at least parts of semiconductor devices in the substrate. A layer 30 of dielectric material, such as a layer of silicon oxide, is deposited by, for example, plasma enhanced chemical vapor

deposition (PECVD). Conventional photolithography is performed to form a photoresist mask or a hard mask exposing the dielectric layer 30 above regions corresponding to the pattern of wiring lines to be formed. Anisotropic etching is performed to form trenches or depressions to a depth of between about 2,000-10,000 Å into the dielectric layer 30. In some circumstances, the etching depth may extend through the dielectric layer 30, using the underlying passivating or insulating layer 12 as a stop for the etching of the trenches. In other circumstances, the etching process may extend only partially through the dielectric layer 30, using the time duration of the etch to determine the depth of the trenches within the thicker dielectric layer 30.

Metal is then deposited over the surface of the device, filling the trenches or depressions in the dielectric layer 30 and covering other portions of the surface of the dielectric layer 30. The deposited metal might be tungsten deposited by chemical vapor deposition (CVD) or "hot" aluminum deposited using physical vapor deposition (PVD) techniques. The first level wiring lines might include layered or other composite structures comprising different types of metals, or including both metals and other materials. After the metal layer is deposited, excess metal is removed from the surface of the dielectric layer 30 by etching or, more preferably, by chemical mechanical polishing to provide metal wiring lines 32 having upper surfaces substantially coplanar with the surface of the dielectric layer 30, as shown in FIG. 6. The trench etching, metal deposition and chemical mechanical polishing of the preferred wiring line formation process provides a pattern of narrow first metal wiring lines more reliably than other metal deposition and photolithography processes.

Next, an etch stop layer 34 (FIG. 7) is formed over the surface of the device, covering the surface of the first level metal wiring line 32 and exposed regions on the surface of the dielectric layer 30. Preferably, the etch stop layer 34 is formed of an insulating material which is different from the dielectric material in layer 30. Most preferably, the etch stop layer 34 is formed of a material that is also different from the layer 36 of insulating material deposited on the etch stop layer. The use of different materials allows etch processes through the multilayer insulating structure to be stopped at each interface. Typically, the dielectric layer 30 is formed of silicon oxide and the

layer 36 of insulating material deposited on the surface of the etch stop layer 34 is also silicon oxide. An appropriate material for the etch stop layer might therefore be silicon nitride. Etching processes can be highly selective between silicon oxide and silicon nitride, particularly when using a high density plasma etching process such as inductively coupled plasma or helicon wave plasma.

The silicon nitride etch stop layer 34 can be deposited by CVD to a thickness of between about 200-1000 Å. Preferably, layer 34 is sufficiently thick to reliably act as an etch stop. The necessary thickness may be as little as 100 Å, depending on the thickness of the dielectric layer 36 through which the via is formed and depending on the planarity of the surfaces of the dielectric layer 30 and the metal wiring line 32. If the polishing process preferred for forming the FIG. 6 structure results in a significant step between the surfaces of the dielectric layer 30 and the metal wiring line 32, then a thicker layer of silicon nitride may be necessary to ensure the preferred complete step coverage. After the etch stop layer is formed, an intermetal dielectric layer 36 is formed by, for example, PECVD of silicon oxide.

A via is then formed through the intermetal dielectric layer 36. A via etch mask is formed on the surface of the intermetal dielectric layer by conventional photolithography or equivalent means. A via 38 is then etched, preferably using an anisotropic process in a high density plasma etcher with a plasma derived from a mixture of source gases including CF_4, C_2F_6 and CO_2. This etch step preferably stops on the etch stop layer 34. The etch stop layer is then etched within the via 38, using, for example, an anisotropic etching process with a plasma derived from CHF_3 that stops on the surface of the dielectric (silicon oxide) layer 30. The via etch mask is removed either at this time or before removing the etch stop layer.

Referring to FIG. 9, an adhesion or glue layer 40 is preferably deposited over the surface of the intermetal dielectric layer 36 and within the via 38. Use of such a glue layer is preferred as improving the adhesion between the conducting plug and the first level wiring line, reducing the possibility of lift off. The glue layer 40 may be titanium, titanium nitride, titanium tungsten, tantalum, tantalum nitride, or other suitable materials

either alone or in combination, typically deposited to a thickness of a few hundred Angstroms by a physical vapor deposition process.

Preferably, a metal plug 42 is then formed within the via in contact with the glue layer, as shown in FIG. 10. For example, a tungsten plug may be formed by CVD of tungsten using a WF_6 source gas. Under some circumstances it may be appropriate to use other materials for forming the plug 42, including for example aluminum. The presently preferred tungsten CVD process deposits tungsten over the entire glue layer. Thus, for devices in which the glue layer covers a portion of the intermetal dielectric layer 36, it is preferred that a CMP or etch back process is used to remove the deposited tungsten from the surface of the dielectric layer 36 outside of the via, and to planarize the tungsten plug with the upper surface of dielectric layer 36, forming a plug 42 as illustrated. In the preferred polishing process, the glue layer 40 is removed from the surface of the dielectric layer 36. Consequently, it is desirable to deposit a second glue layer 44, similar in constitution and in deposition process to the first glue layer 40, over the dielectric layer 36 and over the plug 42. The resulting structure is shown in FIG. 11.

Processing continues to form a second level of wiring lines, including a second level wiring line 46 in contact with the second level glue layer 44, as illustrated by FIG. 11. The process described herein is compatible with a range of different materials for the second level wiring lines, including tungsten and aluminum, formed by a variety of different processes. While the present invention has been described in terms of forming an interconnect between first and second wiring layers, this should be understood as generically referring to a connection formed between conductors or conducting regions on different levels. The method does not require that the conductors be wiring lines or that the conductors be formed on adjacent levels, although certain aspects of the present invention will find their most preferred application to such structures.

While the present invention has been described in terms of certain preferred embodiments, those of ordinary skill will appreciate that various modifications and alterations to the embodiments described herein might be made without altering the basic function of the present invention. Accordingly, the scope of the present invention is not

limited to the particular embodiments described herein; rather, the scope of the present invention is to be determined from the following claims.

What is claimed:

1. A method of forming an interconnect structure in a semiconductor device comprising:

providing a conductive layer adjacent a first insulating layer above a semiconductor substrate, the conductive layer and the first insulating layer having coplanar upper surfaces;

depositing an etch stop layer, different from the first insulating layer, on the upper surfaces of the conductive layer and the first insulating layer;

depositing a second insulating layer, different from the etch stop layer, on the etch stop layer;

etching a via to expose a portion of the etch stop layer, the etched via formed at least partially above the conductive layer;

removing the etch stop layer within the via; and

filling the via with a conductive material.

2. The method of claim 1, wherein the conductive layer is a metal and wherein the coplanar upper surfaces of the conductive layer and the insulating layer are provided by polishing.

3. The method of claim 1, wherein the coplanar surfaces of the conductive layer and the insulating layer are provided by etching back the insulating layer.

4. The method of claim 1, wherein the step of removing the etch stop layer also exposes a portion of the insulating layer.

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

* C L M S *

5. A method of forming an interconnect for a semiconductor device comprising:

providing an insulating layer having an edge and an upper surface disposed above a semiconductor substrate;

providing a metal layer alongside the edge of the insulating layer, the metal layer having an upper surface;

depositing an etch stop layer on the upper surfaces of the insulating layer and the metal layer;

depositing a dielectric layer over the etch stop layer;

forming a via through the dielectric layer to expose the etch stop layer;

removing the etch stop layer within the via to expose at least a portion of the metal layer; and

forming a metal plug within the via connecting the metal layer to a conductor formed above the dielectric layer.

6. The method of claim 5, wherein the step of removing also exposes a portion of the insulating layer.

7. The method of claim 5, further comprising the step of depositing a glue layer on the metal layer within the via.

8. The method of claim 7, wherein the metal plug is formed by chemical vapor deposition of plug metal within the via and over a surface of the dielectric layer, followed by removal of the plug metal from above the surface of the dielectric layer.

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

9. A method of forming an interconnect for a semiconductor device comprising:

providing an insulating layer over a semiconductor substrate;

forming a pattern of depressions in the insulating layer;

depositing a metal layer over the insulating layer;

planarizing the metal layer to form a pattern of first level metal wiring lines within the insulating layer corresponding to the pattern of depressions;

depositing an etch stop layer on surfaces of the insulating layer and the metal wiring lines;

depositing a dielectric layer over the etch stop layer;

etching a via through the dielectric layer to expose the etch stop layer;

removing the etch stop layer within the via to expose at least a portion of a metal wiring line; and

forming a metal plug within the via.

10. The method of claim 9, wherein the step of removing also exposes a portion of the insulating layer.

11. The method of claim 9, further comprising the step of depositing a glue layer on the metal wiring line within the via.

12. The method of claim 11, wherein the metal plug is formed by chemical vapor deposition of plug metal within the via and over a surface of the dielectric layer, followed by removal of the plug metal from above the surface of the dielectric layer.

13. The method of claim 9, further comprising the step of forming a second level wiring line in contact with the dielectric layer and the metal plug, the metal plug connecting the second level wiring line to the first level wiring line.

14. The method of claim 9, wherein the step of forming a pattern of depressions includes steps of forming a mask on the insulating layer and etching partially through the insulating layer.

15. The method of claim 14, wherein the step of planarizing comprises a step of chemical mechanically polishing the metal layer.

16, The method of claim 15, wherein the insulating layer is silicon oxide and the etch stop layer is silicon nitride.

17. The method of claim 16, wherein the dielectric layer comprises silicon oxide.

18. The method of claim 14, wherein the metal plug is formed by first depositing a glue layer over the first level wiring line within the via.

19. The method of claim 18, further comprising the step of depositing tungsten at least within the via by chemical vapor deposition.

20. The method of claim 19, further comprising the step of forming a second level wiring line in contact with the dielectric layer and the metal plug, the metal plug connecting the second level wiring line to the first level wiring line.