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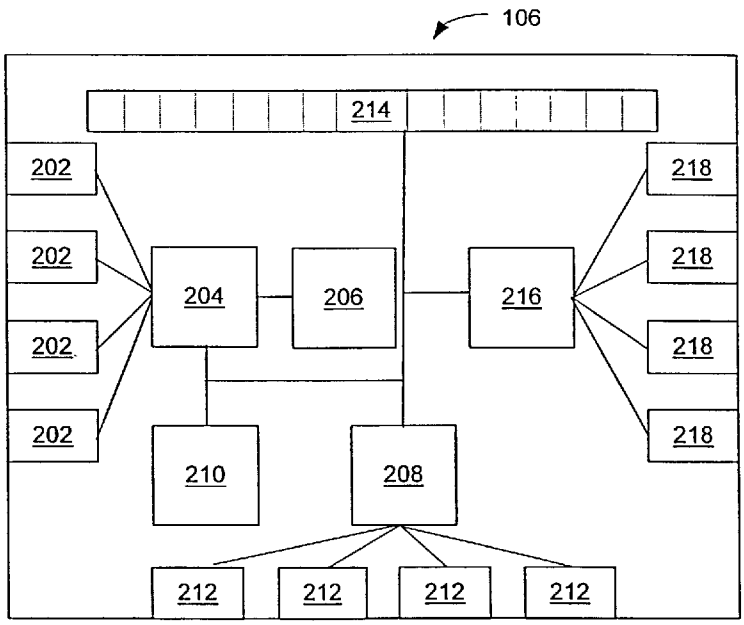
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(54) Title: SCHEDULER FOR A DATA MEMORY ACCESS HAVING MULTIPLE CHANNELS



(57) Abstract: A scheduler configured to schedule multiple channels (212) of a Data Memory Access (DMA) includes a shift structure (600) having entries corresponding to the multiple channels (212) to be scheduled. Each entry (602) in the shift structure includes multiple fields (604). Each entry (602) also includes a weight that is determined based on these multiple fields (604). The scheduler (508) also includes a comparison-logic circuit that is configured to then sort the entries based on their respective weights.

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