

PATENT SPECIFICATION (11)

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to electronic timepieces with digital displays. The main object of the invention is to provide improved electronic timepieces with digital displays having a chronograph function (i.e. which can be used to display elapsed time) as well as a normal time display, and which can display time units shorter than one second when required by actuating a change-over switching circuit. In conventional time pieces with this facility a figure which displays date in the normal display can be changed over to display tenths of a second. With such a time-piece, however, a figure which displays minutes in the normal display is changed over to display the seconds figure in the stop watch display and what is normally an hours display figure is changed over to serve as a minutes display. Accordingly the maximum stop watch time which can be displayed is 60 minutes. This is a disadvantage or limitation which it is the main object of the present invention to avoid.

35 According to this invention there is provided an electronic timepiece which is utilisable at will to display elapsed time or as a timekeeper to display time of day comprising time counting means for counting hours, minutes, seconds and parts of a second; digital time display means; first switch means, operable at will, for selectively utilising said display means for display of either time of day or of elapsed time in hours, minutes and seconds; and further switch means, operable as will and effective when said first switch means selects display of elapsed time to utilise said display means to display parts of a second of elapsed time.

50 Preferably said time counting means comprise 1/100 second counting means, 1/10 second counting means, seconds counting means

minute counting means and hours counting means and wherein said further switch means, in one setting thereof, cause driving signals to be transmitted for display from the seconds, minutes and hours counting means, and, in another setting thereof, cause driving signals to be transmitted for display from the 1/100 second and 1/10 second counting means. Preferably the display is of the liquid crystal multi-segment numeric type.

The invention is illustrated in the accompanying drawings in which Figure 1 is a diagram of one embodiment of Figures 2 (A) and (B) are face views of a wristwatch embodying the invention and shows the nature of the two alternative displays which the watch can provide.

Referring to Figure 1, a time standard quartz oscillator 1 (represented only by its crystal although of course it is a crystal controlled oscillator) feed its output into a divider 2. The oscillator is of such frequency and the division ratio is such that the output signals from 2 are 1/100 second signals. As shown the divider 2 divides by 100 so that the frequency of the oscillator 1 is 10 KHz. The 1/100 second signals from the divider 2 are counted by a counter 3 counting up to 10; a counter 4 counts the 1/10 second signal output from the counter 3 and counts up to 10; a counter 5 counts the one second signals from counter 4; a counter 6 counts the tens figure of the seconds; a counter 7 counts minutes signals from counter 6; counter 8 counters the tens figure of the minutes; counter 9 counts the hours; and counter 10 counts the tens figure of the hours. Transmission gates 13, 14, 15, 16, 17, 18, 20, 21 are provided controlled by a switch SW2 via an anti-chatter circuit in block 12. Block 11 represents reset, start and stop circuitry for use when the timepiece is operating as a stop watch. 19 is a decoder-driver, 22 is a decoder, 23 and 24 are AND gates and 26 is a driver.

The contents of counters 3 and 4 are applied to the transmission gates 13, 15 and 17 and those of counters 5 and 6 are applied to the transmission gates 14, 16 and 18.

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The output of gate 13 is connected to that of gate 14; the output of gate 15 is connected to that of gate 16; and the output of gate 17 is connected to that of gate 18, the outputs of the said gates 13 and 14, 15 and 16 and 17 and 18 being passed, as shown, to the decoder-driver 19. The transmission gates 13 to 18 thus select the contents of counters 3 and 4 or the contents of counters 5 and 6.

10 The driver 26 which is composed as indicated of AND gates 23, 24 and OR gates 25 operates as follows:—when the appropriate output of the decoder 22 is of LOW level, the output of the associated AND gate 23 becomes of LOW level, the associated AND gate 24 opens and a 32 Hz signal is applied by gate 24 to segment electrodes of the liquid crystal display through the associated OR gate 25. If, however, the said 32 Hz signal is also applied to the common electrode (not shown) of the liquid crystal display, the segments are not brought into operation—they come into operation (i.e. they light up) only when a 32 Hz signal is applied thereto.

25 Switch SW1 is a control switch which is closed to bring the stop watch function into use and which, when closed, applies *via* an anti-chatter circuit in block 12, a signal to the apparatus in block 11 to make the stop watch reset start and stop circuitry in that block ready for use. (This circuitry, with its customary switches, is not shown).
30 Block 11 has an output lead on which is produced, when reset is desired, an output which resets the counters 3, 4, 5, 6, 7, 8, 9 and 10 by applying a reset signal to their reset terminals R. A second output from 11 controls the supply of pulses from the divider 2 to the counter 3.

40 The output from counter 3 is fed to the transmission gates 13, 15, 17 and the output from the counter 5 is fed to the transmission gates 14, 16, 18. The outputs from the transmission gate pairs 13 and 14, 15 and 16, 17 and 18 are fed into the decoder driver 19.

45 A 32Hz driving pulse obtained from a quartz crystal oscillator (not shown) is fed to the transmission gate 20 and the same pulse, inverted, (it is represented in Figure

50 1 by 32Hz) is fed to the transmission gate 21. (The 32Hz pulse could be obtained from the oscillator 1 by frequency division). When gate 21 is closed and gate 20 open (as occurs when the switches SW1 and SW2 are closed) 32Hz pulses are passed to AND gates 23

55 through gate 20 instead of the 32Hz pulses which are supplied *via* gate 21 when this is open.

60 The output from counters 7, 8, 9, 10 are fed to the decoder 22 and the corresponding outputs thereof are fed directly to the

remaining inputs of the AND gates 23 and, through inverters as shown, to remaining inputs of the AND gates 24. The outputs from the pairs of AND gates 23 and 24 are fed as inputs to OR gates 25 the outputs from which are used to drive segments of liquid crystal multi-segment numeric display elements in a portion of the display (not shown). The outputs from the decoder driver 19 are used similarly to drive liquid crystal segments in another portion of the display.

70 The operation of Figure 1 will now be described.

75 When SW2 is open, LOW level (digital "0") is fed to the N channel terminals of the transmission gates 13, 15 and 17 and to the P channel terminals of the transmission gates 14, 16 and 18. Consequently, when said switch is open outputs from the counters 5 and 6 are fed to the decoder driver 19 and seconds are displayed by the portion of the display driven by the outputs from 19. So as not to complicate the drawing separate outputs (other than to counter 7) from counter 6 are not shown but they are fed to the decoder driver through transmission gates in the manner already described for counter 5.

80 At this time, the inverted 32Hz pulse is fed to the AND gates 23 and the 32Hz pulse is fed to the AND gates 24. If an output from the decoder 22 is at HIGH level (digital "1") the corresponding AND

85 circuit 23 conducts and the 32Hz pulse is passed by said gate 23. The corresponding AND circuit 24 will have a LOW level output since LOW level, (the level to which the corresponding HIGH level output from the decoder 22 is inverted) is fed to it. An

90 inverted 32Hz pulse is thus produced at the output of the OR circuit 25 and the appropriate liquid crystal segment is energised. Thus, assuming switch SW1 to have been closed to give stop watch operation, switch SW2 is open, a normal stop watch display is obtained, seconds of stop watch time being displayed by the parts of the display driven by decoder-driver 19 and minutes and hours of stop watch time being displayed by the parts of the display driven by the outputs of OR gates 25.

95 However, (assuming switch SW1 is still closed) if switch SW2 is closed, the transmission gates 13, 15 and 17 conduct the transmission gates 14, 16 and 18 are blocked and the decoder-driver 19 is fed with the output of the counters 3 and 4. Accordingly, when SW2 is closed, a 1/100 second figure is displayed where a seconds figure is normally displayed and a 1/10 second figure is displayed where a tens of seconds is normally displayed, in other words what was 130

a display of seconds has become a display of 1/1000 seconds. At this time, the transmission gate 20 conducts in reverse and gate 21 is closed. The 32Hz pulse is accordingly fed to AND circuits 23 and to the AND circuits 24 as well. Therefore whether an output from the decoder 22 is HIGH level or LOW level, a 32Hz pulse is always produced from the OR gate 25. Although this is not shown in the drawing the 32Hz pulse is, of course, always applied to the common electrode of the liquid crystal display so there is no effective voltage drive to any of the parts of the display connected to the OR gates 25 and therefore these parts do not give any display.

Figure 2A shows the type of displays given by the watch when the switch SW1 is open—i.e. it is a normal hours, minutes and seconds time-keeping display—or when the switch SW1 is closed but switch SW2 is open, and the display is hours, minutes and seconds of stop watch time. Figure 2B shows the type of display given when (switch SW1 being closed) switch SW2 is closed, the display being then of hundredths of a second only. Thus, by leaving switch SW1 closed, any stop watch time can be read in hours, minutes and seconds and, whenever it is desired to do so, additionally hundredths of a second and tenths of a second can be ready by closing switch SW2.

Attention is directed to the claims of our Patent No. 1,355,161 which describes and claims related subject matter.

WHAT WE CLAIM IS:—

1. An electronic timepiece which is

utilisable at will as a chronograph to display elapsed time or as a timekeeper to display time of day comprising time counting means for counting hours, minutes, seconds and parts of a second; digital time display means; first switch means, operable at will, for selectively utilising said display means for display of either time of day or of elapsed time in hours, minutes and seconds; and further switch means operable at will and effective when said first switch means selects display of elapsed time, to utilise said display means to display parts of a second of elapsed time.

2. A timepiece as claimed in claim 1 wherein said time counting means comprise 1/100 second counting means, 1/10 second counting means, seconds counting means, minute counting means and hours counting means and wherein said further switch means, in one setting thereof, cause driving signals to be transmitted for display from the seconds, minutes and hours counting means and, in another setting thereof, cause driving signals to be transmitted for display from the 1/100 second and 1/10 second counting means.

3. A timepiece as claimed in claim 1 or 2 wherein the display is of the liquid crystal multi-segment numeric type.

4. Timepieces substantially as herein described with reference to the accompanying drawings.

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Figure 2A shows the type of displays given by the watch when the switch SW1 is open—i.e. it is a normal hours, minutes and seconds time-keeping display—or when the switch SW1 is closed but switch SW2 is open, and the display is hours, minutes and seconds of stop watch time. Figure 2B shows the type of display given when (switch SW1 being closed) switch SW2 is closed, the display being then of hundredths of a second only. Thus, by leaving switch SW1 closed, any stop watch time can be read in hours, minutes and seconds and, whenever it is desired to do so, additionally hundredths of a second and tenths of a second can be ready by closing switch SW2.

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