CLAIMS

What is claimed is

1. A method to fabricate semiconductor devices with die sizes larger than 900mm^2, the method comprising:

providing a first type of source wafers that contain high-resolution circuit elements partitioned into a multitude of pre-fabricated blocks (PFBs), wherein each PFB is at most 900mm^2 in size;

providing a second type of source wafers that contain lower-resolution circuit elements partitioned into a multitude of PFBs, wherein each PFB is at most 1500mm^2 in size;

assembling PFBs from the first type of source wafers onto a product substrate, followed by assembling PFBs from the second type of source wafers onto previously assembled PFBs, wherein the fully-assembled group of high-resolution and low-resolution PFBs is equivalent in function to a monolithically constructed SoC but arbitrarily larger in size than 900mm^2.

2. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

3. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

4. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

5. The method of claim 1, wherein the first type of source wafers or the second type of source wafers have multiple kinds of PFBs.

6. The method of claim 1, wherein the PFBs are less than 10um thick.

7. The method of claim 1, wherein the PFBs are less than 1um thick.

8. The method of claim 1, wherein the PFBs are less than 100nm thick.

9. The method of claim 1, wherein the low-resolution PFBs contain custom-metal dies (CMDs) that include only metal layers.

10. The method of claim 1, wherein a superstrate assembly is used to pick-and-place PFBs and wherein the superstrate assembly has one or more, connected or unconnected, sub-superstrates.

11. The method of claim 10, further comprising controlling, using an overlay control architecture, distortions in PFBs to nanometer scales.

12. The method of claim 10, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

13. The method of claim 10, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

14. The method of claim 1, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive;

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

15. The method of claim 1, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the first type of source wafers and the second type of source wafers.

16. The method of claim 15, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.

17. A method to ensure hardware security during fabrication of semiconductor devices, the method comprising:

providing a first type of source wafers that contain high-resolution circuit elements partitioned into a multitude of pre-fabricated blocks (PFBs), wherein the first type of source wafers can be fabricated at one or more, trusted or untrusted facilities;

providing a second type of source wafers that contain lower-resolution circuit elements partitioned into a multitude of PFBs, wherein the second type of source wafers can be fabricated at one or more, trusted or untrusted facilities; and

assembling PFBs from source wafers of the first type on to a product substrate, followed by assembling PFBs from source wafers of the second type onto previously assembled PFBs, wherein the fully-assembled group of high-resolution and low-resolution PFBs is equivalent in function to a monolithically constructed SoC, wherein the assembly is performed at a trusted facility.

18. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

19. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

20. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

21. The method of claim 17, wherein a source wafer has multiple kinds of PFBs.

22. The method of claim 17, wherein the PFBs are less than 10um thick.

23. The method of claim 17, wherein, the PFBs are less than 1um thick.

24. The method of claim 17, wherein the PFBs are less than 100nm thick.

25. The method of claim 17, wherein the low-resolution PFBs contain only custom-metal dies (CMDs) having only metal layers.

26. The method of claim 17, wherein a superstrate assembly is used to pick-and-place PFBs, wherein superstrate assembly has one or more, connected or unconnected, sub-superstrates.

27. The method of claim 26, wherein an overlay control architecture is used to control distortions in PFBs to nanometer scales.

28. The method of claim 26, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

29. The method of claim 26, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

30. The method of claim 17, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive; and

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

31. The method of claim 17, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the first type of source wafers and the second type of source wafers.

32. The method of claim 31, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.

~~33. A method to fabricate a semiconductor device, the method comprising:~~

~~providing a source wafer having a grid of prefabricated blocks (PFB), wherein the source wafer has a sacrificial layer that can be etched off to relieve the PFBs from the bulk of the wafer;~~

~~applying a tether etch to create tethers underneath the PFBs;~~

~~applying an etchant to dissolve the tether releasing the PFBs on the source wafer to a PFB chuck;~~

~~individually picking one or more of the PFBs from the PFB chuck;~~

placing one or more of the PFBs on a product wafer using nano-precision alignment techniques; and

bonding the PFBs to the product wafer.

34. The method of claim 33, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

35. The method of claim 33, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

36. The method of claim 33, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

37. The method of claim 33, wherein a source wafer has multiple kinds of PFBs.

38. The method of claim 33, wherein the PFBs are less than 10um thick.

39. The method of claim 33, wherein the PFBs are less than 1um thick.

40. The method of claim 33, wherein the PFBs are less than 100nm thick.

41. The method of claim 33, wherein the low-resolution PFBs contain only metal layers, and are referred to as custom-metal dies (CMDs).

42. The method of claim 33, wherein a superstrate assembly is used to pick-and-place PFBs, wherein superstrate assembly has one or more, connected or unconnected, sub-superstrates.

43. The method of claim 42, wherein an overlay control architecture is used to control distortions in PFBs to nanometer scales.

44. The method of claim 42, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

45. The method of claim 42, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

46. The method of claim 33, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive;

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

47. The method of claim 33, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the source wafer.

48. The method of claim 47, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.

49. A method to fabricate a semiconductor device, the method comprising:

providing a source wafer having a grid of prefabricated blocks (PFB),

wherein the source wafer has a sacrificial layer that can be etched off to relieve the PFBs from the bulk of the wafer, and

wherein the source wafer with the sacrificial layers is constructed from a substrate with two or more layers of differing doping levels and/or types, grown using an epitaxial growth process;

applying a tether etch to create tethers underneath the PFBs;

applying an etchant to dissolve the tether releasing the PFBs on the source wafer to a PFB chuck;

individually picking one or more of the PFBs from the PFB chuck;

placing one or more of the PFBs on a product wafer using nano-precision alignment techniques; and

bonding the PFBs to the product wafer.

50. The method of claim 49, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

51. The method of claim 49, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

52. The method of claim 49, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

53. The method of claim 49, wherein a source wafer has multiple kinds of PFBs.

54. The method of claim 49, wherein the PFBs are less than 10um thick.

55. The method of claim 49, wherein the PFBs are less than 1um thick.

56. The method of claim 49, wherein the PFBs are less than 100nm thick.

57. The method of claim 49, wherein the low-resolution PFBs contain only metal layers, and are referred to as custom-metal dies (CMDs).

58. The method of claim 49, wherein a superstrate assembly is used to pick-and-place PFBs, wherein superstrate assembly has one or more, connected or unconnected, sub-superstrates.

59. The method of claim 58, wherein an overlay control architecture is used to control distortions in PFBs to nanometer scales.

60. The method of claim 58, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

61. The method of claim 58, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

62. The method of claim 49, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive;

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

63. The method of claim 49, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the source.

64. The method of claim 63, further comprising inferring the goodness of an entire PFB by testing select portions of the PFBs, and extrapolating using statistical models.

65. A method to fabricate a semiconductor device, the method comprising:

providing a source wafer having a grid of prefabricated blocks (PFB), wherein the source wafer does not have a sacrificial layer;

applying a porosity creation process, along with a porosity repelling field, to create a buried sacrificial layer in the source wafer;

applying a tether etch to create tethers in the buried sacrificial layer underneath the PFBs;

applying an etchant to dissolve the tethers releasing the PFBs on the source wafer to a PFB chuck;

individually picking one or more of the PFBs from the PFB chuck;

placing one or more of the PFBs on a product wafer using nano-precision alignment techniques; and

bonding the PFBs to the product wafer.

66. The method of claim 65, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

67. The method of claim 65, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

68. The method of claim 65, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

69. The method of claim 65, wherein a source wafer has multiple kinds of PFBs.

70. The method of claim 65, wherein the PFBs are less than 10um thick.

71. The method of claim 65, wherein the PFBs are less than 1um thick.

72. The method of claim 65, wherein the PFBs are less than 100nm thick.

73. The method of claim 65, wherein the low-resolution PFBs contain only metal layers, and are referred to as custom-metal dies (CMDs).

74. The method of claim 65, wherein a superstrate assembly is used to pick-and-place PFBs, wherein superstrate assembly has one or more, connected or unconnected, sub-superstrates.

75. The method of claim 74, further comprising controlling, using an overlay control architecture, distortions in PFBs to nanometer scales.

76. The method of claim 74, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

77. The method of claim 74, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

78. The method of claim 65, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive;

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

79. The method of claim 65, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the source.

80. The method of claim 79, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.

81. A method to fabricate a semiconductor device, the method comprising:

providing a first set of source wafers having a grid of prefabricated blocks (PFB);

providing a second set of source wafers each having a grid of custom metal dies (CMDs);

assembling CMDs from the second set on top of the PFBs from the first set of source wafers, wherein the first set of source wafers function as product wafers.

82. A system to fabricate a semiconductor device, the system comprising:

an etch chamber;

a nano-precise pick-and-place assembly unit;

a storage unit having stored therein a plurality of source and product wafers, wherein the plurality of source wafers includes a source wafer of a first type and a second type, each having different pre-fabricated blocks;

a transfer arm to:

transfer one or more of the source wafers to the etch chamber which applies a tether etch; and

transfer, upon completion of the tether etch, the one or more source wafers from the etch chamber to the nano-precise pick-and-place assembly unit; and

wherein the nano-precise pick-and-place assembly unit assembles pre-fabricated blocks (PFBs) from the one or more source wafers to a product substrate.

83. The system of claim 82, wherein the system is part of a mini-fab.

84. The system of claim 83, wherein the mini-fab further comprises:

one or more testing units to test known good dies in the plurality of source wafers;

one or more chemical mechanical polishing (CMP) units to polish the top of the plurality of source wafer.

85. A method to fabricate a semiconductor device, the method comprising:

providing one or more source wafers which contain a grid of pre-fabricated blocks (PFB); and

assembling the PFBs on to a product wafer in two or more layers, wherein PFBs in the second, third or subsequent layers contain solely metal structures.

86. A method to design a 3D SoC, the method comprising:

floorplanning of macro cells and logic standard cells;

partitioning and placing the logic standard cells in multiple tiers using a backend EDA design methodology that utilizes mixed-integer programming (MIP) techniques,

wherein the objective is to minimize the total edge cost for all the nets, including 2D and 3D, under a set of constraints,

wherein the total edge cost of a net is determined by considering timing profile weight of a net, clock frequency, stages in timing path, slack profile, fanout of source and driver cell, delay per micron, MIV parasitics, MIV dimensions, routing blockage impact of neighboring cells, self-routing blockage impact, capacitance, and distance among tiers;

wherein the set of constraints includes the placement of cells in a non-overlapping manner in each tier, placement blockages of MIVs for power delivery network, and area balancing to ensure placement density of any tier doesn't exceed a threshold value;

generating a clock tree synthesis of the macro cells and the logic standard cells;

routing between different circuit elements; and

timing and physical signoff of different circuit elements or blocks.