

-1-

A PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES

FIELD OF THE INVENTION

This invention relates to the field of semiconductor packaging technologies. More specifically, the invention relates to packages which incorporate two or more semiconductor dies in a single enclosure.

BACKGROUND OF THE INVENTION

Electronic circuits integrated on a semiconductor substrate are commonly housed within packages suited to the particular integrated circuit (IC) device. A typical semiconductor package comprises a leadframe which interconnects the IC to external circuitry located on a printed circuit board. A standard leadframe is larger than the size of the integrated circuit die so that bonding pad regions on the die can be wire-bonded to extensions or "fingers" of the leadframe. After the IC on the die has been wire-bonded to the leadframe, the assembly is normally encapsulated in plastic or some other type of packaging material. Terminals connected to the leadframe fingers extend outside the packaging material to provide points of interconnection to other electronic components.

A continuing goal of the semiconductor industry is to maximize circuit density. One past scheme for increasing circuit density has been to house multiple semiconductor die in a single package. By way of example, multi-chip semiconductor packages are disclosed in U.S. Patent Nos. 5,012,323 and 5,019,893. The problem with prior art multi-chip packages, however, is that they either require the use of a specially-adapted custom package, or they impose size restrictions on the semiconductor dies that may be housed together. In addition, conventional dual die semiconductor packages often mandate a custom bonding pad routing for the ICs so that interconnection can be made to a single leadframe. Thus, past efforts have often resulted in costly package designs limited in use to specific die sizes or particular bonding pad configurations.

-2-

Another drawback associated with traditional multi-die packages is that many designs fail to address the problem of insuring adequate data and code security. Because modern semiconductor devices represent a tremendous investment of time, money, and human effort, there is a heightened concern among manufacturers to find new ways of preventing access to critical or sensitive functional portions of the integrated circuitry. This concern has lead to an increased demand for semiconductor packages which include adequate protection mechanisms against outside intrusion.

For example, today many designers wish they could integrate a microprocessor or controller (or some other function) with additional non-volatile flash memory (e.g., 8 MBytes) in a single package offering security protection. A typical application might have the flash memory storing highly proprietary code that is accessed or executed by the controlling processor. For obvious reasons, such code must be kept secret. In this type of system, it is desirable to have code or programs only be addressed through the microprocessor or controller. The problem with previous packaging technologies has been the inability to prohibit access to information stored in on or both of the semiconductor devices from outside intruders.

Therefore what is needed is a semiconductor package which increases circuit density by housing multiple semiconductor die in a single leadframe package while overcoming the drawbacks of the prior art. Furthermore, the package should render functionality important circuitry inaccessible to outside intruders, and critical algorithms, code, or programs should remain hidden from interloping copiers or competitors.

As will be seen, the present invention is a multi-die semiconductor package that allows a wide variety of existing semiconductor chips to be integrated on the same leadframe with relatively little change to the standard packaging process flow. The invention also obviates changes to the bond pad routing of the ICs. Performance is enhanced by providing greater package density at a lower manufacturing cost. The invented multiple semiconductor die

-3-

package also permits implementation of powerful encryption/decryption systems to prevent interrogation of hidden integrated circuit functions.

SUMMARY OF THE INVENTION

The present invention is a package housing two or more semiconductor die. The invented package greatly increases IC density and is capable of accommodating a variety of different sizes of semiconductor die.

In one embodiment, the semiconductor package of the present invention comprises a leadframe which includes a rectangular paddle and a number of lead fingers extending near to the paddle. A flexible (or "flex") circuit is adhesively attached to both sides of the paddle. A first semiconductor die is then bonded to the bottom surface of the paddle and wire-bonded to the flexible circuit. The leadframe is then turned over and the operation repeated with a second semiconductor die being attached to the opposite or top surface of the paddle. Wires are used to electrically connect the integrated circuits on the first and second semiconductor die to the flexible circuit and to the lead fingers of the leadframe. In each case, the semiconductor dies are attached with their back sides mounted on the flex circuit against opposing surfaces of the paddle. In other embodiments, the semiconductor dies may be mounted face down; that is, with the integrated circuit mounted against and facing the flex circuit.

Finally, the leadframe is either encapsulated in plastic or another suitable material. A polymer security coating may be dispensed and cured to cover the semiconductor dies prior to encapsulation in the casing material.

Special advantages are achieved by the present invention in applications where the upper chip comprises a processor or controller device and the lower chip comprises a memory (e.g., a flash memory). In such cases, the invented package permits the implementation of an encryption/decryption scheme with the versatility of the controller coupled to the maximum density of a large flash memory array while preventing interrogation of hidden functions. Programs, code, or

-4-

algorithms for encrypting data may be stored on the lower memory chip and addressed solely through the controlling upper semiconductor chip. Such a system prohibits direct memory access to the lower chip and provides a powerful data security system in a compact single leadframe package.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description which follows and from the accompanying drawings, which however, should not be taken to limit the invention to the specific embodiments shown, but are for explanation and understanding only.

Figure 1 is a sectional perspective view of one embodiment of the semiconductor package of the present invention.

Figure 2 is a cross-sectional side view of the embodiment illustrated in Figure 1.

Figure 3 is a cross-sectional side view of another embodiment of the present invention.

Figure 4 is a cross-sectional side view of yet another embodiment of the present invention.

Figure 5 is a cross-sectional side view of still another embodiment of the present invention.

DETAILED DESCRIPTION

In the following description, a package housing multiple semiconductor die is set forth in specific detail in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details may not be needed to practice the present invention. In other instances, well-known

-5-

methods, materials, processing techniques, etc., are not described in detail in order to avoid unnecessarily obscuring the present invention.

Referring now to Figure 1, there is shown a sectional perspective view of one embodiment of the multiple semiconductor die package of the present invention. The package comprises a leadframe which includes a die-mounting paddle 20 and a plurality of lead fingers 21 extending near to, but not contacting, paddle 20. The leadframe is fabricated in the standard manner according to conventional packaging technology wherein the die paddle 20 is a rectangular platform located in the center of the leadframe and held in place at one or more points. In the embodiment of Figure 1 paddle 20 and lead fingers 21 are located in the same general plane and are fabricated from the same material.

With continuing reference to Figure 1, a first semiconductor die 22 is shown comprising an essentially wafer-thin rectangular solid having an upper surface 23 on which is constructed an integrated circuit. The bottom or back surface 24 of die 22 is mounted on a flexible interconnect circuit 27. As can be seen, paddle 20 is larger than flexible circuit 27 and semiconductor die 22.

In accordance with one embodiment of the invention, flexible ("flex") circuit 27 is adhesively attached to the upper and lower primary surfaces of paddle 20. By way of example, flex circuit 27 is normally bonded to the upper primary surface with an adhesive glue, wrapped around the side of the paddle, and then adhesively bonded to the lower primary surface of paddle 20. It is appreciated that the upper and lower primary surfaces of the paddle are essentially parallel to one another and perpendicular to the side surfaces.

Flex circuit 27 may be bonded to paddle 20 using a variety of methods. For instance, flex circuit 27 may be manufactured with an adhesive backing to allow straightforward attachment to the paddle surfaces. Alternatively, flex circuit 27 may be bonded utilizing conventional adhesives. A polyimide adhesive may be utilized to tightly hold flexible circuit 27 against the surfaces of paddle 20 to prevent formation of air bubbles between paddle 20 and the flex circuit 27.

-6-

Flex circuit 27 is made up of a plurality of interconnects connected to sets of bonding pads 28. Figure 1 illustrates a set of bonding pads 28 being arranged about flex circuit 27 so as to define a die-mounting area for semiconductor die 22 over the upper surface of paddle 20. Likewise, another set of bonding pads 28 are disposed to provide a second die-mounting area for a second semiconductor die mounted over the lower surface of paddle 20 (see Figure 2).

All of the interconnect lines of flex circuit 27 may be embedded in a flexible insulating material that extends over the side of paddle 20 to provide electrical interconnection between the first set of bonding pads 28 located on the upper surface of paddle 20 and the second set of bonding pads 28 located on the bottom surface of paddle 20. Typically, flex circuit 27 is on the order of 1.5 thousandths of an inch thick, and easily fits in the space separating lead fingers 21 from one side of paddle 20.

Semiconductor die 22 has a front surface on which is constructed integrated circuitry that includes a plurality of input/output (I/O) bond pads 25, usually distributed around the periphery of the die. In accordance with one embodiment, extremely fine wires 31, typically comprising gold or aluminum, are utilized to electrically connect I/O bond pads 25 with bonding pads 28 and/or lead fingers 21.

Figure 2 illustrates a cross-sectional side view of the package of Figure 1 taken across cut lines 30 - 30'. As can be seen, Figure 2 shows semiconductor die 22 mounted on flex circuit 27 against the upper surface of paddle 20. Flex circuit 27 is wrapped around a side 35 of paddle 20 and includes a second set of bonding pads 28 that define another die-mounting area for a second semiconductor die 23. Semiconductor die 23 is mounted against the lower primary surface of paddle 20.

Instead of mounting the semiconductor dies 22 and 23 to the flex circuit insulation material, an alternative is to have the die-mounting areas removed from flex circuit 27 so that openings are defined large enough to fit the associated die. Such an embodiment is shown in Figure 5 in which the semiconductor dies 22 and 23 are mounted

-7-

directly against paddle 20 within openings 29. Flex circuit 27 is still laminated to paddle 20, but because the material of the flex circuit no longer insulates the die from the paddle there is better thermal conduction. Hence, this alternative is well-suited for ICs having high power dissipation.

In the embodiment of Figure 2, integrated circuitry is constructed on the outward face of semiconductor dies 22 and 23. Each die has a back that is devoid of circuitry. In accordance with the present invention, the back of semiconductor dies 22 and 23 is mounted against flex circuit 27, which is laminated to the upper and lower primary surfaces of paddle 20, respectively. In other words, the integrated circuitry fabricated on the faces of semiconductor dies 22 and 23 is exposed to permit wire-bonding. Connections are made from various I/O bond pads 25 of the respective die to bonding pads 28 on flex circuit 27 via wires 31. It should be understood that an assortment of wire-bonding techniques may be employed during the manufacturing process in accordance with the present invention.

In an alternative embodiment, one or both of the dies may be mounted face down against the flex circuit using the well-know "flip-chip" mounting technique. By way of example, Figure 4 illustrates a configuration in which dies 22 and 23 are mounted face-down against flex circuit 27 in a "flip-chip" manner. Flip-chip mounting involves forming solder bumps 41 on the bond pads 25 of the integrated circuitry. Flex circuit 27 is manufactured such that when the die is placed face-down against the flex circuit substrate, solder bumps 41 align to corresponding bonding pads 28 (or similar metal connection points) of the flex circuit. The respective faces of dies 22 and 23 thereby adjoin the sections of the flex circuit laminated to the upper and lower surfaces of paddle 20.

Thus, flip-chip mounting obviates wire bonding to connect the integrated circuitry to the flex circuit. Of course, wires 31 are still needed to interconnect flex circuit 27 (e.g., via additional bonding pads 28) to lead fingers 21 of the frame.

-8-

With reference again to Figure 2, an exemplary process useful for the manufacture of the package shown in that embodiment may include the following steps. First, once flex circuit 27 has been adhesively attached to paddle 20 the backside die (semiconductor die 23) is bonded to the lower surface of paddle 20 on a die-mounting area of flex circuit 27. Die 23 may be mounted using ordinary epoxy adhesive. Next, wires 31 are bonded to I/O pads 25 of the integrated circuit constructed on die 23 and to corresponding bonding pads 28 on flex circuit 27. The configuration of bonding pads 28 on flex circuit 27 is originally adapted for the particular semiconductor die.

An implementation of the invented semiconductor package in an encrypted system would maximize the number of connections between semiconductor dies 22 and 23 and minimize the number of connections from die 22 to lead fingers 21. For example, sensitive address and data line connections between dies 22 and 23 would be made via wire bonds from bonding pads 25 to bonding pads 28, but not also to fingers 21. Wire connections from pads 25 to pads 28 and lead fingers 21 for die 22 would be limited to power supply lines and basic I/O signals.

Designing an interconnect routing between sets of pads 28 is a relatively simple and low-cost operation as compared to prior art methods which normally involved defining locations and routing patterns for I/O bond pads 25 of the integrated circuit. One of the advantageous features of the present invention is that no changes need be made to the IC fabricated on the die -- the only essential requirement is that bonding pads 28 of flex circuit 27 be distributed beyond the edges of die 23 so as to provide a sufficient die-mounting area. Furthermore, note that no wires 31 are used to interconnect semiconductor die 23 with lead fingers 21. In other words, semiconductor die 23 is only interconnected to flex circuit 27. This aspect of the present invention advantageously makes it possible to implement a data security scheme.

After die 23 has been mounted and wire-bonded to flex circuit 27, the leadframe may be flipped over and the same process repeated with respect to semiconductor die 22. The only difference in the operations

-9-

is that wires 31 are used to bond the integrated circuit of die 22 to both the flex circuit 27 and to lead fingers 21. By way of example, some of bond pads 25 on die 22 may only be connected to lead fingers 21, others only to pads 28 on flex circuit 27, and still others to both pads 28 and fingers 21. Once all wire bonding has been completed, the semiconductor die, paddle, and lead fingers are encased in a packaging material 50, which typically comprises plastic. The processing steps employed for encasing the components are well known and standard in the packaging industry.

To provide maximum protection against intrusion, a security coating 40 is applied to cover both of the semiconductor dies prior to the encasing procedure. This aspect of the invention is shown in Figure 2 wherein security coating 40 is a conformal coating of a material that encapsulates the die to prevent physical tampering of the integrated circuitry. In one embodiment, a polymer encapsulate is used as security coating 40. Ideally, the material used should be impervious to visual light, or to other forms of penetrating radiation, e.g., X-rays. The purpose of security coating 40 is to provide physical protection to the integrated circuitry housed within the package. Therefore, any material utilized as a security coating 40 should have properties which include adhesion to the surface of the semiconductor die such that any attempts to penetrate coating 40 result in substantial destruction of the integrated circuitry constructed therein.

As discussed earlier, the present invention provides an excellent package for implementing an encryption/decryption system. The invented package is also ideally-suited for integrating two or more die having complementary functions in the same leadframe. As an example, semiconductor die 22 of Figure 2 may comprise a microprocessor or microcontroller device with semiconductor die 23 comprising a non-volatile flash memory. Because semiconductor die 23 is bonded only to pads 28 of flex circuit 27, it may only be accessed through the integrated circuitry of semiconductor die 22. This permits a great deal of flexibility in devising encryption/decryption techniques which can make it virtually impossible for an intruder to access data,

-10-

programs, code, or algorithms stored on semiconductor die 23. Moreover, the back-to-back relationship of semiconductor dies 22 and 23, coupled with the use of security coating 40, makes it extremely difficult for a would-be copier to physically penetrate the package for the purpose of probing either of the semiconductor die. Thus, the present invention is well-suited for special applications which require maximum data security. Furthermore, the invention is easily adapted for use with many different semiconductor devices and package types since the flex circuit 27 need only be changed to accommodate different components or die.

With reference now to Figure 3, there is shown a cross-sectional view of another embodiment of the multi-die package of the present invention. In Figure 3, a single semiconductor die 22 is mounted against the portion of flex circuit 27 that is laminated to the upper primary surface of paddle 20. Two semiconductor dies 23 and 33 are shown mounted against the portion of flex circuit 27 that is laminated to the lower primary surface of paddle 20. The flex circuit bonding, die-mounting, and wire-bonding operations for the embodiment of Figure 3 are the same as described in conjunction with Figures 1 and 2.

Practitioners in the art will appreciate the only limitation on the number of chips that may be housed within a single package in accordance with the present invention is that the paddle 20 must be large enough to accommodate each of the individual die. In the case where more than two semiconductor die are mounted against paddle 20, flex circuit 27 needs to have sets of bonding pads 28 arranged so as to define separate die-mounting areas for the respective die. It is worth noting that there is no strict limit on the relative sizes of the semiconductor dies; that is, semiconductor die 22 may be larger than or smaller than semiconductor die 23 (Figure 2), and semiconductor die 22 may be larger than or smaller than the combination of semiconductor dies 23 and 33 (Figure 3).

Whereas many alterations and modifications to the present invention will no doubt become apparent to the person of ordinary skill in the art after having read the foregoing description, it is to be

-11-

understood that the particular embodiments shown and described by way of illustration are in no way intended to be limiting. Therefore, reference to the details of the illustrated diagrams is not intended to limit the scope of the claims which themselves recite only those features regarded as essential to the invention.



-12-

CLAIMS

I claim:

1. A semiconductor package comprising:
 - a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;
 - a plurality of interconnects bonded to the first and second primary surfaces of the paddle, the interconnects having a first set of bonding areas disposed on the first primary surface and a second set of bonding areas disposed on the second primary surface of the paddle;
 - first and second semiconductor dies each having a face with integrated circuitry constructed thereon and a back, the back of the first semiconductor die being bonded against the first primary surface, and the back of the second semiconductor die being bonded against the second primary surface of the paddle;
 - a first set of wires electrically connecting the integrated circuitry of the first semiconductor die to the first set of bonding areas;
 - a second set of wires electrically connecting the integrated circuitry of the second semiconductor die to the second set of bonding areas, thereby coupling together the integrated circuitry of the first and second semiconductor dies;
 - a third set of wires electrically coupling the integrated circuitry of the first semiconductor die to the lead fingers; and
 - a casing which encloses the semiconductor dies.
2. The semiconductor package of claim 1 further comprising a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.
3. The semiconductor package of claim 2 wherein the material is characteristically impervious to light.

REPLACED SHEETS SG

- ☐ Description : paged to paged
- ☒ Claim(s) : paged ...13... to paged ...21...
- ☐ Drawing(s) : paged to paged
- ☐ Abstract : paged to paged





-13-

4. The semiconductor package of claim 1 wherein the casing comprises a plastic.

5. The semiconductor package of claim 1 wherein the casing comprises a ceramic.

6. The semiconductor package of claim 1 wherein the paddle and the first and second semiconductor dies each have a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions of either the first or second semiconductor dies.

7. The semiconductor package of claim 6 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.

8. The semiconductor package of claim 6 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

9. The semiconductor package of claims 2, 3, 4, 5, 6, 7 or 8 wherein the plurality of interconnects comprises a flexible circuit laminated to the first and second primary surfaces and wrapped around the side of the paddle.

10. A semiconductor package comprising:
a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;
a substrate having a plurality of interconnects embedded therein, a first section of the substrate being bonded to the first primary surface of the paddle, and a second section of the substrate being bonded to the second primary surface of the paddle;





-14-

first and second semiconductor dies each having a back, and a face with integrated circuitry constructed thereon, the integrated circuitry on the face of the first semiconductor die being connected to a plurality of conductive bumps mounted to the first section of the substrate wherein the bumps provide electrical connection between the integrated circuitry of the first semiconductor die and the plurality of interconnects; the back of the second semiconductor die being mounted to the second section of the substrate;

a first set of wires electrically connecting the plurality of interconnects to the lead fingers;

a casing which encloses the first and second semiconductor dies and the first and second sets of wires.

11. The semiconductor package of claim 10 further comprising a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the first and second semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

12. The semiconductor package of claim 11 wherein the material is characteristically impervious to light.

13. The semiconductor package of claim 10 wherein the casing comprises a plastic.

14. The semiconductor package of claim 10 wherein the casing comprises a ceramic.

15. The semiconductor package of claim 10 wherein the paddle and the first and second semiconductor dies each have a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions of either the first or second semiconductor dies.





-15-

16. The semiconductor package of claim 15 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.

17. The semiconductor package of claim 15 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

18. A semiconductor package comprising:
a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;
a substrate having a plurality of interconnects embedded therein, a first section of the substrate being bonded to the first primary surface of the paddle, and a second section of the substrate being bonded to the second primary surface of the paddle;
first and second semiconductor dies each having a back, and a face with integrated circuitry constructed thereon, the integrated circuitry on the face of the first semiconductor die being connected to a plurality of first conductive bumps mounted to the first section of the substrate wherein the first bumps provide electrical connection between the integrated circuitry of the first semiconductor die and the plurality of interconnects, the integrated circuitry on the face of the second semiconductor die being connected to a plurality of second conductive bumps mounted to the second section of the substrate wherein the second bumps provide electrical connection between the integrated circuitry of the second semiconductor die and the plurality of interconnects;
a set of wires electrically connecting a portion of the plurality of interconnects to the lead fingers; and
a casing which encloses the first and second semiconductor dies and the set of wires.





-16-

19. The semiconductor package of claim 18 further comprising a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the first and second semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

20. The semiconductor package of claim 19 wherein the material is characteristically impervious to light.

21. The semiconductor package of claim 18 wherein the casing comprises a plastic.

22. The semiconductor package of claim 18 wherein the casing comprises a ceramic.

23. The semiconductor package of claim 18 wherein the paddle and the first and second semiconductor dies each have a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions of either the first or second semiconductor dies.

24. The semiconductor package of claim 23 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.

25. The semiconductor package of claim 23 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

26. A semiconductor package comprising:
a leadframe which includes a paddle having first and second substantially parallel primary surfaces and a side, the first and second primary surfaces being substantially perpendicular to the side, the





-17-

leadframe also including a plurality of lead fingers disposed in the same general plane as the first and second primary surfaces of the paddle, the lead fingers extending near to, but not contacting, the paddle, with a portion of the lead fingers being separated from the side of the paddle by a determined distance;

a flexible circuit comprising a plurality of conductive lines interconnecting distinct sets of bonding pads, the flexible circuit being bonded to the first and second primary surfaces and wrapped over the side of the paddle such that a first set of bonding pads provide a first die-mounting area against the first primary surface, and a second set of bonding pads provide a second die-mounting area against the second primary surface of the paddle;

first and second semiconductor dies each having a back and a face with integrated circuitry constructed thereon, the first semiconductor die being mounted to the first die-mounting area of the flexible circuit, and the second semiconductor die being mounted to the second die-mounting area of the flexible circuit;

first and second sets of interconnects electrically connecting the integrated circuitry of the first and second semiconductor dies to the first and second sets of bonding pads, respectively, thereby coupling together the integrated circuitry of the first and second semiconductor dies;

a set of wires electrically connecting the integrated circuitry of the first semiconductor die to the lead fingers; and

a casing which encapsulates the first and second semiconductor dies.

27. The semiconductor package of claim 26 wherein the first and second sets of interconnects each comprise solder bumps such that the faces of the first and second semiconductor dies adjoin the first and second die-mounting areas of the flexible circuit, respectively.

28. The semiconductor package of claim 27 wherein the plurality of conductive lines comprise copper.





-18-

29. The semiconductor package of claim 26 wherein the paddle is centrally-located within the package.

30. The semiconductor package of claim 26 wherein the flexible circuit further includes a third set of bonding pads providing a third die-mounting area on the second primary surface of the paddle, the package further comprising:

a third semiconductor die having a back and a face with integrated circuitry constructed thereon, the third semiconductor die being mounted to the third die-mounting area of the flexible circuit; and

a third set of interconnects electrically connecting the integrated circuitry of the third semiconductor die to the third set of bonding pads, thereby coupling the integrated circuitry of the third semiconductor die to either the first or second semiconductor dies, or to both the first and second semiconductor dies.

31. The semiconductor package of claim 30 wherein the back of the third semiconductor die is mounted to the third die-mounting area of the flexible circuit, and the third set of interconnects comprise wires coupling the integrated circuitry on the face of the third semiconductor die to the third set of bonding pads.

32. The semiconductor package of claim 30 wherein the third set of interconnects comprise solder bumps such that the face of the third semiconductor die adjoins the third die-mounting area of the flexible circuit.

33. The semiconductor package of claim 30 wherein the casing comprises a plastic.

34. The semiconductor package of claim 30 wherein the casing comprises a ceramic.





-19-

35. The semiconductor package of claims 26, 27, 28, 29, 30, 31, 32, 33 or 34 further comprising a coating which conformably covers the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the semiconductor dies such penetration of the material substantially destroys the integrated circuitry constructed thereon.

36. The semiconductor package of claim 35 wherein the material is characteristically impervious to light.

37. The semiconductor package of claim 26 wherein the integrated circuitry of the first semiconductor die comprises a microcontroller.

38. The semiconductor package of claim 37 wherein the integrated circuitry of the second semiconductor die comprises a memory device.

39. A method of packaging multiple semiconductor dies comprising the steps of:

(a) providing a leadframe having a paddle with first and second primary surfaces and a plurality of lead fingers which extend near to the paddle;

(b) bonding a flex circuit to the paddle such that a first portion of the flex circuit having a first set of bonding pads providing a first die-mounting area covers a first primary surface, and a second set of bonding pads providing a second die-mounting area covers the second primary surface, the first and second sets of bonding pads being electrically interconnected;

(c) mounting first and second semiconductor dies against the first and second die-mounting areas, respectively, the first and second semiconductor dies each having a back and a face with integrated circuitry constructed thereon;





-20-

- (d) coupling the integrated circuitry of the first and second semiconductor dies to the flex circuit and at least the integrated circuitry of the first semiconductor die to the lead fingers; and
- (e) encasing the first and second semiconductor dies.

40. The method of claim 39 wherein the backs of the first and second semiconductor dies are mounted against the first and second die-mounting areas, respectively, in step (c).

41. The method of claim 40 wherein step (d) comprises the steps of:

wire-bonding the integrated circuitry on the face of the first semiconductor die to the first set of bonding pads; and

wire-bonding the integrated circuitry on the face of the second semiconductor die to the second set of bonding pads.

42. The method of claim 39 further comprising the step, prior to step (e), of:

conformably coating the first and second semiconductor dies with a material that encapsulates the first and second semiconductor dies.

43. A semiconductor package comprising:

a lead frame which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surface;

first and second semiconductor dies each having a face with integrated circuitry constructed thereon and a back, the paddle and the first and second semiconductor dies each having a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions of either the first or second semiconductor dies;

means for mounting the first and second semiconductor dies against the first and second primary surfaces of the paddle, respectively;



-21-

means for interconnecting the integrated circuitry of the first and second semiconductor dies together, the interconnecting means being attached to the first and second primary surfaces of the paddle;

electrically coupling means for at least the first semiconductor die to the lead fingers;

means for encasing the semiconductor dies.

44. The semiconductor package of claim 43 wherein the backs of the first and second semiconductor dies are mounted against the first and second primary surfaces, respectively.

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1/4

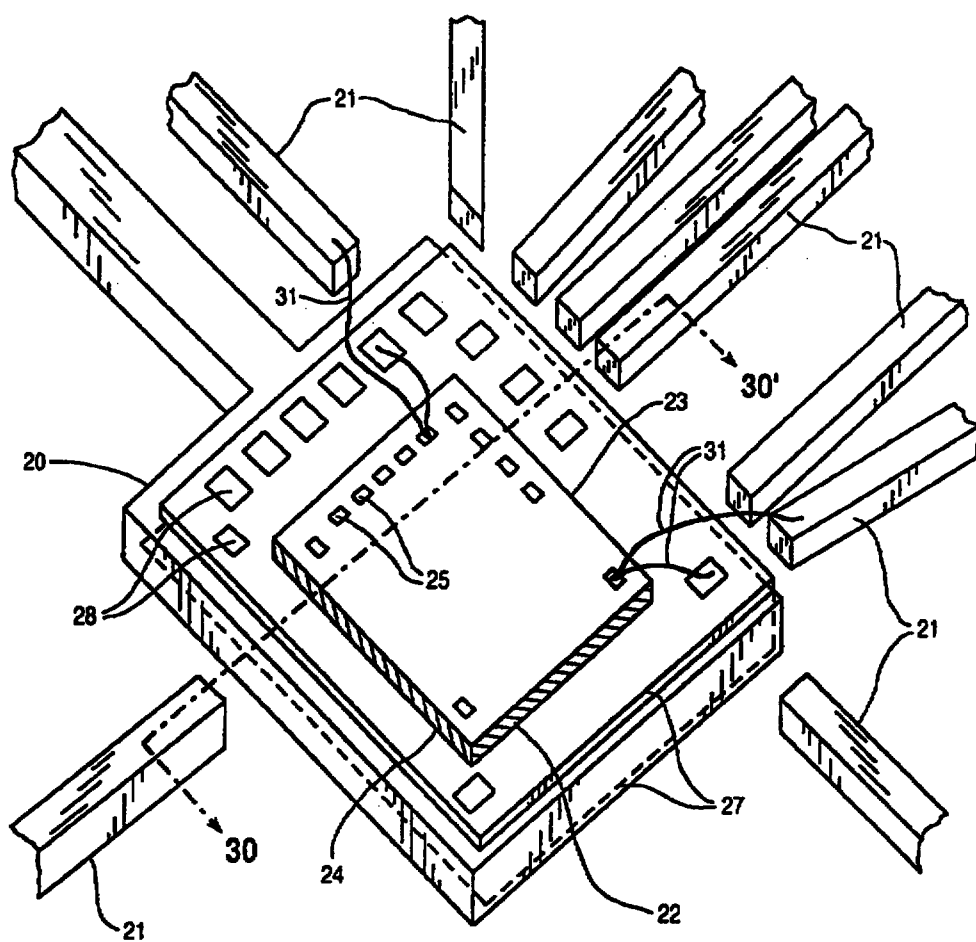


FIG. 1

2/4

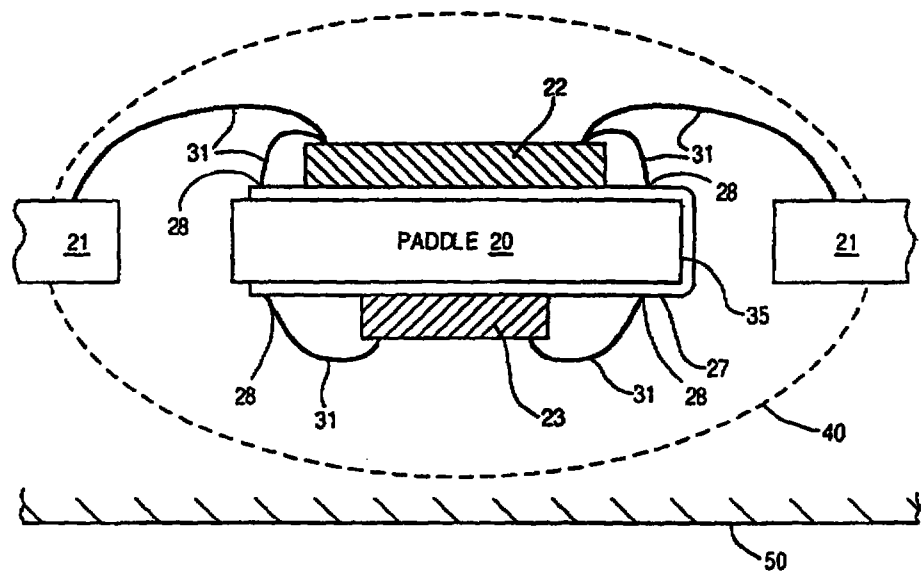


FIG. 2

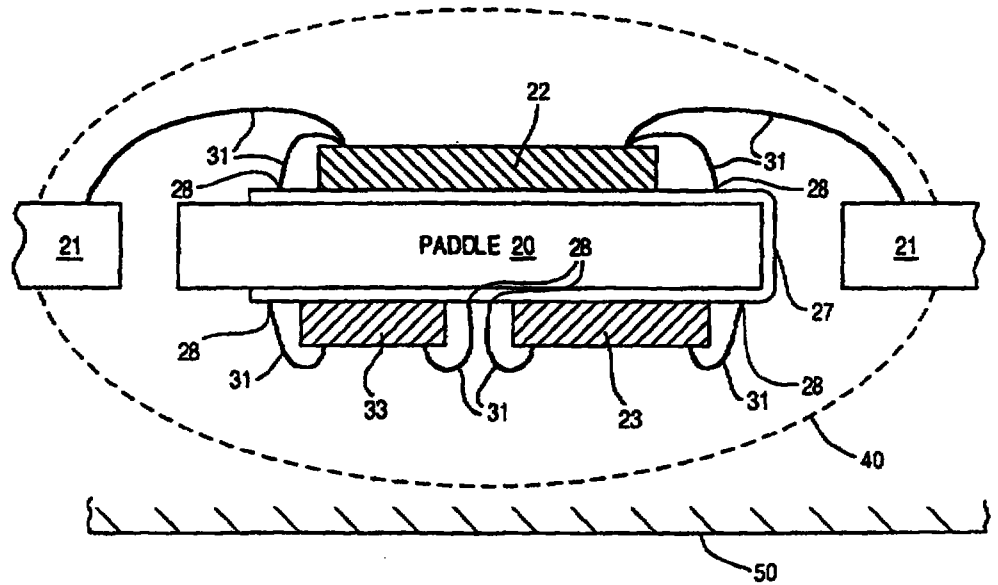
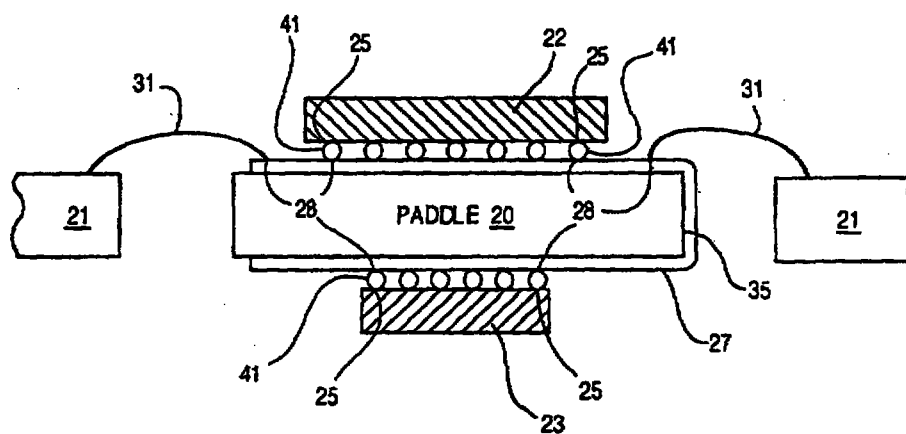


FIG. 3

3/4

**FIG. 4**

4/4

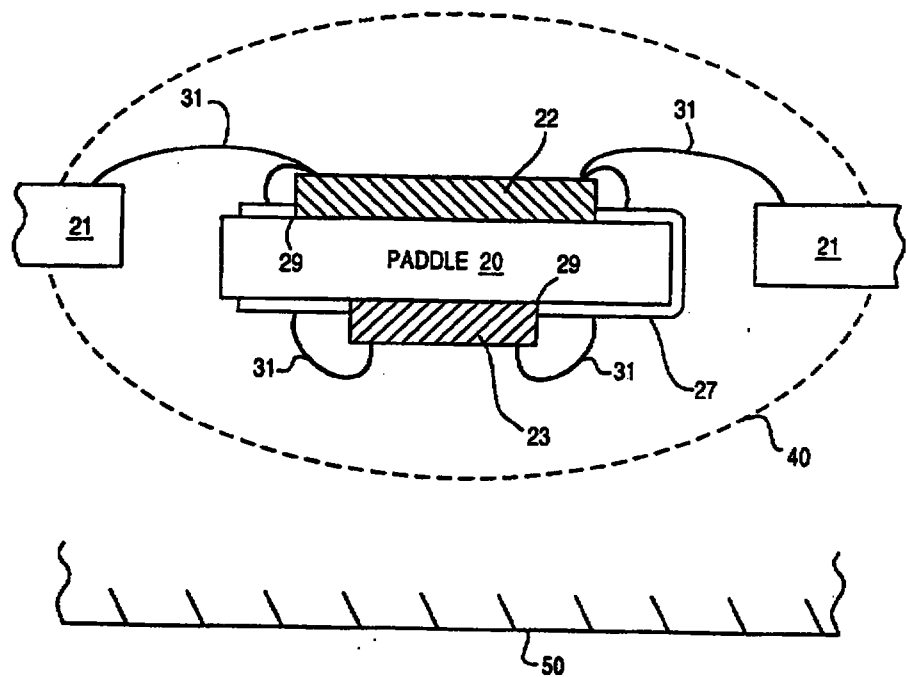


FIG. 5

- 12 -

CLAIMS

I claim:

1. A semiconductor package comprising:

a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;

a flexible circuit laminated to the first and second primary surfaces and wrapped around the side of the paddle, the flexible circuit having a plurality of interconnects embedded therein, the interconnects having a first set of bonding areas disposed on the first primary surface and a second set of bonding areas disposed on the second primary surface of the paddle;

first and second semiconductor dies each having a face with integrated circuitry constructed thereon and a back, the back of the first semiconductor die being bonded over the first primary surface, and the back of the second semiconductor die being bonded over the second primary surface of the paddle;

a first set of wires electrically connecting the integrated circuitry of the first semiconductor die to the first set of bonding areas and to the lead fingers;

a second set of wires electrically connecting the integrated circuitry of the second semiconductor die to the second set of bonding areas, thereby coupling together the integrated circuitry of the first and second semiconductor dies; and

a casing which encloses the semiconductor dies.



- 13 -

2. The semiconductor package of claim 1 further comprising a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

3. The semiconductor package of claim 2 wherein the material is characteristically impervious to light.

4. The semiconductor package of claim 1 wherein the casing comprises a plastic.

5. The semiconductor package of claim 1 wherein the casing comprises a ceramic.

6. The semiconductor package of claim 1 wherein the paddle and the first and second semiconductor dies each have a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions than either the first or second semiconductor dies.

7. The semiconductor package of claim 6 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.



- 14 -

8. The semiconductor package of claim 6 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

9. The semiconductor package of claims 2, 3, 4, 5, 6, 7 or 8 wherein the a flexible circuit includes an opening, the first set of bonding pads being disposed about the opening, the first semiconductor die being mounted directly to the first primary surface of the paddle through the opening.

10. A semiconductor package comprising:

a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;

a flexible substrate having a plurality of interconnects embedded therein, a first section of the flexible substrate being bonded to the first primary surface of the paddle, and a second section of the flexible substrate being bonded to the second primary surface of the paddle;

first and second semiconductor dies each having a back, and a face with integrated circuitry constructed thereon, the integrated circuitry on the face of the first semiconductor die being connected to a plurality of conductive bumps mounted to the first section of the flexible substrate wherein the bumps provide electrical connection between the integrated circuitry of the first semiconductor die and the plurality of interconnects; the back of the second semiconductor die being mounted to the second section of the flexible substrate;



- 15 -

a first set of wires electrically connecting the plurality of interconnects to the lead fingers;

a second set of wires electrically connecting the integrated circuitry of the second semiconductor die to the plurality of interconnects, thereby coupling together the integrated circuitry of the first and second semiconductor dies; and

a casing which encloses the first and second semiconductor dies and the first and second sets of wires.

11. The semiconductor package of claim 10 further comprising a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the first and second semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

12. The semiconductor package of claim 11 wherein the material is characteristically impervious to light.

13. The semiconductor package of claim 10 wherein the casing comprises a plastic.

14. The semiconductor package of claim 10 wherein the casing comprises a ceramic.

15. The semiconductor package of claim 10 wherein the paddle and the first and second semiconductor dies each have a lateral



- 16 -

dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions than either the first or second semiconductor dies.

16. The semiconductor package of claim 15 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.

17. The semiconductor package of claim 15 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

18. A semiconductor package comprising:

a leadframe which includes a plurality of lead fingers and a paddle having a body with a side and first and second substantially parallel primary surfaces;

a flexible substrate having a plurality of interconnects embedded therein, a first section of the flexible substrate being bonded flush to the first primary surface of the paddle, and a second section of the flexible substrate being bonded flush to the second primary surface of the paddle;

first and second semiconductor dies each having a back, and a face with integrated circuitry constructed thereon, the integrated circuitry on the face of the first semiconductor die being connected to a plurality of first conductive bumps mounted to the first section of the flexible



- 17 -

substrate wherein the first bumps provide electrical connection between the integrated circuitry of the first semiconductor die and the plurality of interconnects, the integrated circuitry on the face of the second semiconductor die being connected to a plurality of second conductive bumps mounted to the second section of the flexible substrate wherein the second bumps provide electrical connection between the integrated circuitry of the second semiconductor die and the plurality of interconnects;

a set of wires electrically connecting the plurality of interconnects to the lead fingers; and

a casing which encloses the first and second semiconductor dies and the set of wires.

19. The semiconductor package of claim 18 further comprising:

a coating covering the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the first and second semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

20. The semiconductor package of claim 19 wherein the material is characteristically impervious to light.

21. The semiconductor package of claim 18 wherein the casing comprises a plastic.



- 18 -

22. The semiconductor package of claim 18 wherein the casing comprises a ceramic.

23. The semiconductor package of claim 18 wherein the paddle and the first and second semiconductor dies each have a lateral dimension associated therewith, the lateral dimension of the paddle being substantially parallel to the first and second primary surfaces and larger than the lateral dimensions than either the first or second semiconductor dies.

24. The semiconductor package of claim 23 wherein the lateral dimension of the first semiconductor die is larger than the lateral dimension of the second semiconductor die.

25. The semiconductor package of claim 23 wherein the lateral dimension of the second semiconductor die is larger than the lateral dimension of the first semiconductor die.

26. A semiconductor package comprising:
a leadframe which includes a paddle having first and second substantially parallel primary surfaces and a side, the first and second primary surfaces being substantially perpendicular to the side, the leadframe also including a plurality of lead fingers disposed in the same general plane as the first and second primary surfaces of the paddle, the lead fingers extending near to, but not contacting, the paddle, with a



- 19 -

portion of the lead fingers being separated from the side of the paddle by a determined distance;

a flexible circuit comprising a plurality of conductive lines interconnecting distinct sets of bonding pads, the flexible circuit being laminated to the first and second primary surfaces and wrapped over the side of the paddle such that a first set of bonding pads provide a first die-mounting area against the first primary surface, and a second set of bonding pads provide a second die-mounting area against the second primary surface of the paddle;

first and second semiconductor dies each having a back and a face with integrated circuitry constructed thereon, the first semiconductor die being mounted in the first die-mounting area of the flexible circuit, and the second semiconductor die being mounted in the second die-mounting area of the flexible circuit;

first and second sets of interconnects electrically connecting the integrated circuitry of the first and second semiconductor dies to the first and second sets of bonding pads, respectively, thereby coupling together the integrated circuitry of the first and second semiconductor dies;

a set of wires electrically connecting the integrated circuitry of the second semiconductor die to the second set of bond pads, thereby coupling the integrated circuitry of the first and second semiconductor dies; and

a casing which encapsulates the first and second semiconductor dies.



- 20 -

27. The semiconductor package of claim 26 wherein the first and second sets of interconnects each comprise solder bumps such that the faces of the first and second semiconductor dies adjoin the first and second die-mounting areas of the flexible circuit, respectively.

28. The semiconductor package of claim 27 wherein the plurality of conductive lines comprise copper.

29. The semiconductor package of claim 26 wherein the paddle is centrally-located within the package.

30. The semiconductor package of claim 26 wherein the flexible circuit further includes a third set of bonding pads providing a third die-mounting area against the second primary surface of the paddle, the package further comprising:

a third semiconductor die having a back and a face with integrated circuitry constructed thereon, the third semiconductor die being mounted in the third die-mounting area of the flexible circuit; and

a third set of interconnects electrically connecting the integrated circuitry of the third semiconductor die to the third set of bonding pads, thereby coupling the integrated circuitry of the third semiconductor die to either the first or second semiconductor dies, or to both the first and second semiconductor dies.

31. The semiconductor package of claim 30 wherein the back of the third semiconductor die is mounted in the third die-mounting area



- 21 -

of the flexible circuit, and the third set of interconnects comprise wires coupling the integrated circuitry on the face of the third semiconductor die to the third set of bonding pads.

32. The semiconductor package of claim 30 wherein the third set of interconnects comprise solder bumps such that the face of the third semiconductor die adjoins the third die-mounting area of the flexible circuit.

33. The semiconductor package of claim 30 wherein the casing comprises a plastic.

34. The semiconductor package of claim 30 wherein the casing comprises a ceramic.

35. The semiconductor package of claims 26, 27, 28, 29, 30, 31, 32, 33 or 34 further comprising a coating which conformably covers the first and second semiconductor dies, the coating comprising a material which adheres to the faces of the semiconductor dies such that penetration of the material substantially destroys the integrated circuitry constructed thereon.

36. The semiconductor package of claim 35 wherein the material is characteristically impervious to light.



- 22 -

37. The semiconductor package of claim 26 wherein the integrated circuitry of the first semiconductor die comprises a microprocessor or a microcontroller.

38. The semiconductor package of claim 37 wherein the integrated circuitry of the second semiconductor die comprises a memory device storing a proprietary code.

39. A method of packaging multiple semiconductor dies comprising the steps of:

(a) providing a leadframe having a paddle with first and second primary surfaces and a plurality of lead fingers which extend near to the paddle;

(b) bonding a flex circuit to the paddle such that a first portion of the flex circuit having a first set of bonding pads providing a first die-mounting area is flush with the first primary surface, and a second set of bonding pads providing a second die-mounting area is flush with the second primary surface, the first and second sets of bonding pads being electrically interconnected;

(c) mounting first and second semiconductor dies against the first and second die-mounting areas, respectively, the first and second semiconductor dies each having a back and a face with integrated circuitry constructed thereon;

(d) coupling the integrated circuitry of the first and second semiconductor dies to the flex circuit and to the plurality of lead fingers;
and



- 23 -

(e) encasing the first and second semiconductor dies.

40. The method of claim 39 wherein the backs of the first and second semiconductor dies are mounted against the first and second die-mounting areas, respectively, in step (c).

41. The method of claim 40 wherein step (d) comprises the steps of:

wire-bonding the integrated circuitry on the face of the first semiconductor die to the first set of bonding pads and to the plurality of lead fingers; and

wire-bonding the integrated circuitry on the face of the second semiconductor die to the second set of bonding pads.

42. The method of claim 39 further comprising the step, prior to step (e), of:

conformably coating the first and second semiconductor dies with a material that encapsulates the first and second semiconductor dies.

43. A semiconductor package providing code and/or data security comprising:

a leadframe which includes a plurality of lead fingers and a paddle having opposing first and second primary surfaces;

a flexible circuit having a first section, a second section, and a plurality of interconnects embedded therein, the first and second



- 24 -

sections being laminated against the first and second primary surfaces of the paddle, respectively;

first and second semiconductor dies having respective first and second integrated circuits fabricated thereon, the first semiconductor die being mounted in the first section of the flexible circuit and the second semiconductor die being mounted in the second section of the flexible circuit, the second integrated circuit comprising a memory storing a code and/or data and the first integrated circuit comprising a device that provides sole access to the code and/or data stored in the memory of the second integrated circuit;

means for electrically coupling the first and second semiconductor dies to the interconnects of the flexible circuit;

means for electrically connecting the first semiconductor die to the lead fingers; and

a casing which encloses the first and second semiconductor dies.

44. The semiconductor package of claim 43 wherein the first integrated circuit comprises a microprocessor or microcontroller.

45. The semiconductor package of claim 43 further comprising
a
polymer encapsulate which coats the first and second semiconductor dies, the polymer encapsulate being sufficiently adherent to the semiconductor dies such that penetration of the polymer encapsulate results in substantial destruction of the integrated circuitry fabricated thereon.



- 25 -

46. The semiconductor package of claim 45 wherein the polymer encapsulate is impervious to light.

47. The semiconductor package of claim 45 wherein each of the semiconductor dies has a back and a face, the integrated circuit of each of the semiconductor dies being fabricated on the face, with the semiconductor dies being mounted to the flexible circuit in a back-to-back relationship.

48. The semiconductor package of claim 43 wherein the first section of the flexible circuit includes a first opening, the first semiconductor die being mounted to the first primary surface of the paddle through the first opening.

49. The semiconductor package of claim 48 wherein the second section of the flexible circuit also includes an opening, the second semiconductor die being mounted to the second primary surface of the paddle through the second opening.





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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H01R 9/09, 43/02, H01L 21/60, 23/14, 23/495, B23K 31/02, H05K 5/02	A1	(11) International Publication Number: WO 96/28860 (43) International Publication Date: 19 September 1996 (19.09.96)
(21) International Application Number: PCT/US96/03331 (22) International Filing Date: 12 March 1996 (12.03.96) (30) Priority Data: 08/402,933 13 March 1995 (13.03.95) US (71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventor: KUHN, Harry, A.; 9068 North 28th Street, Phoenix, AZ 85028 (US). (74) Agents: BEREZNAK, Bradley, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).	(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report.	
(54) Title: A PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES		
(57) Abstract A package (50) housing multiple semiconductor dies (22, 23) includes a leadframe having a paddle (20) and a number of lead fingers (21). A flexible circuit (27) is adhesively laminated to both sides of the paddle. A first semiconductor die (23) is back-mounted to the bottom surface of the paddle and wire-bonded to the flexible circuit and the lead fingers. A second semiconductor die (22) is back-mounted to the top surface of the paddle and to the flexible circuit. The dies (22, 23) are encapsulated in a security coating (40) and encased in plastic (50).		