

PATENT SPECIFICATION

(11) 1387 749

1387 749

- (21) Application No. 27576/72 (22) Filed 13 June 1972
 (31) Convention Application No. 7108233 (32) Filed 16 June 1971 in
 (33) Netherlands (NL)
 (44) Complete Specification published 19 March 1975
 (51) INT CL² H03F 3/18//H01L 29/72
 (52) Index at acceptance



H3T 1A1 2J 2T2X 2T3J 2T3X 2T4 2T5 3J 3N 3P 4A2
 4C 4D 4M 4R 4X
 G1A 205 207 247 248 39X 506 773
 G2A 401 404 603 706 711 712 BJ
 H1K 211 217 21Y 353 422 511 521 54Y 563 581 583 639
 657

(54) CIRCUIT FOR GENERATING A CURRENT
 SUBSTANTIALLY EQUAL TO AN INPUT CURRENT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a circuit for generating a current which is substantially equal to an input current, over a wide current range, in which the input current operates by producing a difference between the current at the emitter of a first transistor of a first conductivity type and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the currents supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite conductivity type the base of which is controlled in accordance with the voltage produced at the collector of the first transistor.

Such a circuit may be used, for example, in photographic cameras for automatic setting of the exposure time. The output current obtained is supplied to an integrating network, the shutter being closed when a prescribed voltage is reached which is also determined by the sensitivity of the film and by the stop used. A similar use is found in automatic printing devices for printing film negatives.

As a measuring element for converting the incident light into an electric current a photo-sensitive semiconductor diode is increasingly being used. Such a diode may simply be connected to, or included in, an integrated circuit, its small size and low sensitivity to variations in temperature and supply voltage being of importance in this respect. The invention utilizes the recognition of the fact

that the measurement will be appreciably more accurate when the short-circuit current (i.e. the current measured at an external voltage=zero) than when the open-circuit voltage (i.e. the voltage measured at an external current=zero) of the photodiode is measured; in the latter method of measuring a leakage current of the order of 100 pA per volt, which current depends upon the voltage across the diode, plays a part which limits the maximum sensitivity to be attained.

In a known circuit of the aforementioned type, which was also designed to re-generate the short-circuit current of a current source, two current mirrors are used one of which includes a *pnp* transistor whilst the other includes *nnp* transistors. This circuit is intended to cover a current range from 20 μ A to 20 mA. It is an object of the invention to provide an improvement such that an integrated circuit is obtained which is suitable for input currents in a range from less than 10 pA to more than 10 μ A, that is a range of at least 6 powers of ten.

According to the present invention there is provided a circuit for generating a current which is substantially equal to an input current over a wide current range, in which the input current operates by producing a difference between the currents at the emitter of a first transistor of a first conductivity type and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the current supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite conductivity type the base of which is controlled in accordance with the voltage produced at the collector of the first transistor, in which the second transistor has a plurality of collectors a first one of which supplies the current to the diode and a second one of which supplies the current to the col-

lector of the first transistor, in that the base current of the second transistor is produced by a current-amplifying transistor circuit which comprises at least a third transistor of the first conductivity type, the output current being derived from a third collector of the second transistor or from the collector of a fourth transistor of the first conductivity type the base of which is connected to the base of the first transistor.

Further according to the present invention there is provided an integrated circuit for generating a current which is substantially equal to an input current, over a wide current range, in which the input current operates by producing a difference between the currents at the emitter of a first transistor and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the currents supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite conductivity type the base of which is controlled in accordance with the voltage produced at the collector of the first transistor, characterized in that the first transistor takes the form of a vertical (preferably *npn*) transistor, in that the second transistor takes the form of a lateral (preferably *pnp*) transistor having a plurality of collectors a first one of which supplies the current to the diode and a second one of which supplies the current to the collector of the first transistor, in that the base current of the second transistor is produced by a current-amplifying transistor circuit which comprises at least a third, vertical transistor, the output current being derived from a third collector of the lateral transistor or from the collector of a fourth, vertical transistor the base of which is connected to that of the first transistor.

In the circuit according to the invention the diode and the first transistor also form a current mirror; however, the transistor circuit which includes the second transistor deliberately is not designed as a current mirror, for although when multicollector lateral transistors are used it can be ensured that the currents delivered by these collectors are substantially equal to one another or are in a fixed ratio to one another which is determined by the ratio between the collecting areas, in the case of current operation of the order of several pA the required base current is such as to give rise to a new error source in the output current produced; this error source is suppressed by the use of the steps according to the invention.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Fig. 1 is a circuit diagram of a simplified embodiment of the invention,

Fig. 2 is a more elaborate circuit diagram, Fig. 3 is the associated semiconductor layout, and

Fig. 4 is a modification of the circuit shown in Fig. 1.

Referring now to Figure 1, the base emitter path of a first transistor T_1 is shunted by the series combination of a diode D_1 and a current source in the form of a photodiode P . The currents to the collector of the transistor T_1 and to the diode D_1 are supplied by collectors c_1 and c_2 respectively of a second transistor T_2 of the opposite conductivity type. The collector of the transistor T_1 is also connected to the base of a transistor T_3 the conductivity type of which is the same as that of T_1 and the collector of which is connected to the base of T_2 . The output current is derived from a further collector c_3 of T_2 .

The circuit is made in integrated-circuit form, however, in general the photodiode P preferably is not included in this circuit to permit greater freedom in the choice of the photosensitivity and/or colour sensitivity of such a diode.

The transistors T_1 and T_3 are vertical (transversal) transistors, i.e. in the semiconductor element of the integrated circuit the various active transistor regions, when viewed from above, lie one on top of the other. The transistor T_2 here is a lateral transistor, i.e. the active transistor regions, when viewed from above, lie side by side. The diode D_1 also is a vertical transistor the base and collector of which are electrically interconnected. Preferably T_1 and T_3 are vertical *npn* transistors and T_2 is a lateral *pnp* transistor.

It is a known property of multi-collector transistors that the currents which flow to the various collectors c_1 , c_2 and c_3 are solely determined, within close tolerances, by the sizes of the collecting areas of these collectors. With the very low current biases mentioned hereinbefore special attention must be paid to a symmetrical arrangement of the collectors with respect to the emitter, but this may readily be achieved in practice. It is also known that in vertical transistors having parallel-connected emitter base paths the ratios between the emitter currents are substantially determined only by the sizes of the emitting areas. These known properties are utilized in the present invention.

Assuming the areas of the collectors c_1 and c_2 to be equal, these collectors will deliver equal currents. Neglecting the base currents of the transistors T_1 and T_3 with respect to their collector currents, which neglect is permissible with vertical transistors, the diode D_1 and the emitter base junction of the transistor T_1 pass equal currents. When the emitter areas of D_1 and T_1 are equal the voltages across D_1 and across the emitter base junction

tion of T_1 will also be equal, in other words, the voltage across P is zero.

Consequently the photo-diode P is operated at its short-circuit current I so that errors due to diode leakage are avoided. The currents delivered by c_1 and c_2 will automatically adjust themselves so as to become equal to I, for if the current delivered by c_2 were smaller than the current I impressed by P by an amount of ΔI , this deficiency ΔI will be amplified in T_1 and T_3 and will reach the base of T_2 with a phase such that ΔI is greatly suppressed.

The described combination of steps provides a circuit which is suitable for far smaller currents than is the known circuit. In the known circuit the transistor T_2 is replaced by a current mirror and the output current is supplied by a further transistor connected in series with the diode of the current mirror, the conductivity type of this further transistor being equal to that of the transistors of the current mirror. The transistors are assumed to be ideal transistors; hence those of the one conductivity type form part of another integrated circuit than those of the other conductivity type. However, when according to the concept of the invention all the transistors are accommodated in one common integrated circuit, the lateral transistors used will cause a deviation from the ideal such that the output current produced differs widely from the input current offered.

In the case of a comparatively large bias currents the circuit hitherto described will tend to instability, for a deficiency ΔI of offered current is amplified in each of the transistors T_1 and T_3 by a factor of β_n and then multiplied in the transistor T_2 by a factor of β_p , where β is the collector base current gain factor. At a very low current setting, for example $I=20$ pA, β_n may be 20 and β_p may be 0.5, so that a (negative) loop amplification $\beta_n^2 \cdot \beta_p = 200$ is to be expected. At a current setting which is higher by some powers of ten, for example $I=20$ μ A, β_n may rise to 100 and β_p may rise to 20, so that the loop amplification will be 200,000. It is true that the provision of capacitors at suitable points enables the circuit to be maintained stable, however, this step will also cause the response of the circuit to rapid variations of the current I offered by P to become slower.

In the circuit shown in Figure 2 this disadvantage is obviated in that the current gain of T_1 is artificially reduced to unity and that of T_2 is controlled so that it substantially cannot exceed a fixed value. Thus the loop amplification is determined only by the β_n of T_3 , so that the likelihood of instability is largely suppressed. By means of a small artifice this β_n may readily be stabilised at a

value which is independent of the spread in the actual β .

The circuit shown in Figure 2 includes an additional diode D_2 whilst the collector c_2 has a larger collecting area than has the collector c_1 . In practice the diode D_2 also is a vertical transistor the collector of which is connected to the base. When the emitter area of D_2 also is equal to that of T_1 , the area of c_2 is made twice that of c_1 , which is shown symbolically by the double line of c_2 . When c_1 supplies a current $I-\Delta I$, c_2 will supply a current $2I-2\Delta I$. D_1 can only pass a current I. Hence the remainder of the current, $I-2\Delta I$, is supplied to D_2 and to the base of T_1 which behave as a current mirror. Thus the collector of T_1 passes a current $I-2\Delta I$; c_1 offers a current $I-\Delta I$ and consequently the current difference ΔI is supplied to the further current amplifier which includes the transistor T_3 .

This current amplifier further comprises vertical transistors T_4 and T_5 of a conductivity type equal to that of T_1 . The collector of T_1 is connected to the base of T_4 and to the collector of T_5 . The emitter of T_4 is connected to the bases of T_5 and T_3 ; its collector is connected to the supply terminal + or, if required, to the collector of T_3 . A small reverse bias voltage V, for example of the order of 100 mV, is set up in the emitter of T_5 . This circuit arrangement causes the current ΔI supplied to $T_4-T_5-T_3$ to be amplified by a fixed factor of N which is determined by the voltage V, so that a current $N\Delta I$ flows in the collector of T_3 .

The transistor T_2 has an additional lateral collector c_4 which is connected to the base of T_2 . The collecting area of c_4 is made equal, for example, to that of c_1 , so that c_4 also passes a current $I-\Delta I$. If the area of c_3 also is equal to that of c_1 , the base current of T_2 will be

$$\frac{5(I-\Delta I)}{\beta_p}$$

so that

$$N\Delta I = \frac{5(I-\Delta I)}{\beta_p} + (I-\Delta I) \quad 110$$

(The factor of 5 corresponds to the number of collectors used, for β_p is defined as the ratio between the combined currents flowing to c_1 to c_4 and the base current of T_2). If now β_p is less than 1 (low current setting), the first term of the right side will play the chief part; if, however, β_p increases to exceed 10 (higher current setting), the first term may be progressively neglected with respect to the second term, which means that the effective current gain of T_2 is limited.

Figure 3 shows the layout of the circuit of Figure 2. The current offered by the photodiode P is supplied to a bonding pad 1 which is connected to one electrode of the diode D₁ the other electrode of which is connected by a lead 2 to the corresponding electrode of the diode D₂, to a base contact b₁ of the transistor T₁ and to collectors c₂ of the transistor T₂. The other electrode of D₂ and emitter contacts e₁ and e₃ of T₁ and T₃ respectively are connected by a lead 3 to one another and to a pad 4 which is to be earthed. T₁, T₃, T₄ and T₅ have the form of vertical transistors, preferably of the *npn* type. Hence the *p*-type base region extends beneath the *n*-type emitter region having a contact e, whilst the *n*-type collector region in turn extends beneath this base region. Where these three regions are directly superimposed, transistor action with a comparatively high current gain β_n is obtained.

A collector k₁ of T₁ is connected by a lead 5 to the collectors c₁ of T₂ and k₂ of T₅ and to the base b₄ of T₄. The collector region of T₄ forms part of a large *n*-type island which also comprises the base region of T₂. This island includes *p*-type regions which are arranged side by side and ensure a lateral transistor action. The emitter of T₂ comprises three circular *p*-type regions e₂ which by a lead 6 are connected to one another and to a pad 7 to be connected to the (positive) supply terminal. This lead 6 is also connected to the collector k₂ of T₄. The *p*-type collector regions c are arranged symmetrically around the emitter regions. As the Figure shows, the collecting areas of c₂, c₃ and c₄ are twice, five times and four times respectively that of c₁. When we recall to mind the discussion with reference to Figure 2 we will see that these collectors c₁—c₄ supply the currents I, 2I, 5I and 4I respectively.

The regions c₄ which are interconnected by a lead are connected at 8 to the *n*-type island which comprises the base region of T₂ and the collector region of T₅. The collectors c₃, which are interconnected by a lead, are further connected to an output pad 9 which supplies the re-generated current (in this case 5I). A lead 10 connects the base b₅ of T₅ to the base b₅ of T₃ and to the emitter e₄ of T₄, and the emitter e₅ of T₅ is connected to a pad 11 to which the voltage V is to be applied.

The device described may be manufactured by means of photolithographic etching generally used in semiconductor technology in combination with epitaxial growing techniques and doping methods, such as for example diffusion, possibly of doped-out oxide, or ion implantation. Obviously other arrangements of the collectors c of the transistor T₂ around its emitter may be used, for example a single strip-shaped emitter region flanked

on both sides by symmetrically disposed discrete collector regions.

In the modified embodiment shown in Figure 4 the photodiode P is included in the emitter circuit of the transistor T₁ the base of which is connected to earth via the diode D₁. The lateral transistor T₂ here also through its collectors c₁ and c₂ supplies equal currents to the collector of T₁ and to the diode D₁ respectively, assuming the emitting areas of T₁ and D₁ to be equal. P is again operated at zero voltage, i.e. at its short-circuit current. The collector voltage of T₁ is applied to a lateral transistor T₄ of the same conductivity type as is T₂, after which current amplification in the vertical transistor T₃ is effected. The loop amplification now is $\beta_n \cdot \beta_p^2$. In this embodiment also the same refinements as described with reference to Figure 2 may be used, i.e. providing the diode D₂ limiting the current gain of T₂ by means of the collector c₄, and limiting the current gain β_p of T₄ in a similar manner.

Naturally a variety of obvious modifications may be conceived. If, for example, the active area of the diode D₁ is n₁ times the emitter area of T₁, in Figure 1 the collecting area of c₂ also is to be made n₁ times that of c₁. If the effective gain of T₁ is to be stabilised at a fixed value greater than unity, the active area of D₂ in Figure 2 may be made n₂ times smaller than the emitting area of T₁, where n₂ is to be smaller than β_n and the area of c₂ is to be

$$\frac{1}{(n_1 + \frac{1}{n_2})}$$

times that of c₁. The connection between c₂ and D₁ may further include the collector emitter path of a further vertical transistor the base of which is connected to c₁, thus perfecting the current mirror action. The output current need not be derived from c₂ but may alternatively be derived from the collector of a further vertical transistor T₇ (see Figure 1) the base of which is connected to that of T₁, for if the emitter areas of T₁ and T₇ are equal, these transistors will pass equal currents which are substantially equal to I.

WHAT WE CLAIM IS:—

1. Circuit for generating a current which is substantially equal to an input current over a wide current range, in which the input current operates by producing a difference between the currents at the emitter of a first transistor of a first conductivity type and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the currents supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite con-



Figure 3 shows the layout of the circuit of Figure 2. The current offered by the photodiode P is supplied to a bonding pad 1 which is connected to one electrode of the diode D₁ the other electrode of which is connected by a lead 2 to the corresponding electrode of the diode D₂, to a base contact b₁ of the transistor T₁ and to collectors c₂ of the transistor T₂. The other electrode of D₂ and emitter contacts e₁ and e₃ of T₁ and T₃ respectively are connected by a lead 3 to one another and to a pad 4 which is to be earthed. T₁, T₃, T₄ and T₅ have the form of vertical transistors, preferably of the *n**p**n* type. Hence the *p*-type base region extends beneath the *n*-type emitter region having a contact e, whilst the *n*-type collector region in turn extends beneath this base region. Where these three regions are directly superimposed, transistor action with a comparatively high current gain β_n is obtained.

A collector k₁ of T₁ is connected by a lead 5 to the collectors c₁ of T₂ and k₅ of T₅ and to the base b₄ of T₄. The collector region of T₅ forms part of a large *n*-type island which also comprises the base region of T₂. This island includes *p*-type regions which are arranged side by side and ensure a lateral transistor action. The emitter of T₂ comprises three circular *p*-type regions e₂ which by a lead 6 are connected to one another and to a pad 7 to be connected to the (positive) supply terminal. This lead 6 is also connected to the collector k₄ of T₄. The *p*-type collector regions c are arranged symmetrically around the emitter regions. As the Figure shows, the collecting areas of c₂, c₃ and c₄ are twice, five times and four times respectively that of c₁. When we recall to mind the discussion with reference to Figure 2 we will see that these collectors c₁—c₄ supply the currents I, 2I, 5I and 4I respectively.

The regions c₄ which are interconnected by a lead are connected at 8 to the *n*-type island which comprises the base region of T₂ and the collector region of T₃. The collectors c₂, which are interconnected by a lead, are further connected to an output pad 9 which supplies the re-generated current (in this case 5I). A lead 10 connects the base b₃ of T₃ to the base b₅ of T₅ and to the emitter e₄ of T₄, and the emitter e₅ of T₅ is connected to a pad 11 to which the voltage V is to be applied.

The device described may be manufactured by means of photolithographic etching generally used in semiconductor technology in combination with epitaxial growing techniques and doping methods, such as for example diffusion, possibly of doped-out oxide, or ion implantation. Obviously other arrangements of the collectors c of the transistor T₂ around its emitter may be used, for example a single strip-shaped emitter region flanked

on both sides by symmetrically disposed discrete collector regions.

In the modified embodiment shown in Figure 4 the photodiode P is included in the emitter circuit of the transistor T₁ the base of which is connected to earth via the diode D₁. The lateral transistor T₂ here also through its collectors c₁ and c₂ supplies equal currents to the collector of T₁ and to the diode D₁ respectively, assuming the emitting areas of T₁ and D₁ to be equal. P is again operated at zero voltage, i.e. at its short-circuit current. The collector voltage of T₁ is applied to a lateral transistor T₄ of the same conductivity type as is T₂, after which current amplification in the vertical transistor T₃ is effected. The loop amplification now is $\beta_n \cdot \beta_p^2$. In this embodiment also the same refinements as described with reference to Figure 2 may be used, i.e. providing the diode D₂, limiting the current gain of T₂ by means of the collector c₄, and limiting the current gain β_p of T₄ in a similar manner.

Naturally a variety of obvious modifications may be conceived. If, for example, the active area of the diode D₁ is n₁ times the emitter area of T₁, in Figure 1 the collecting area of c₂ also is to be made n₁ times that of c₁. If the effective gain of T₂ is to be stabilised at a fixed value greater than unity, the active area of D₂ in Figure 2 may be made n₂ times smaller than the emitting area of T₁, where n₂ is to be smaller than β_n and the area of c₂ is to be

$$(n_1 + \frac{1}{n_2})$$

times that of c₁. The connection between c₂ and D₁ may further include the collector emitter path of a further vertical transistor the base of which is connected to c₁, thus perfecting the current mirror action. The output current need not be derived from c₂ but may alternatively be derived from the collector of a further vertical transistor T₇ (see Figure 1) the base of which is connected to that of T₁, for if the emitter areas of T₁ and T₇ are equal, these transistors will pass equal currents which are substantially equal to I.

WHAT WE CLAIM IS:—

1. Circuit for generating a current which is substantially equal to an input current over a wide current range, in which the input current operates by producing a difference between the currents at the emitter of a first transistor of a first conductivity type and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the currents supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite con-



ductivity type the base of which is controlled in accordance with the voltage produced at the collector of the first transistor, in which the second transistor has a plurality of collectors a first one of which supplies the current to the diode and a second one of which supplies the current to the collector of the first transistor, in that the base current of the second transistor is produced by a current-amplifying transistor circuit which comprises at least a third transistor of the first conductivity type, the output current being derived from a third collector of the second transistor or from the collector of a fourth transistor of the first conductivity type the base of which is connected to the base of the first transistor.

2. Integrated circuit for generating a current which is substantially equal to an input current over a wide current range, in which the input current operates by producing a difference between the currents at the emitter of a first transistor and at an electrode of a diode the other electrode of which is connected to the base of this transistor, the currents supplied to the diode and to the collector of the first transistor being provided by a transistor circuit which comprises a second transistor of the opposite conductivity type the base of which is controlled in accordance with the voltage produced at the collector of the first transistor, characterized in that the first transistor takes the form of a vertical (preferably *npn*) transistor, in that the second transistor takes the form of a lateral (preferably *pnp*) transistor having a plurality of collectors a first one of which supplies the current to the diode and a second one of which supplies the current to the collector of the first transistor, in that the base current of the second transistor is produced by a current-amplifying transistor circuit which comprises at least a third, vertical transistor, the output current being derived from a third collector of the lateral transistor or from the collector of a

fourth, vertical transistor the base of which is connected to that of the first transistor.

3. Circuit as claimed in Claim 2, characterized in that a fourth collector of the lateral transistor is connected to the base thereof. 50

4. Circuit as claimed in Claim 2 or Claim 3, characterized in that the base of the first transistor is connected to a second diode and the area of the second collector of the lateral transistor for supplying the current through this second diode is made correspondingly greater. 55

5. Circuit as claimed in Claim 2, Claim 3 or Claim 4, characterized in that the collector of the first transistor is connected to the base of a fourth transistor and to the collector of a fifth, vertical transistor to the emitter of which a small reverse bias voltage is applied and the base of which is connected to that of the third transistor and to the emitter of the fourth transistor. 60 65

6. Circuit as claimed in Claim 2, Claim 3 or Claim 4, characterized in that the collector of the first transistor is connected to the base of a sixth, lateral transistor the collector of which is connected to the base of the third transistor. 70

7. Circuit for generating over a wide current range a current substantially equal to an input current substantially as described with reference to Figures 1, 2 or 4 of the accompanying drawings. 75

8. Integrated circuit for generating over a wide current range a current substantially equal to an input current, substantially as described with reference to Figure 1 or Figures 2 and 3, or Figure 4 of the accompanying drawings. 80

C. A. CLARK,
Chartered Patent Agent,
Century House,
Shaftesbury Avenue,
London, W.C.2.
Agent for the Applicants.