# FLIP CHIP ASSEMBLY PROCESS FOR ULTRA THIN SUBSTRATE AND PACKAGE ON PACKAGE ASSEMBLY

## FIELD OF THE INVENTION

Embodiments of the present invention generally relate to the field of integrated circuit packages, and, more particularly to flip chip assembly process for ultra thin substrate and package on package assembly.

## BACKGROUND OF THE INVENTION

As microelectronic components shrink in size, a trend has emerged to provide package substrates that may be characterized as thin core substrates (that is, substrates having a core with a thickness less than or equal to 400 microns and larger than zero), or no-core substrates (that is, substrates without cores).

Disadvantageously, with a thin or no-core substrate, however, decrease in yield at first level chip attach due to warpage causing nonwets may occur during the package manufacturing process, such as, for example, during flip chip bonding where substrate flatness and rigidity are required. To address the above issue, the prior art sometimes provides substrates that may have a thickness of at least several tens of microns or more. However, the above measure disadvantageously detracts from further package size minimization.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements, and in which:

**FIG. 1** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 2** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 3** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 4** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 5** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 6** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention;

**FIG. 7** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention; and

**FIG. 8** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention.

## DETAILED DESCRIPTION

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that embodiments of the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

**Fig. 1** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. In accordance with the illustrated example embodiment, package 100 includes one or more of coreless substrate strip 102, backside contacts 104, topside contacts 106 and substrate thickness 108.

Coreless substrate strip 102 represents a thin substrate that may be rolled out and processed before being singulated. In one embodiment, coreless substrate strip 102 is a direct laser lamination generation 3 (DLL3) strip. In one embodiment, substrate thickness 108 is about 200 micrometers.

**Fig. 2** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 200, solder balls 202 have been attached to backside 204 of coreless substrate strip 102. In one embodiment, solder ball diameter 206 is about 10 mils.

**Fig. 3** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 300, mold compound 302 is dispensed as a liquid amongst the solder balls and compressed by mold form 304. In one embodiment, mold form 304 is designed to compress mold compound 302 below the height of the solder balls. Mold form 304 may be held in place for some time and may be heated to allow mold compound 302 to cure.

**Fig. 4** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 400, stiffening mold 402 is cured amongst solder balls 202 and provides added stiffness to package 400. In one embodiment, stiffening mold 402 has a mold thickness 404 of about 200 micrometers.

**Fig. 5** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 500, the package has been flipped over for topside processing.

**Fig. 6** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 600, integrated circuit device 602 has been attached to topside 604 of coreless substrate strip 102. Integrated circuit device 602 may represent any type of silicon processor or controller or logic.

**Fig. 7** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 700, underfill material 702 has been dispensed under integrated circuit device 602.

**Fig. 8** is a graphical illustration of a cross-sectional view of a partially formed IC package, in accordance with one example embodiment of the invention. As shown in package 800, second integrated circuit device package 802 has been attached to topside 604 through solder balls 804. Second integrated circuit device package 802 may be any type of package and need not be a flip chip package.

In one embodiment, package 800 is processed further and singulated from other packages.

In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced

without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form.

Many of the methods are described in their most basic form but operations can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present invention. Any number of variations of the inventive concept is anticipated within the scope and spirit of the present invention. In this regard, the particular illustrated example embodiments are not provided to limit the invention but merely to illustrate it. Thus, the scope of the present invention is not to be determined by the specific examples provided above but only by the plain language of the following claims.

## CLAIMS

What is claimed is:

1. A method comprising:

receiving a coreless substrate strip;

attaching solder balls to a backside of the coreless substrate strip; and

forming a backside stiffening mold amongst the solder balls.

2. The method of claim 1, wherein forming a backside stiffening mold amongst the solder balls comprises:

dispensing a liquid mold compound; and

compressing the liquid mold compound below a height of the solder balls.

3. The method of claim 1, wherein the coreless substrate strip comprises a direct laser lamination generation 3 (DLL3) strip.

4. The method of claim 1, further comprising attaching an integrated circuit device to a topside of the coreless substrate strip.

5. The method of claim 4, further comprising attaching a second integrated circuit device package to the topside of the coreless substrate strip.

6. A method comprising:

receiving a direct laser lamination generation 3 (DLL3) substrate strip;

attaching solder balls to a backside of the DLL3 substrate strip; and

forming a backside stiffening mold amongst the solder balls.

7. The method of claim 6, wherein the DLL3 substrate strip comprises a thickness of about 200 micrometers.

8. The method of claim 6 wherein the backside stiffening mold comprises a thickness of about 200 micrometers.

9. The method of claim 6, wherein forming a backside stiffening mold amongst the solder balls comprises:

dispensing a liquid mold compound; and

compressing the liquid mold compound below a height of the solder balls.

10. The method of claim 6, further comprising attaching an integrated circuit device to a topside of the coreless substrate strip.

11. The method of claim 10, further comprising attaching a second integrated circuit device package to the topside of the coreless substrate strip.

12. An apparatus comprising:

a coreless substrate strip;

a plurality of solder balls attached to a backside of the coreless substrate strip; and a backside stiffening mold amongst the solder balls.

13. The apparatus of claim 12, wherein the backside stiffening mold comprises a height of about 200 micrometers.

14. The apparatus of claim 12, wherein the coreless substrate strip comprises a height of about 200 micrometers.

15. The apparatus of claim 14, further comprising an integrated circuit device attached to a topside of the coreless substrate strip.

16. An apparatus comprising:

a direct laser lamination generation 3 (DLL3) substrate strip;

a plurality of solder balls attached to a backside of the DLL3 substrate strip;

a backside stiffening mold amongst the solder balls; and

an integrated circuit device attached to a topside of the DLL3 substrate strip.

17. The apparatus of claim 16, wherein the backside stiffening mold comprises a height of about 200 micrometers.

18. The apparatus of claim 16, wherein the DLL3 substrate strip comprises a height of about 200 micrometers.

19. The apparatus of claim 16, wherein the solder balls comprise a diameter of about 10 mils.

20. The apparatus of claim 16, further comprising a second integrated circuit device package attached to the topside of the DLL3 substrate strip.