

SPECIFICATION

Solid-state switching device

- 5 This invention relates to solid-state switching devices and, in particular, to high voltage solid-state switches.

In an article entitled "A Field Terminated Diode" by Douglas E. Houston et al., published in *IEEE*

- 10 *Transactions on Electron Devices*, Vol. ED-23, No. 8, August 1976, there is described a discrete solid-state high voltage switch that has a vertical geometry and which includes a region which can be pinched off to provide an "OFF" state or which can be made highly
- 15 conductive with dual carrier injection to provide an "ON" state. One problem with this switch is that it is not easily integrated, i.e., manufactured with other like switching devices on a common substrate. Another problem is that the spacing between the
- 20 grids and the cathode should be small to limit the magnitude of the control grid voltage; however, this limits the useful voltage range because it decreases grid-to-cathode breakdown voltage. This limitation effectively limits to relatively low voltages the use of
- 25 two of the devices connected in antiparallel, i.e., with the cathode of each coupled to the anode of the other. Such a dual device structure would be useful as a high voltage bidirectional solid-state switch. An additional problem is that the base region should
- 30 ideally be highly doped to avoid punch-through from the anode to the grid, but this leads to a low voltage breakdown between anode and cathode. Widening of the base region limits the punch-through effect but it also increases the resistance of the devices in
- 35 the "ON" state.

- According to the present invention there is provided a solid-state switching device comprising: a semiconductor body whose bulk is of one conductivity type and which has a major surface; a localized
- 40 first region which is of the one conductivity type; a localized second region which is of the opposite conductivity type; the localized first and second regions being of relatively low resistivity as compared to the bulk of the semiconductor body and
- 45 being separated by portions of the bulk of the semiconductor body; each of the first and second regions having a portion that forms part of the major surface; a gate region of the said opposite conductivity type which has a low resistivity as compared to
- 50 the bulk of the semiconductor body and is separated from the first and second regions by portions of the bulk of the semiconductor body; the structure being adapted to selectively facilitate current flow between the first and second regions or by application of a
- 55 suitable potential to the gate region, to divert a sufficient portion of the current into the gate region so as to substantially interrupt the current flow between the first and second regions; the structure being also adapted to substantially inhibit current
- 60 from flowing between the first and second regions while the said suitable potential is applied to the gate region.

- Such a switching device, which is to be denoted herein as a gate diode switch (GDS), is capable in the
- 65 OFF state of blocking relatively large potential

differences between anode and cathode regions, independent of polarity, and is capable in the ON state of conducting relatively large amounts of current with a relatively low voltage drop between anode and cathode.

- 70 Arrays of these GDSs can be fabricated on a single integrated circuit chip together with other high voltage circuit components. The bilateral blocking characteristic of the structure facilitates its use in a bidirectional switch formed by two of the structures of the present invention with the cathode of each coupled to the anode of the other and the gates being coupled together.

- Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings, of which:-

Figure 1 illustrates a switching device in accordance with the invention;

- Figure 2 illustrates a proposed electrical circuit symbol for the device of Figure 1;

Figure 3 illustrates a bidirectional switch in accordance with the invention;

Figure 4 illustrates another device in accordance with the invention;

- 90 Figure 5 illustrates another device in accordance with the invention; and

Figure 6 illustrates another device in accordance with the invention;

- 95 Figure 7 illustrates another device in accordance with the invention;

Figure 8 is a plan view of the device of Figure 7.

- Referring now to Figure 1, there is illustrated a structure 10 comprising a support member 12 of n-conductivity type having a major surface 11 and a
- 100 monocrystalline semiconductor body 16 whose bulk is of p-conductivity type and which is separated from support member 12 by a dielectric layer 14.

- A localized anode region 18, which is of p+ type conductivity, is included in body 16 and has a
- 105 portion thereof that extends to surface 11. A localized gate region 20, which is of n+ conductivity, also is included in body 16 and has a portion thereof which extends to surface 11. A localized cathode region 24, which is of n+ type conductivity, is
- 110 included in body 16 and has a portion which extends to surface 11. A region 22, which is of p+ type conductivity and has a portion which extends to surface 11, surrounds region 24 and acts as a depletion layer punch-through shield. In addition it acts to inhibit inversion of the portions of body 16 at or near surface 11 between regions 20 and 24. Gate region 20 exists between anode region 18 and region 22 and is separated from both by bulk portions of body 16. The resistivities of regions 18, 20 and 24 are
- 115 low compared to that of the bulk portions of body 16. The resistivity of region 22 is intermediate that of cathode region 24 and the bulk portion of body 16.

- Electrodes 28, 30 and 32 are conductors which make low resistance contact to the surface portions of regions 18, 20, and 24, respectively. A dielectric layer 26 covers major surface 11 so as to isolate electrodes 28, 30 and 32 from all regions other than those intended to be electrically contacted. An electrode 36 provides a low resistance contact to
- 120 support 12 by way of a highly doped region 34 which
- 130

is of the same conductivity type as support 12.

The support 12 and the body 16 are each of silicon.

The support 12 which has been specified as *n* type, may equally well be *p* type. Each of electrodes 23, 30

5 and 32 advantageously overlaps the semiconductor region to which it makes low resistance contact. Electrode 32 also overlaps region 22. This overlapping, which is known as field plating, facilitates high voltage operation because it increases the voltage at 10 which breakdown occurs. Dielectric layer 14 is silicon dioxide and electrodes 28, 30, 32 and 36 are all aluminium. Conductivities complementary to those described may be used.

A plurality of separate bodies 16 can be formed in 15 a common support 12 to provide a plurality of switches. Significantly, planar processing techniques can be used to fabricate many devices as an integrated circuit on a common surface.

Structure 10 is typically operated as a switch 20 which has a low impedance path between anode region 18 and cathode region 24 when in the ON (conducting) state and has a high impedance between the said two regions when in the OFF (blocking) state. The potential applied to gate region 25 20 determines the state of the switch. Conduction between anode region 18 and cathode region 24 occurs if the potential of gate region 20 is below that of the potential of anode region 18 and cathode region 24. During the ON state holes are injected into 30 body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons can be in sufficient numbers to form a plasma which conductivity modulates body 16. This reduces the resistance of body 16 so that the 35 resistance between anode region 18 and cathode region 24 is low when structure 10 is operating in the ON state. This type of operation is denoted as dual carrier injection. The type of structure described herein is denoted as a gated diode switch (GDS).

40 Region 22 helps limit the punch-through of a depletion layer formed during operation between gate region 20 and cathode region 24 and helps inhibit formation of a surface inversion layer between these two regions. This permits closer spacing of gate region 20 and cathode region 24 and 45 results in a relatively low resistance between anode region 18 and cathode regions 22 during the ON state.

Substrate 12 is typically held at the most positive 50 potential level available. Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of gate region 20 is sufficiently more positive than that of anode region 18 and cathode region 24. The amount of excess positive 55 potential needed to inhibit or cut off conduction depends on the geometry and impurity concentration (doping) levels of structure 10. This positive gate potential causes the portion of body 16 between gate region 20 and dielectric layer 14 to be depleted of 60 current carrier so that the potential of this portion of body 16 is more positive than that of anode region 18 and cathode region 24. This positive potential barrier inhibits the conduction of holes from anode region 18 to cathode region 24. It essentially pinches 65 off body 16 against dielectric layer 14 in the bulk

portion between gate region 20 and dielectric layer 14. It also serves to collect electrons emitted at cathode region 24 before they can reach anode region 18.

70 During the ON state of structure 10, the junction diode comprising body 16 and region 20 becomes forward-biased. Current limiting means (not illustrated) are preferably included to limit the conduction through the forward-biased diode.

75 A proposed electrical symbol adopted for this type of switch is illustrated in Figure 2. The anode, gate, and cathode electrodes of the GDS are denoted as terminals 28, 30, and 32, respectively.

One embodiment of structure 10 has been fabricated with the following design. Support member 12 80 is an *n* type silicon substrate, 0.457 to 0.559 mm. thick, with an impurity concentration of approximately 2×10^{13} impurities/cm³, and has a resistivity greater than 100 ohm-centimetres. Dielectric layer 14 85 is a silicon dioxide layer 14 that is 2 to 4 microns thick. Body 16 is typically 30 to 50 microns thick, approximately 430 microns long, 300 microns wide, and is of *p* type conductivity with an impurity concentration in the range of approximately 5×10^{13} 90 to 9×10^{13} impurities/cm³. Anode region 18 is of *p*+ type conductivity, is typically 2 to 4 microns thick, 44 microns wide, 52 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 28 is typically aluminum, with a thickness 95 of 1½ microns, a width of 84 microns, and a length of 105 microns. Region 20 is of *n*+ type conductivity and is typically 2 to 4 microns thick, 15 microns wide, 300 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 30 is 100 aluminum, 1½ microns thick, 50 microns wide, and 210 microns long. The spacing between adjacent edges of electrodes 28 and 30 and between adjacent edges of electrodes 30 and 32 is typically 40 microns in both cases. Region 22 is *p* type conductivity and is 105 typically 3-6 microns thick, 64 microns wide, 60 microns long, and has an impurity concentration of approximately 10^{17} to 10^{18} impurities/cm³. Cathode region 24 is *n*+ type conductivity and is typically 2 110 microns thick, 48 microns wide, 44 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 32 is aluminum, 1½ microns thick, 104 microns wide, and 104 microns long. The spacing between the ends of regions 18 and 22 and the respective ends of region 16 is 115 typically 55 microns. Region 34 is *n*+ type conductivity and is typically 2 microns thick, 26 microns wide, 26 microns long, and has an impurity concentration of 10^{19} impurities/cm³. Electrode 36 is aluminum which is 1½ microns thick, 36 microns wide, and 26 120 microns long.

Structure 10, using the parameters denoted above, has been operated as a gated diode switch (GDS) with 500 volts between anode and cathode. A layer of silicon nitride (not illustrated) was deposited by 125 chemical vapor deposition on top of silicon dioxide layer 26 to provide a sodium barrier. Electrodes 28, 30, 32, and 36 were then formed and thereafter a coating of radio frequency plasma deposited silicon nitride (not illustrated) was applied to the entire 130 surface of structure 10 except where electrical

contact is made. The layers of silicon nitride serve to help prevent high voltage breakdown in the air between adjacent electrodes.

Typically the anode had +250 volts applied thereto, the cathode had -250 volts applied thereto; and substrate 12 had +280 volts applied thereto. The -250 volts can also be applied to the anode and the +250 volts applied to the cathode. Thus, structure 10 bilaterally blocks voltage between anode and cathode. A potential of +280 volts applied to gate conductor 30 interrupted (broke) 350 mA of current flow between anode region 15 and cathode region 24. The ON resistance of the GDS with 100 mA flowing between anode and cathode is approximately 15 ohms and the voltage drop between anode and cathode is typically 2.2 volts.

Referring now to Figure 3, there is illustrated a bidirectional switch combination comprising two GDSs (GDS and GDSa) in accordance with the present invention with electrode 28 (the anode electrode of GDS) electrically connected to electrode 32a (the cathode electrode of GDSa), and electrode 32 (the cathode electrode of GDS) electrically connected to electrode 28a (the anode electrode of GDSa). This switch combination is capable of conducting signals from electrodes 28 and 32a to electrodes 28a and 32 or vice versa. The bilateral blocking characteristic of structure 10 facilitates this bilateral switch combination. Two separate bodies 16 can be formed in a common support 12 and the appropriate electrical connections can be made to form the above-described bidirectional switch. A plurality of separate bodies 16 can be formed in a common support 12 to form an array of switches.

Referring now to Figure 4, there is illustrated a structure 410 which is very similar to structure 10 with all components essentially identical or very similar to those of structure 10 being denoted by the same reference number with the addition of a "4" at the beginning. The basic difference between structures 410 and 10 is the elimination from structure 410 of semiconductor region 22 of Figure 1. Appropriately increasing the spacing of region 424 from region 420 provides sufficient protection against depletion layer punch-through to region 424 and permits the use of structure 410 as a high voltage switch.

Referring now to Figure 5, there is illustrated a structure 510 which is very similar to structure 10 and all components of which are essentially the same or very similar are denoted by the same reference number with the addition of a "5" at the beginning. The main difference between structure 510 and structure 10 is the use of a semiconductor guard ring region 540 which encircles cathode region 524. The dashed line portion of guard ring 540 illustrates that it can be extended so as to contact cathode region 524. The combination of region 522 and guard ring 540 provides protection against inversion of portions of region 516 at or near surface 511 particularly between gate region 520 and cathode region 524 and provides protection against depletion layer punch-through to cathode region 524. Guard ring 540 is of the same conductivity as region 522, but is of lower resistivity. This type of dual protection

structure encircling cathode region 524 is the preferred protection structure.

Referring to Figure 6 there is shown another embodiment with reference numbers in the 600 series corresponding to Figure 1, in which the semiconductor body 616 is isolated from the dielectric layer 614 by an intervening semiconductor layer 638 having a conductivity type opposite that of semiconductor body 616. Electrodes 628, 630, and 632 are conductors which make low resistance contact to the surface portions of regions 618, 620, and 624, respectively. A dielectric layer 26 covers major surface 611 so as to isolate electrodes 628, 630, and 632 from all regions other than those intended to be electrically contacted. Electrode 630 makes electrical contact to region 638 at surface 611 in the rear or front of body 616 (not illustrated).

Layer 638 may exist only on the lower portion of body 16 as shown by region 638a. With such modification an appropriate diffused or ion implanted region(s) (not illustrated) is formed between surface 611 and modified layer 638a. Electrode 630 extends to make electrical contact to this region at surface 611.

Layer 638 serves to isolate body 616 from the properties of dielectric layer 614 and thus aids the fabrication process in that the tolerances in the formation of the dielectric layer 14 can be relaxed somewhat. This increases fabrication yields and reduces costs. In addition layer 638 serves as a lower gate region which aids in reducing the magnitude of the gate potential needed to inhibit or cut off conduction between the anode 618 and cathode 624 regions. The use of only portion 638a of layer 638 serves to isolate body 616 from region 614 in the portion of body 616 which is under region 620. This particular portion of body 616 is the most critical portion since body 616 is essentially "pinched off" in this portion when structure 610 is operated in the OFF state.

Layer 638a does not provide complete isolation from dielectric layer 14, but it reduces the gate potential needed for turn-off while essentially not affecting the breakdown voltage of the structure. Layer 638 provides complete isolation from dielectric layer 614 but does reduce the breakdown voltage of the structure somewhat. If layer 638 is used, then generally body 616 is increased in thickness to maintain breakdown voltages at preselected levels.

Layer 638 need not necessarily be directly connected to electrode 630. Because positive charge resides in layer 626, a surface inversion layer will form near the surface 611 of body 616 between layer 638 and gate region 620 which may electrically couple the two. Even without said positive charge it is believed that, owing to punch-through, electrode 630 and layer 638 will be electrically coupled.

Referring to Figures 7 and 8, there is shown still another embodiment, having reference numbers in the 700 series corresponding to Figure 1, in which the gate region 720 is not located between the anode region 718 and the cathode region 724. Structure 710 is designed such that anode region 18 and cathode region 724 can be spaced relatively closely to each

other in order to reduce the resistance between the two during the ON (conducting) state. A conductor 738, is located on top of layer 726 between electrodes 728 and 732. Conductor 738 is electrically coupled to electrode 730, and it helps reduce the magnitude of the gate voltage necessary in the operation of structure 710, but is not essential for operation.

One embodiment of structure 710 has been fabricated with the following design. Semiconductor wafer (substrate) 712 is an n-type silicon substrate, 457 to 559 microns thick, with an impurity concentration of approximately 5×10^{13} impurities/cm³, and is 100 ohm-centrimetre type material. Dielectric layer 714 is silicon dioxide that is typically 2 to 4 microns thick. Body 716 is typically 30 to 40 microns thick, approximately 430 microns long, 170 microns wide, and is of p-type conductivity with an impurity concentration of approximately 5×10^{13} to 9×10^{13} impurities/cm³. Anode region 718 is of p+ type conductivity, is typically 2 to 4 microns thick, 28 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 728 is aluminum, with a thickness of $1\frac{1}{2}$ microns, a width of 55 microns, and a length of 95 microns. Gate region 720 is of n+ type conductivity, is typically 2 to 4 microns thick, 38 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 730 is aluminum with a thickness of $1\frac{1}{2}$ microns, a width of 76 microns, and a length of 95 microns. The spacing between adjacent edges of electrodes 728 and 732 is typically 40 microns (with no conductor 738) and the spacing between adjacent edges of electrodes 728 and 730 is typically 40 microns. Region 722 is of p type conductivity and is typically 3.5 microns thick, 44 microns wide, 44 microns long, and has a surface impurity concentration of approximately 10^{18} impurities/cm³. Cathode region 724 is of n+ type conductivity and is typically 2 microns thick, 30 microns wide, 30 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 32 is aluminum, $1\frac{1}{2}$ microns thick, 82 microns wide, and 82 microns long. The spacing between the ends of electrodes 728 and 732 and the respective ends of p-type body 716 is 50 microns. Conductor region 738, which is aluminium, is spaced 30 microns apart from electrodes 728 and 732 and is 10 microns wide, $1\frac{1}{2}$ microns thick, and 75 microns long. Conductor region 738 makes electrical contact to electrode 730 in the front or rear of region 16. It can be appreciated that with this configuration the cathode to anode spacing is significantly reduced.

Structure 710, using the parameters denoted above, has been operated as a gated diode switch with 400 volts between anode and cathode. The anode had +200 volts applied thereto and the cathode has -200 volts applied thereto. As before, the -200 volts can also be applied to the anode and the +200 volts can be applied to the cathode since the device exhibits bilateral voltage blocking. With conductor region 738 present, a potential of +210 volts was found sufficient to break 1 mA of current flow between anode and cathode. It is estimated that this voltage would need to be 20 volts higher if

conductor 738 were eliminated. The ON resistance of the gated diode switch with 100 mA flowing between anode and cathode was approximately 10-12 ohms and the voltage drop between anode and cathode was typically 2.2 volts. A layer of silicon nitride (not illustrated) was deposited by chemical vapour deposition on top of silicon dioxide layer 26 to act as a sodium barrier. Electrodes 728, 730, 732, and 736 were then formed and a coating of radio frequency plasma deposited silicon nitride (not illustrated) was applied to the entire surface of structure 710 to help prevent high voltage breakdown in the air between adjacent electrodes.

As in Figure 5, a guard ring either surrounding or enclosing and contacting the cathode region 724 can be used, or, as in Figure 4, region 722 can be eliminated if the anode cathode spacing is sufficient. Gate region 720 can be located to the right of cathode region 724, as indicated by the dashed lines of Figure 7, or to the front or rear of semiconductor body 716 as indicated by the dashed line of Figure 8. Gate region 720 can be separated from the dielectric layer 714 or, as illustrated by the dashed lines of Figure 7, extend so as to contact dielectric layer 714.

Various modifications of the embodiments described will be apparent to a person skilled in the art to which this invention relates. For example, the support members 12 etc., can alternatively be p-type conductivity silicon, gallium arsenide, sapphire, a conductor, or an electrically inactive material. If the support members are of electrically inactive materials then the dielectric layers 14 etc. can be eliminated. Furthermore, bodies 16 etc. can be fabricated as air-insulated structures. This allows for the elimination of support members 12 etc. and dielectric layers 14 etc. The electrodes can be doped polysilicon, gold, titanium, or other types of conductors. Further, the impurity concentration levels, spacings between different regions, and other dimensions of the regions can be adjusted to allow significantly different operating voltages and current than are described. Other types of dielectric materials, such as silicon nitride, can be substituted for silicon dioxide. The conductivity types of all semiconductor regions can be reversed provided the voltage polarities are appropriately changed.

CLAIMS

1. A solid-state switching device comprising: a semiconductor body whose bulk is of one conductivity type and which has a major surface; a localized first region which is of the one conductivity type; a localized second region which is of the opposite conductivity type; the localized first and second regions being of relatively low resistivity as compared to the bulk of the semiconductor body and being separated by portions of the bulk of the semiconductor body; each of the first and second regions having a portion that forms part of the major surface; a gate region of the said opposite conductivity type which has a low resistivity as compared to the bulk of the semiconductor body and is separated from the first and second regions by portions of the bulk of the semiconductor body; the structure being



other in order to reduce the resistance between the two during the ON (conducting) state. A conductor 738, is located on top of layer 726 between electrodes 728 and 732. Conductor 738 is electrically coupled to electrode 730, and it helps reduce the magnitude of the gate voltage necessary in the operation of structure 710, but is not essential for operation.

One embodiment of structure 710 has been fabricated with the following design. Semiconductor wafer (substrate) 712 is an n-type silicon substrate, 457 to 559 microns thick, with an impurity concentration of approximately 5×10^{13} impurities/cm³, and is 100 ohm-centimetre type material. Dielectric layer 714 is silicon dioxide that is typically 2 to 4 microns thick. Body 716 is typically 30 to 40 microns thick, approximately 430 microns long, 170 microns wide, and is of p-type conductivity with an impurity concentration of approximately 5×10^{13} to 9×10^{13} impurities/cm³. Anode region 718 is of p+ type conductivity, is typically 2 to 4 microns thick, 28 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 728 is aluminum, with a thickness of $1\frac{1}{2}$ microns, a width of 55 microns, and a length of 95 microns. Gate region 720 is of n+ type conductivity, is typically 2 to 4 microns thick, 38 microns wide, 55 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 730 is aluminum with a thickness of $1\frac{1}{2}$ microns, a width of 76 microns, and a length of 95 microns. The spacing between adjacent edges of electrodes 728 and 732 is typically 40 microns (with no conductor 738) and the spacing between adjacent edges of electrodes 728 and 730 is typically 40 microns. Region 722 is of p type conductivity and is typically 3.5 microns thick, 44 microns wide, 44 microns long, and has a surface impurity concentration of approximately 10^{18} impurities/cm³. Cathode region 724 is of n+ type conductivity and is typically 2 microns thick, 30 microns wide, 30 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³. Electrode 732 is aluminum, $1\frac{1}{2}$ microns thick, 82 microns wide, and 82 microns long. The spacing between the ends of electrodes 728 and 732 and the respective ends of p-type body 716 is 50 microns. Conductor region 738, which is aluminium, is spaced 30 microns apart from electrodes 728 and 732 and is 10 microns wide, $1\frac{1}{2}$ microns thick, and 75 microns long. Conductor region 738 makes electrical contact to electrode 730 in the front or rear of region 16. It can be appreciated that with this configuration the cathode to anode spacing is significantly reduced.

Structure 710, using the parameters denoted above, has been operated as a gated diode switch with 400 volts between anode and cathode. The anode had +200 volts applied thereto and the cathode has -200 volts applied thereto. As before, the -200 volts can also be applied to the anode and the +200 volts can be applied to the cathode since the device exhibits bilateral voltage blocking. With conductor region 738 present, a potential of +210 volts was found sufficient to break 1 mA of current flow between anode and cathode. It is estimated that this voltage would need to be 20 volts higher if

conductor 738 were eliminated. The ON resistance of the gated diode switch with 100 mA flowing between anode and cathode was approximately 10-12 ohms and the voltage drop between anode and cathode was typically 2.2 volts. A layer of silicon nitride (not illustrated) was deposited by chemical vapour deposition on top of silicon dioxide layer 26 to act as a sodium barrier. Electrodes 728, 730, 732, and 736 were then formed and a coating of radio frequency plasma deposited silicon nitride (not illustrated) was applied to the entire surface of structure 710 to help prevent high voltage breakdown in the air between adjacent electrodes.

As in Figure 5, a guard ring either surrounding or enclosing and contacting the cathode region 724 can be used, or, as in Figure 4, region 722 can be eliminated if the anode cathode spacing is sufficient. Gate region 720 can be located to the right of cathode region 724, as indicated by the dashed lines of Figure 7, or to the front or rear of semiconductor body 716 as indicated by the dashed line of Figure 8. Gate region 720 can be separated from the dielectric layer 714 or, as illustrated by the dashed lines of Figure 7, extend so as to contact dielectric layer 714.

Various modifications of the embodiments described will be apparent to a person skilled in the art to which this invention relates. For example, the support members 12 etc., can alternatively be p-type conductivity silicon, gallium arsenide, sapphire, a conductor, or an electrically inactive material. If the support members are of electrically inactive materials then the dielectric layers 14 etc. can be eliminated. Furthermore, bodies 16 etc. can be fabricated as air-insulated structures. This allows for the elimination of support members 12 etc. and dielectric layers 14 etc. The electrodes can be doped polysilicon, gold, titanium, or other types of conductors. Further, the impurity concentration levels, spacings between different regions, and other dimensions of the regions can be adjusted to allow significantly different operating voltages and current than are described. Other types of dielectric materials, such as silicon nitride, can be substituted for silicon dioxide. The conductivity types of all semiconductor regions can be reversed provided the voltage polarities are appropriately changed.

CLAIMS

1. A solid-state switching device comprising: a semiconductor body whose bulk is of one conductivity type and which has a major surface; a localized first region which is of the one conductivity type; a localized second region which is of the opposite conductivity type; the localized first and second regions being of relatively low resistivity as compared to the bulk of the semiconductor body and being separated by portions of the bulk of the semiconductor body; each of the first and second regions having a portion that forms part of the major surface; a gate region of the said opposite conductivity type which has a low resistivity as compared to the bulk of the semiconductor body and is separated from the first and second regions by portions of the bulk of the semiconductor body; the structure being



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adapted to selectively facilitate current flow between the first and second regions or by application of a suitable potential to the gate region, to divert a sufficient portion of the current into the gate region

5 so as to substantially interrupt the current flow between the first and second regions; the structure being also adapted to substantially inhibit current from flowing between the first and second regions while the said suitable potential is applied to the gate
10 region.

2. A device as claimed in claim 1 wherein the gate region is located between the first and second regions.

3. A device as claimed in claim 1 wherein the first
15 and second regions are closely adjacent and the gate region is not between them.

4. A device as claimed in claim 3 including a conductor electrically coupled to the gate region overlying but insulated from that part of the bulk
20 portion of the body which lies between the first region and the second region.

5. A device as claimed in any of the preceding claims including a shield region of the same conductivity type as but lower of resistivity than the bulk
25 portion and surrounding the second region.

6. A device as claimed in claim 5 wherein the resistivity of the shield region is greater than that of the second region.

7. A device as claimed in claim 5 or claim 6
30 including an annular guard region of the same conductivity type as but of lower resistivity than the shield region and laterally surrounding the second region at the said major surface.

8. A device as claimed in any of the preceding
35 claims wherein the body is located in a support member and insulated therefrom by a dielectric layer.

9. A device as claimed in claim 8 including a layer region of the said opposite conductivity type
40 between the bulk portion of the body and the dielectric layer and electrically coupled to the gate region.

10. A device as claimed in claim 9 wherein the layer region is located in only that part of the body
45 which is between the gate region and the dielectric layer.

11. A device as claimed in claim 9 wherein the layer region separates the bulk portion from the dielectric layer substantially completely.

50 12. A bidirectional switch comprising a pair of devices as claimed in any of the preceding claims, the gate regions of the devices being connected together and the first region of each device being connected to the second region of the other device.

55 13. A plurality of devices as claimed in any of claims 8 to 11 having a common support member.

14. A plurality as claimed in claim 13, including a pair of devices constituting a switch as claimed in claim 12.

60 15. A switch as claimed in any of claims 8 to 11 or a plurality as claimed in claim 13 or claim 14 wherein the support member is of a semiconductor material and including an ohmic contact to the support member.

65 16. A device substantially as herein described

with reference to any of Figures 1 and 3 to 8 of the accompanying drawings.

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