

CLAIMS

1. A data processing method, comprising:

receiving, by a processing core, a first synchronization signal;

determining, by the processing core, according to the first synchronization signal, a first storage area used by a self-task of the processing core and a second storage area used by a non-self-task of the processing core;

wherein the first storage area differs from the second storage area such that the reading and writing of the first storage area and the reading and writing of the second storage area are independent of each other;

accessing the first storage area to execute the self-task and accessing the second storage area to execute the non-self-task by the processing core in a first synchronization cycle determined by the first synchronization signal;

receiving, by the processor core, a second synchronization signal;

determining, by the processing core, according to the second synchronization signal, the first storage area used by the non-self-task of the processing core and the second storage area used by the self-task of the processing core; and

accessing the first storage area to execute the non-self-task and accessing the second storage area to execute the self-task by the processing core in a second synchronization cycle determined by the second synchronization signal.

2. The data processing method according to claim 1, wherein the first storage area comprises a plurality of first memories; the self-task comprises a computational task and a sending task; and in the first synchronization cycle,

the computational task and the sending task use a same first memory, or

the computational task and the sending task use different first memories.

3. The data processing method according to claim 2, wherein

the self-task comprises a plurality of the sending tasks, wherein each of the sending tasks corresponds to a different or same target processing core, and each of the sending tasks is marked with a storage area of the target processing core.

4. The data processing method according to any one of claims 1-3, wherein the second storage area comprises a plurality of second memories; the non-self-task comprises more than one receiving tasks, wherein different receiving tasks use different second memories in the first synchronization cycle.

5. The data processing method according to claim 4, wherein the different receiving tasks correspond to different source processing cores or a same source processing core.

6. The data processing method according to any one of claims 1-5, further comprising, before receiving, by the processing core, the first or second synchronization signal:

receiving, by the processing core, configuration information, the configuration information comprising, in a synchronization cycle determined by each synchronization signal, the self-task of the processing core, the non-self-task of the processing core and the respective first and second storage areas used by the self-task and non-self-task.

7. A data processing method, comprising:

receiving, by a processing core, a first synchronization signal;

executing, by the processing core, a first computational task and a first receiving task in a first synchronization cycle determined by the first synchronization signal, wherein data of the first receiving task is from a source processing core;

accessing, by the processing core, a first storage area to execute the first computational task;

receiving the data of the first receiving task transmitted from the source processing core and writing the data into a second storage area by the processing core;

receiving, by the processing core, a second synchronization signal;

executing, by the processing core, a second computational task and a second receiving task in a second synchronization cycle determined by the second synchronization signal, wherein data of the second receiving task is from a same or different source processing core;

accessing, by the processing core, the second storage area to execute the second computational task; and

receiving the data of the second receiving task transmitted from the same or different source processing core and writing the data into the first storage area by the processing core;

wherein the first storage area differs from the second storage area such that the reading and writing of the first storage area and the reading and writing of the second storage area are independent of each other.

8. The data processing method according to claim 7, wherein

the data of the first receiving task is from a plurality of the source processing cores, and the processing core has a plurality of second storage areas corresponding to different source processing cores or a same source processing core.

9. A data processing apparatus, comprising:

a synchronization signal receiving module for receiving a first synchronization signal and a second synchronization signal by a processing core;

a storage area determining module for determining a first storage area used by a self-task of the processing core and a second storage area used by a non-self-task of the processing core by the processing core, according to the first synchronization signal;

wherein the first storage area differs from the second storage area such that the reading and writing of the first storage area and the reading and writing of the second storage area are independent of each other;

a task executing module for accessing the first storage area to execute the self-task and accessing the second storage area to execute the non-self-task by the processing core in a first synchronization cycle determined by the first synchronization signal;

wherein the storage area determining module determines the first storage area used by the non-self-task of the processing core and the second storage area used by the self-task of the processing core by the processing core, according to the second synchronization signal; and the task executing module accesses the first storage area to execute the non-self-task and accesses the second storage area to execute the self-task by the processing core in a second synchronization cycle determined by the second synchronization signal.

10. A data processing apparatus, comprising:

a synchronization signal receiving module for receiving a first synchronization signal and a second synchronization signal by a processing core;

a task determining module for executing a first computational task and a first receiving task by the processing core in a first synchronization cycle determined by the first

synchronization signal, wherein data of the first receiving task is from a source processing core;

a computational task executing module for accessing a first storage area to execute the first computational task by the processing core; and

a receiving task executing module for receiving the data of the first receiving task transmitted from the source processing core and writing the data into a second storage area by the processing core;

wherein the task determining module executes a second computational task and a second receiving task by the processing core in a second synchronization cycle determined by the second synchronization signal, wherein data of the second receiving task is from a same or different source processing core;

the computational task executing module accesses the second storage area to execute the second computational task by the processing core;

the receiving task executing module receives the data of the second receiving task transmitted from the same or different source processing core and writing the data into the first storage area by the processing core;

wherein the first storage area differs from the second storage area such that the reading and writing of the first storage area and the reading and writing of the second storage area are independent of each other.

11. An electronic device, comprising:

a memory for storing computer-readable instructions; and

one or more processors for executing the computer-readable instructions, which, upon execution, cause the processors to implement a data processing method according to any one of claims 1-8.

12. A non-transitory computer-readable storage medium storing computer-readable instructions, which, upon execution by a computer, cause the computer to execute a data processing method according to any one of claims 1-8.

13. A computer program product, wherein the program comprises computer-readable instructions, which, upon execution by a computer, cause the computer to execute a data processing method according to any one of claims 1-8.