FIG. 1

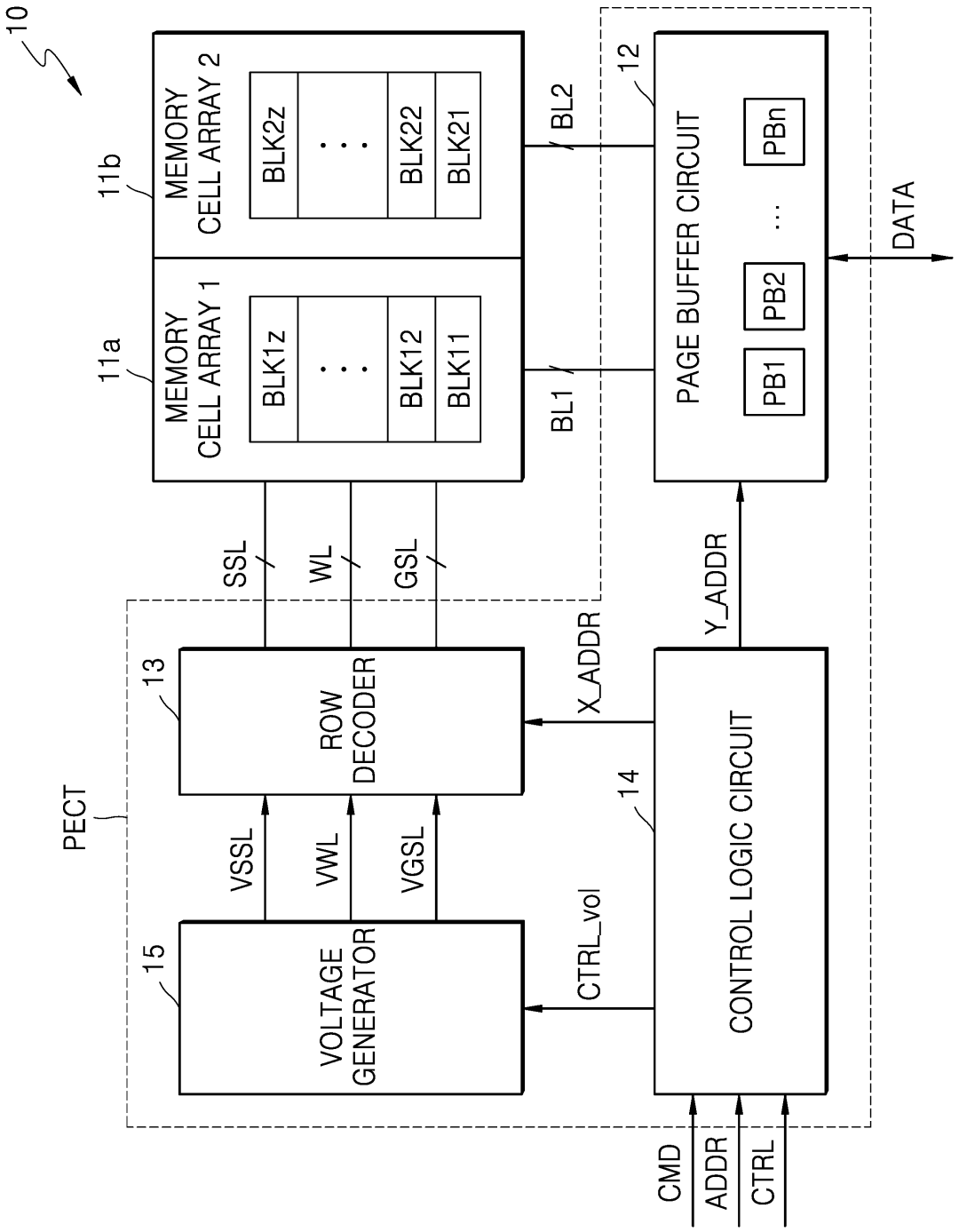

10
11b
MEMORY CELL ARRAY 2
BLK2z
BLK22
BLK21
11a
MEMORY CELL ARRAY 1
BLK1z
BLK12
BLK11
BL2
BL1
12
PAGE BUFFER CIRCUIT
PB1
PB2
PBn
DATA
SSL
WL
GSL
X_ADDR
Y_ADDR
PECT
13
ROW DECODER
VSSL
VWL
VGSL
14
CONTROL LOGIC CIRCUIT
CTRL_vol
15
VOLTAGE GENERATOR
CMD
ADDR
CTRL

FIG. 2

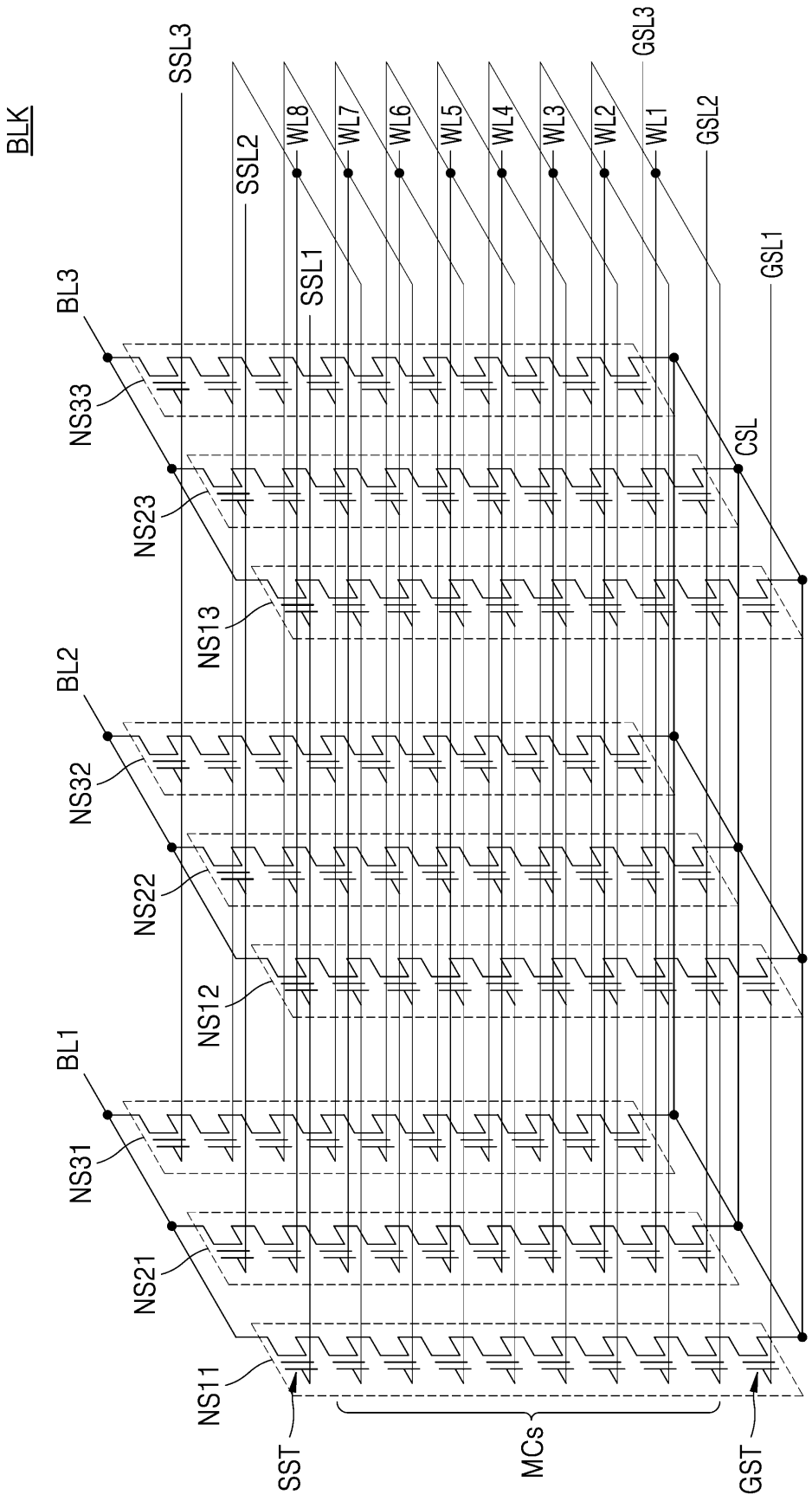

BLK
SSL3
SSL2
SSL1
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL3
GSL2
GSL1
CSL
BL3
BL2
BL1
NS33
NS23
NS13
NS32
NS22
NS12
NS31
NS21
NS11
SST
MCs
GST

FIG. 3A

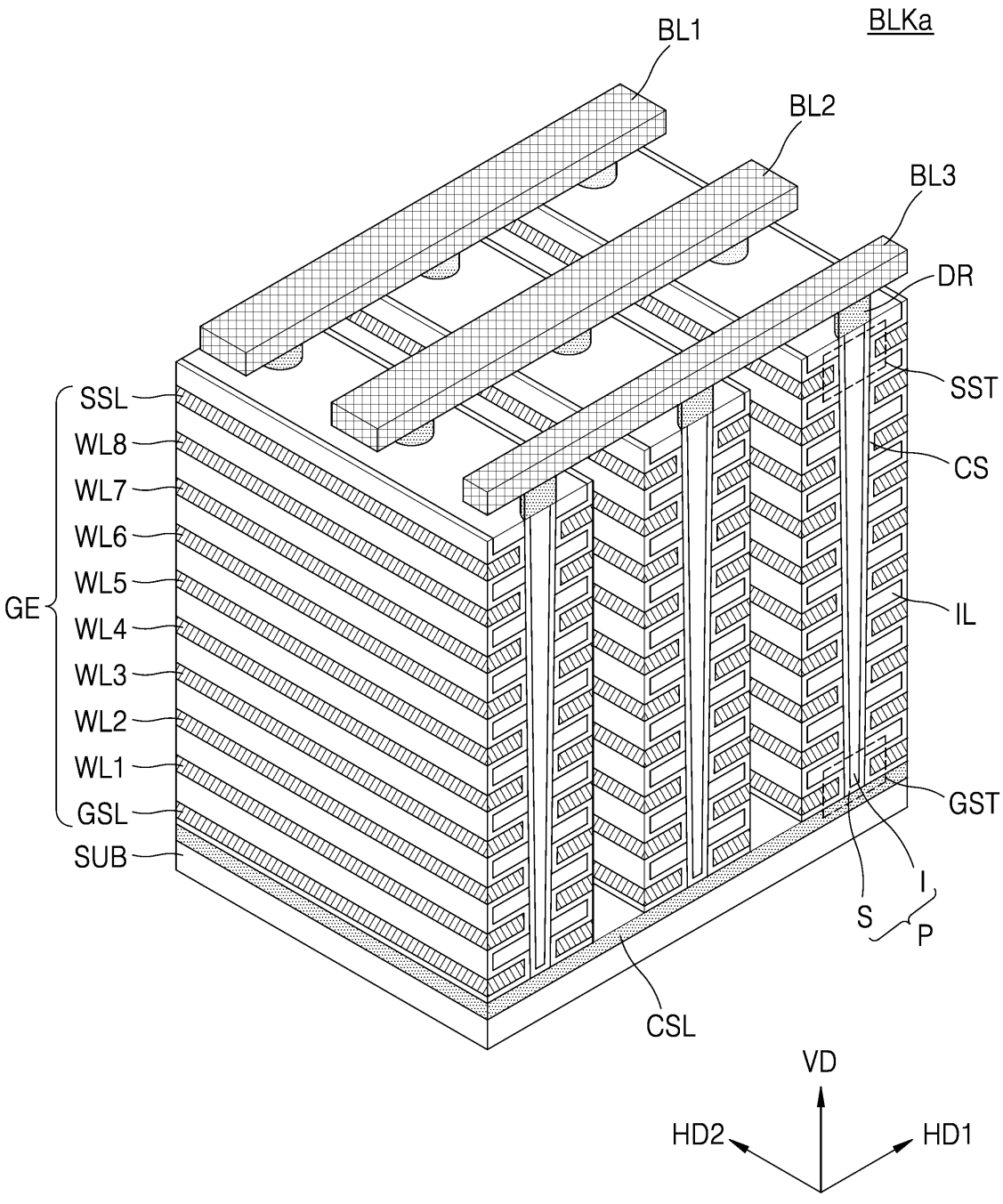

BLKa
BL1
BL2
BL3
DR
SST
CS
IL
GST
I
S
P
CSL
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
GE
SUB
VD
HD2
HD1

FIG. 3B

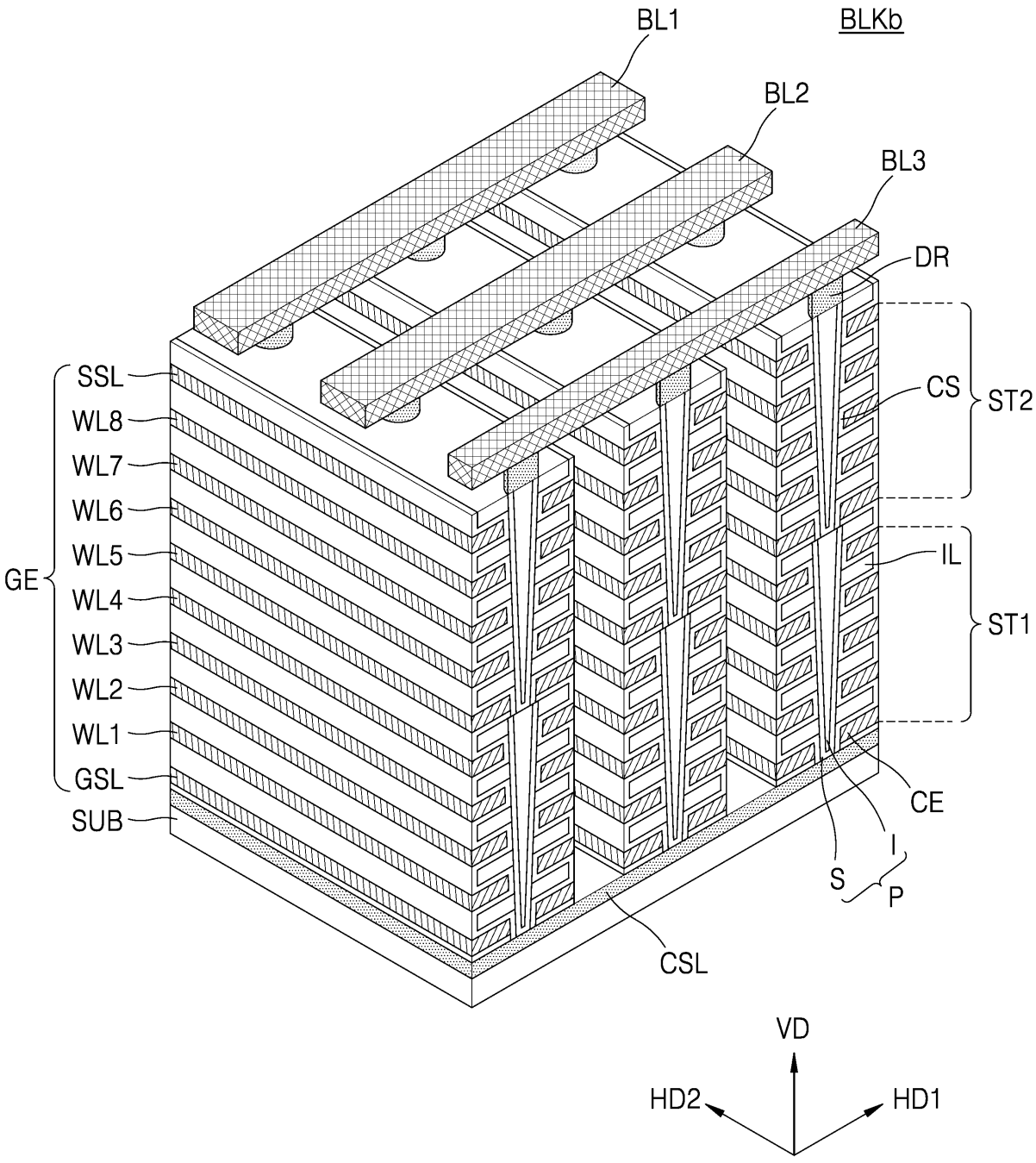

BL1
BLKb
BL2
BL3
DR
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
CS
ST2
IL
ST1
CE
I
S
P
CSL
VD
HD2
HD1

FIG. 4

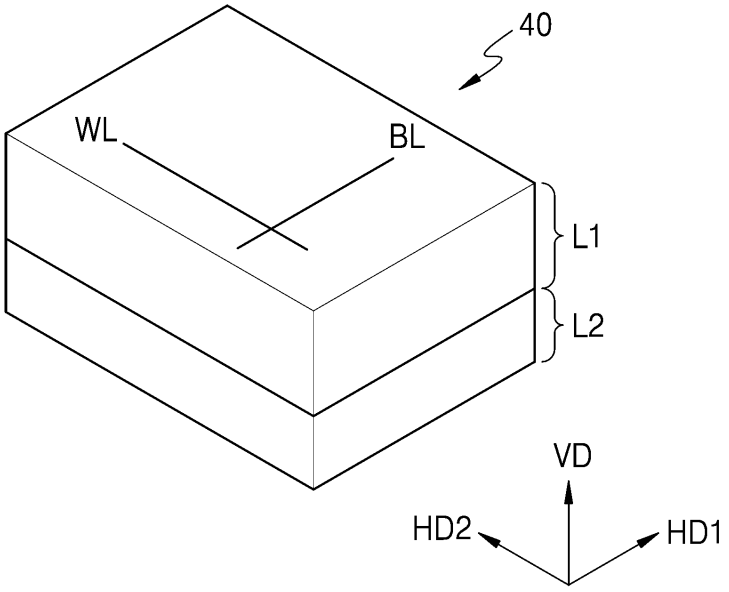


FIG. 5

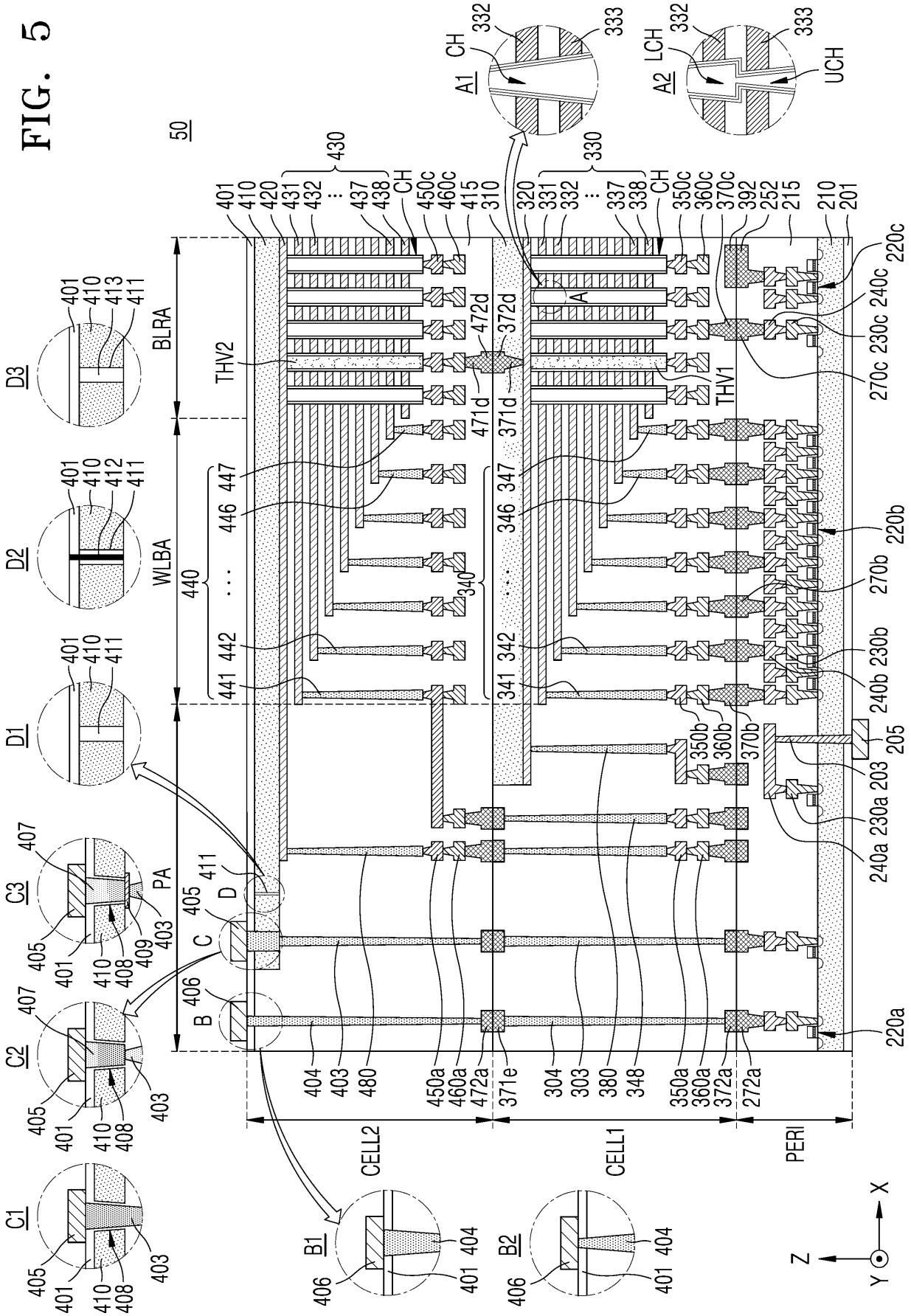

50
BLRA
WLBA
THV2
THV1
CELL2
CELL1
PERI
A1
A2
CH
LCH
UCH
A
B
C
D
PA
B1
B2
C1
C2
C3
D1
D2
D3
X
Y
Z

FIG. 6

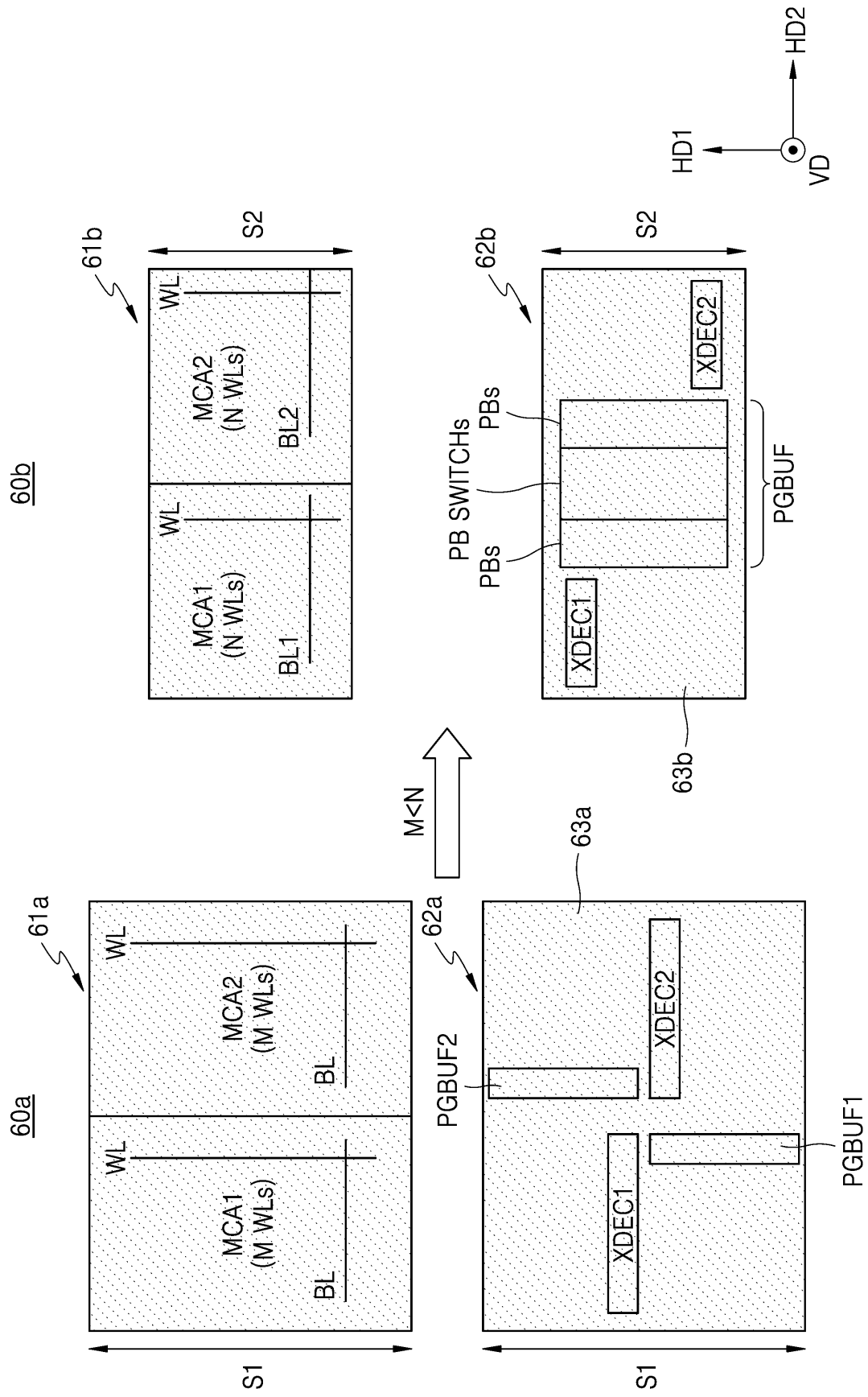

60a
61a
WL
MCA2
(M WLs)
BL
WL
MCA1
(M WLs)
BL
S1
60b
61b
WL
MCA2
(N WLs)
BL2
WL
MCA1
(N WLs)
BL1
S2
M<N
62a
63a
PGBUF2
XDEC2
XDEC1
PGBUF1
S1
62b
63b
PB SWITCHs
PBs
PBs
XDEC2
XDEC1
PGBUF
S2
HD1
HD2
VD

FIG. 7A

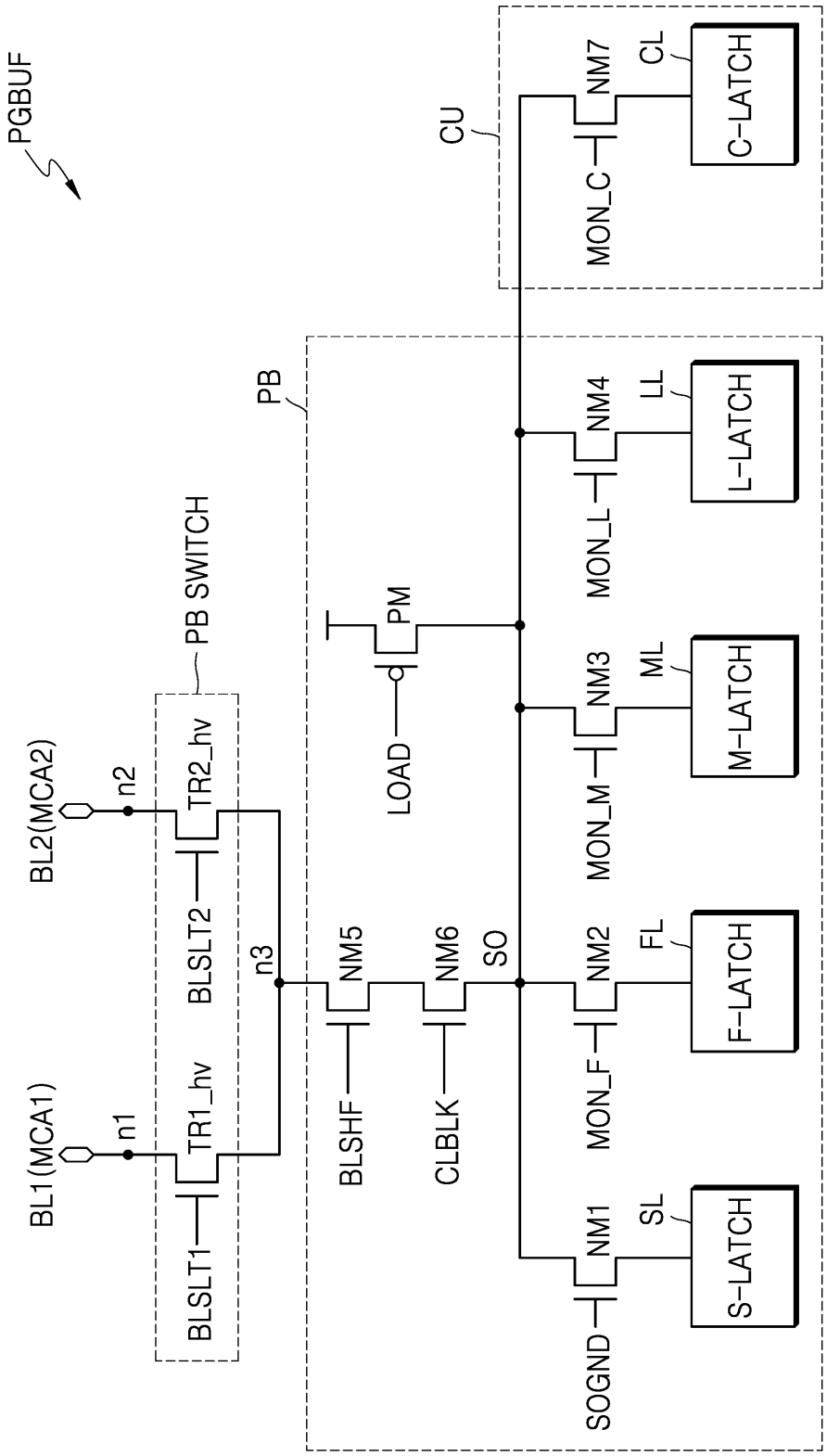

PGBUF
BL1(MCA1)
BL2(MCA2)
n1
n2
n3
TR1_hv
TR2_hv
BLSLT1
BLSLT2
PB SWITCH
PB
CU
PM
LOAD
BLSHF
CLBLK
SO
NM1
NM2
NM3
NM4
NM5
NM6
NM7
MON_C
MON_L
MON_M
MON_F
SOGND
SL
FL
ML
LL
CL
S-LATCH
F-LATCH
M-LATCH
L-LATCH
C-LATCH

FIG. 7B

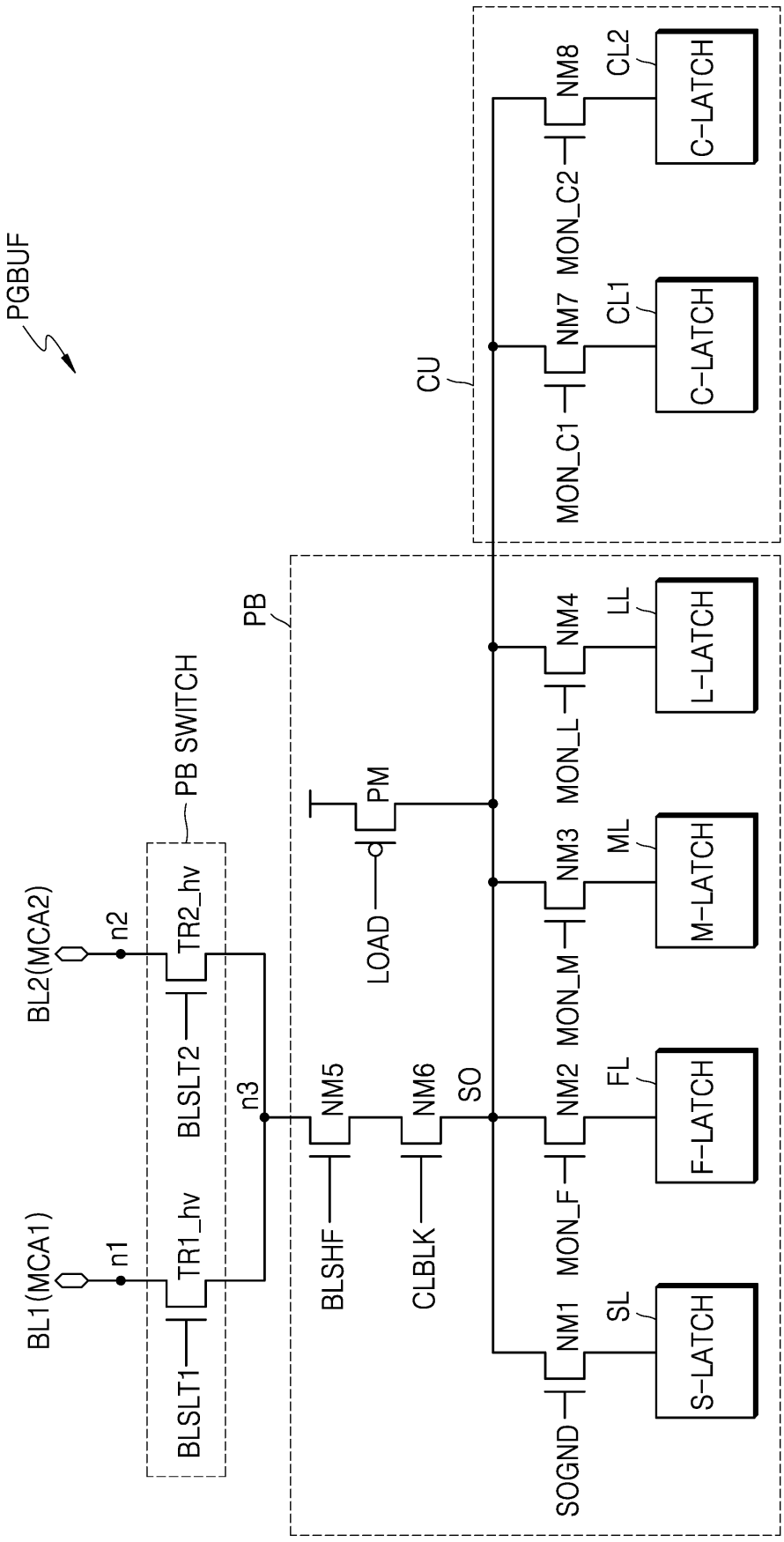

PGBUF
BL1(MCA1)
BL2(MCA2)
n1
n2
n3
TR1_hv
TR2_hv
BLSLT1
BLSLT2
PB SWITCH
PB
CU
BLSHF
CLBLK
LOAD
PM
NM1
NM2
NM3
NM4
NM5
NM6
NM7
NM8
MON_F
MON_M
MON_L
MON_C1
MON_C2
SOGND
SO
SL
FL
ML
LL
CL1
CL2
S-LATCH
F-LATCH
M-LATCH
L-LATCH
C-LATCH
C-LATCH

FIG. 7C

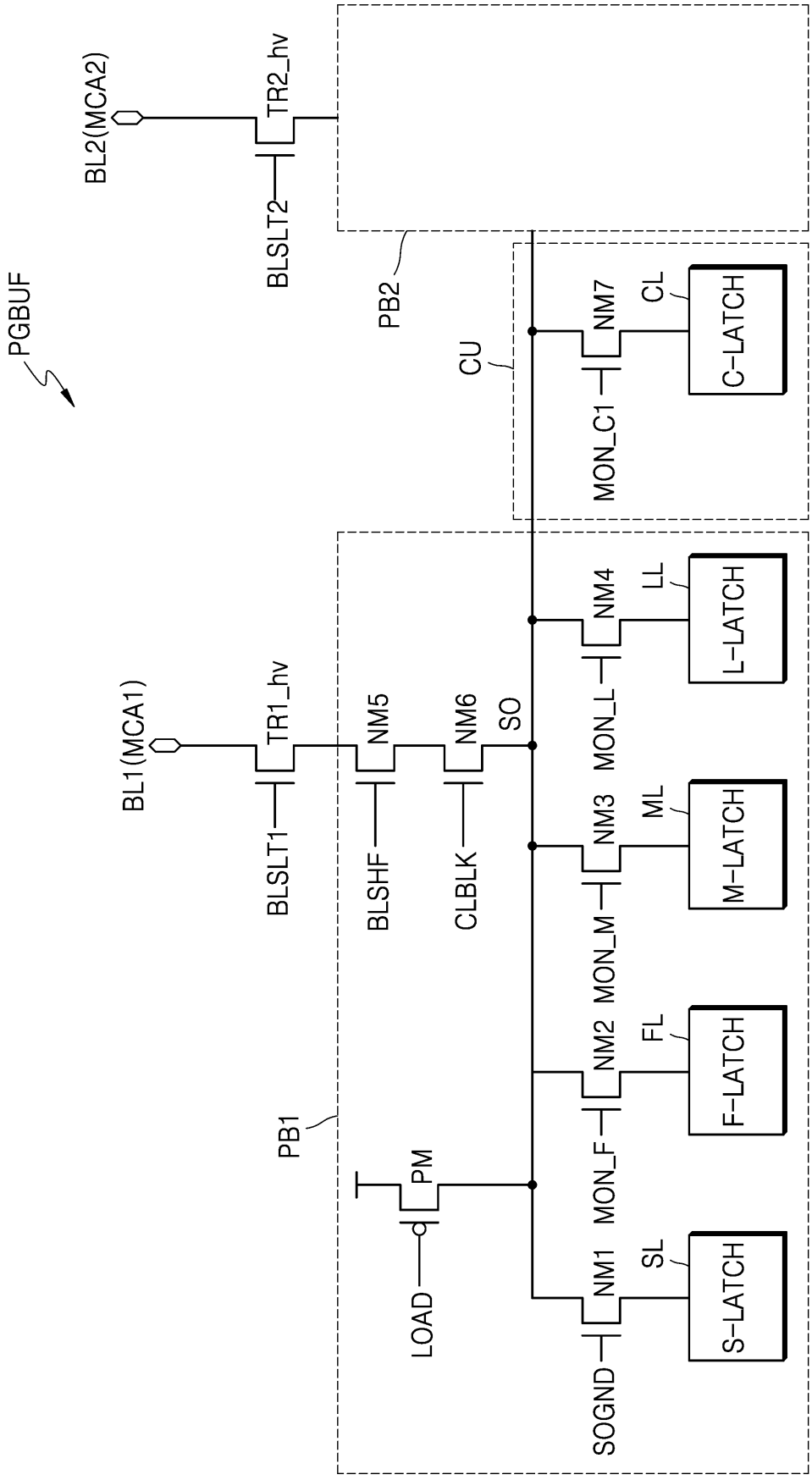

PGBUF
BL2(MCA2)
TR2_hv
BLSLT2
PB2
CU
NM7
CL
C-LATCH
MON_C1
BL1(MCA1)
TR1_hv
BLSLT1
NM5
BLSHF
NM6
CLBLK
SO
NM4
LL
L-LATCH
MON_L
NM3
ML
M-LATCH
MON_M
NM2
FL
F-LATCH
MON_F
NM1
SL
S-LATCH
SOGND
PB1
PM
LOAD

FIG. 8

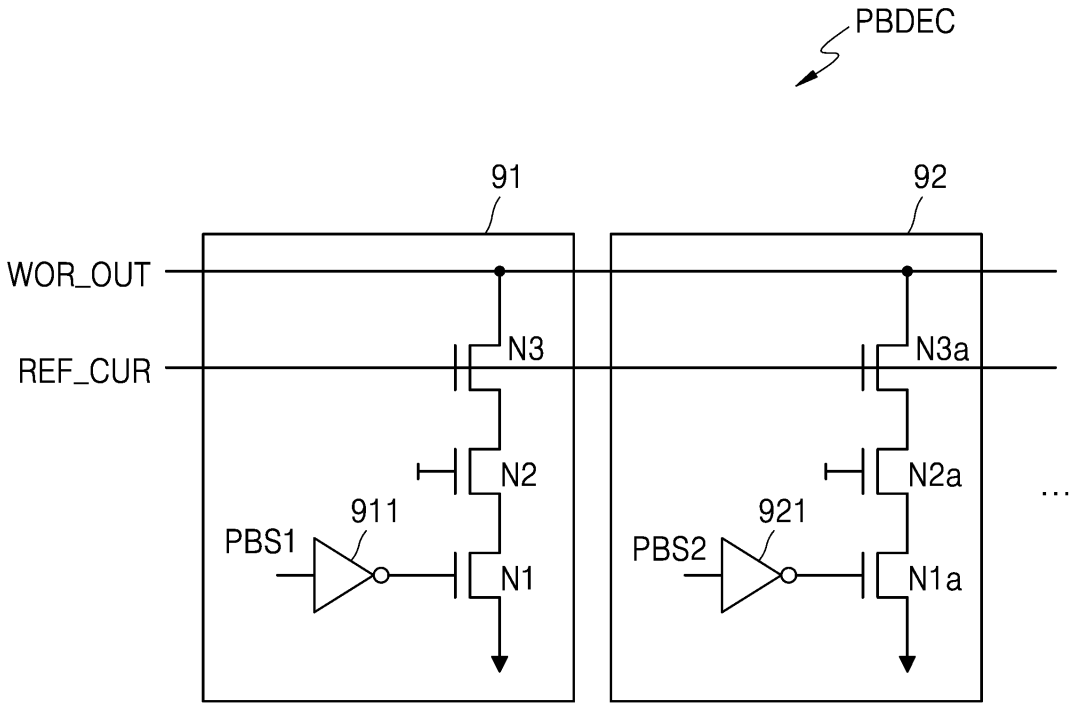

PBDEC
91
92
WOR_OUT
REF_CUR
N3
N3a
N2
N2a
911
921
PBS1
PBS2
N1
N1a
...

FIG. 9

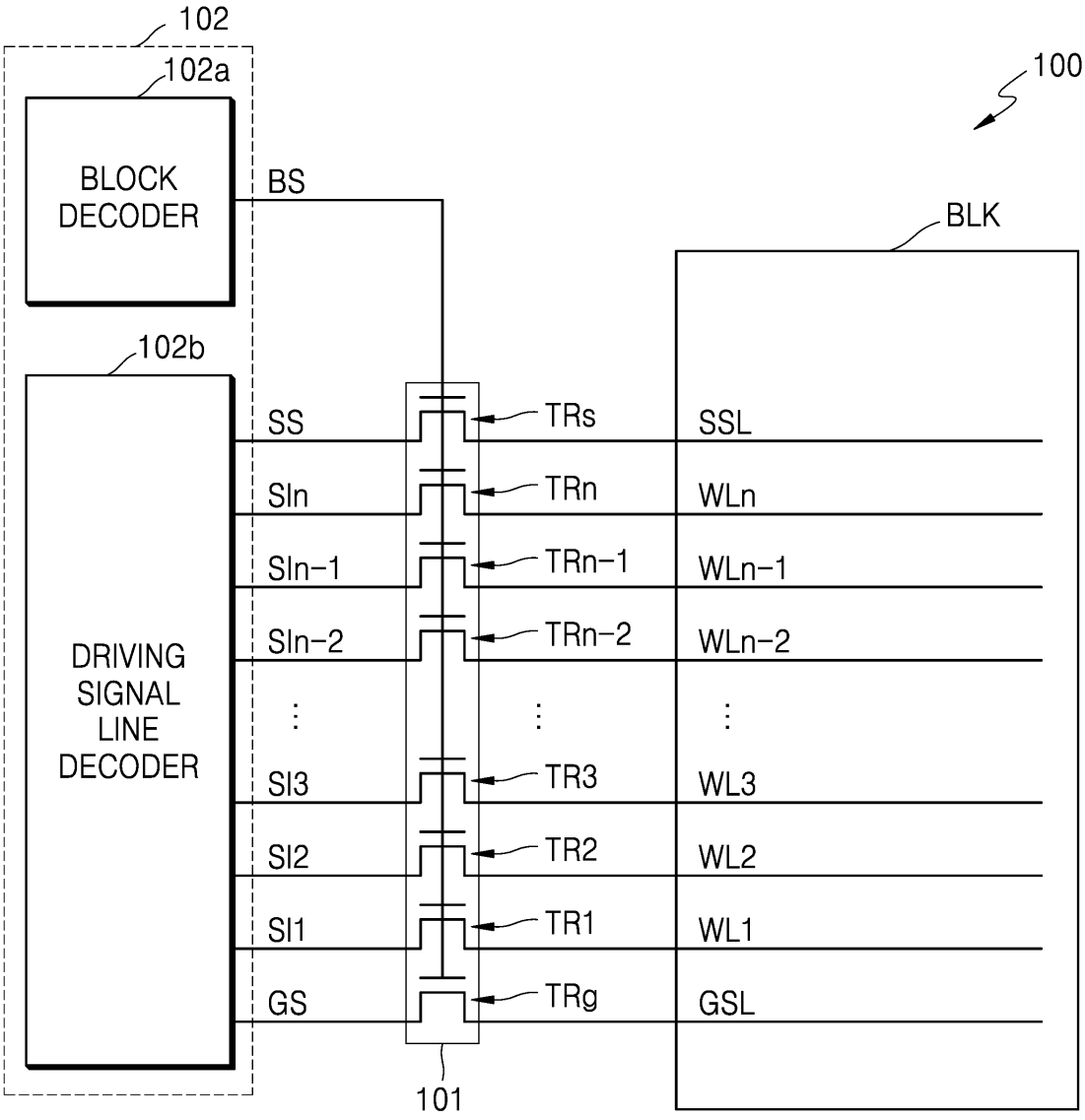

102
102a
BLOCK DECODER
BS
102b
DRIVING SIGNAL LINE DECODER
SS
SIn
SIn-1
SIn-2
SI3
SI2
SI1
GS
TRs
TRn
TRn-1
TRn-2
TR3
TR2
TR1
TRg
101
100
BLK
SSL
WLn
WLn-1
WLn-2
WL3
WL2
WL1
GSL

FIG. 10

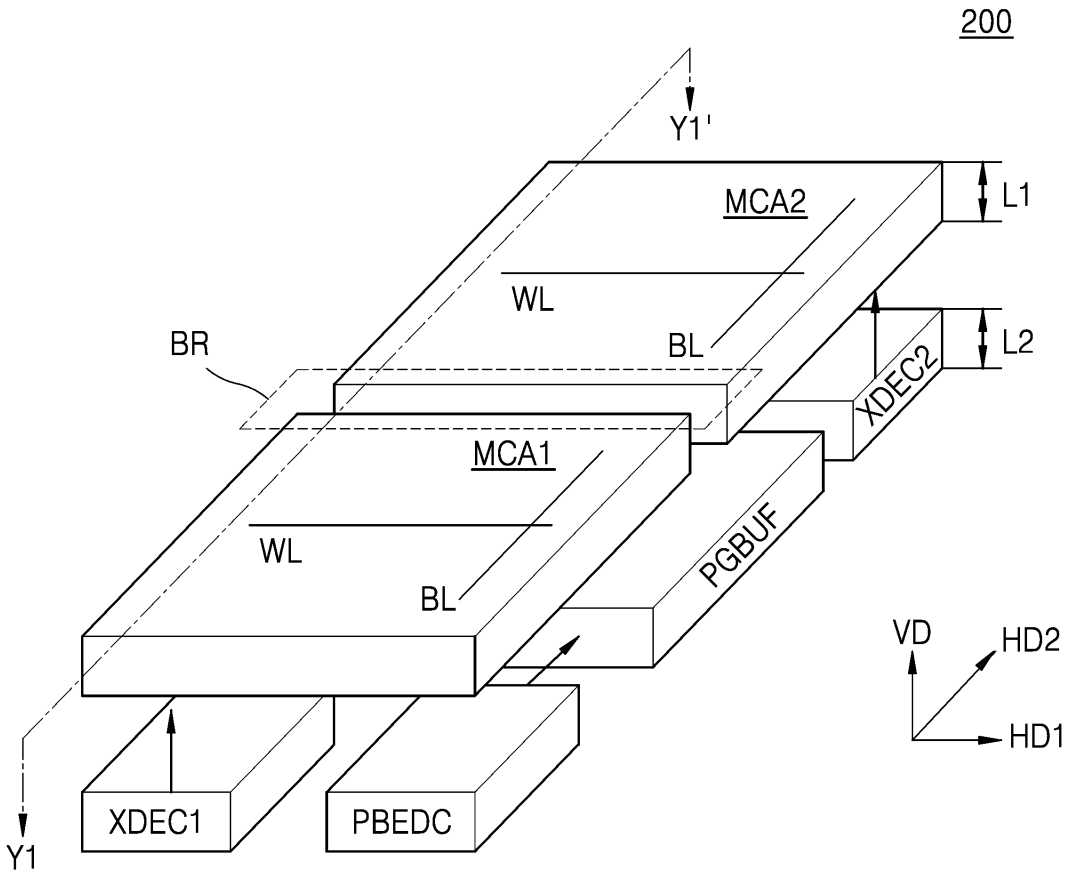

200
Y1'
MCA2
L1
WL
BR
BL
L2
XDEC2
MCA1
WL
PGBUF
BL
VD
HD2
HD1
XDEC1
PBEDC
Y1

FIG. 11A

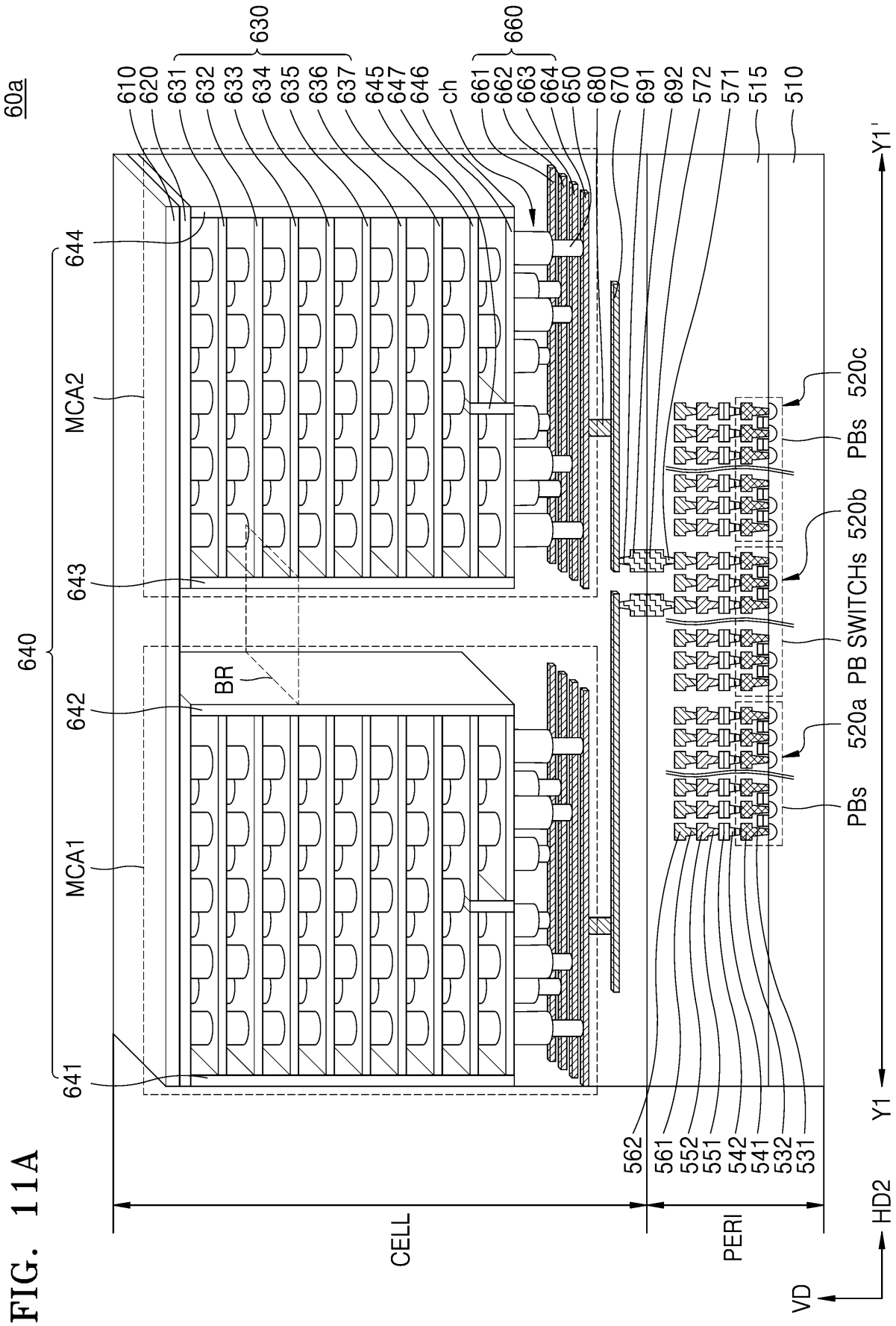

60a
640
630
660
610
620
631
632
633
634
635
636
637
645
647
646
ch
661
662
663
664
650
680
670
691
692
572
571
515
510
644
MCA2
643
642
BR
MCA1
641
562
561
552
551
542
541
532
531
520c
PBs
520b
SWITCHs
PB
520a
PBs
Y1'
Y1
HD2
VD
CELL
PERI

FIG. 11B

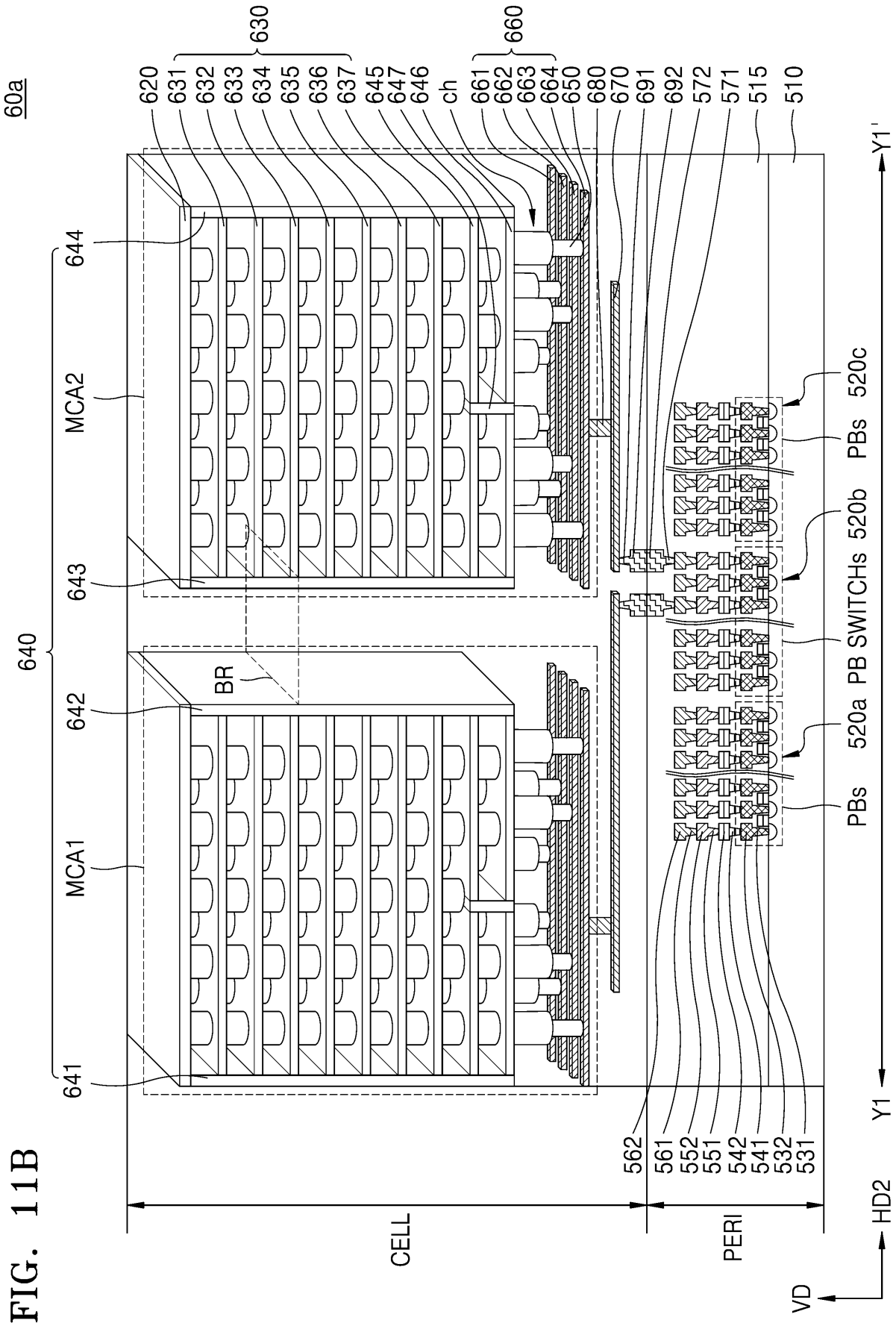

60a
640
641
642
643
644
MCA1
MCA2
BR
620
631
632
633
634
635
636
637
630
645
647
646
ch
661
662
663
664
660
650
680
670
691
692
572
571
515
510
520c
PBs
520b
SWITCHs
PB
520a
PBs
562
561
552
551
542
541
532
531
CELL
PERI
Y1
Y1'
HD2
VD

FIG. 12A

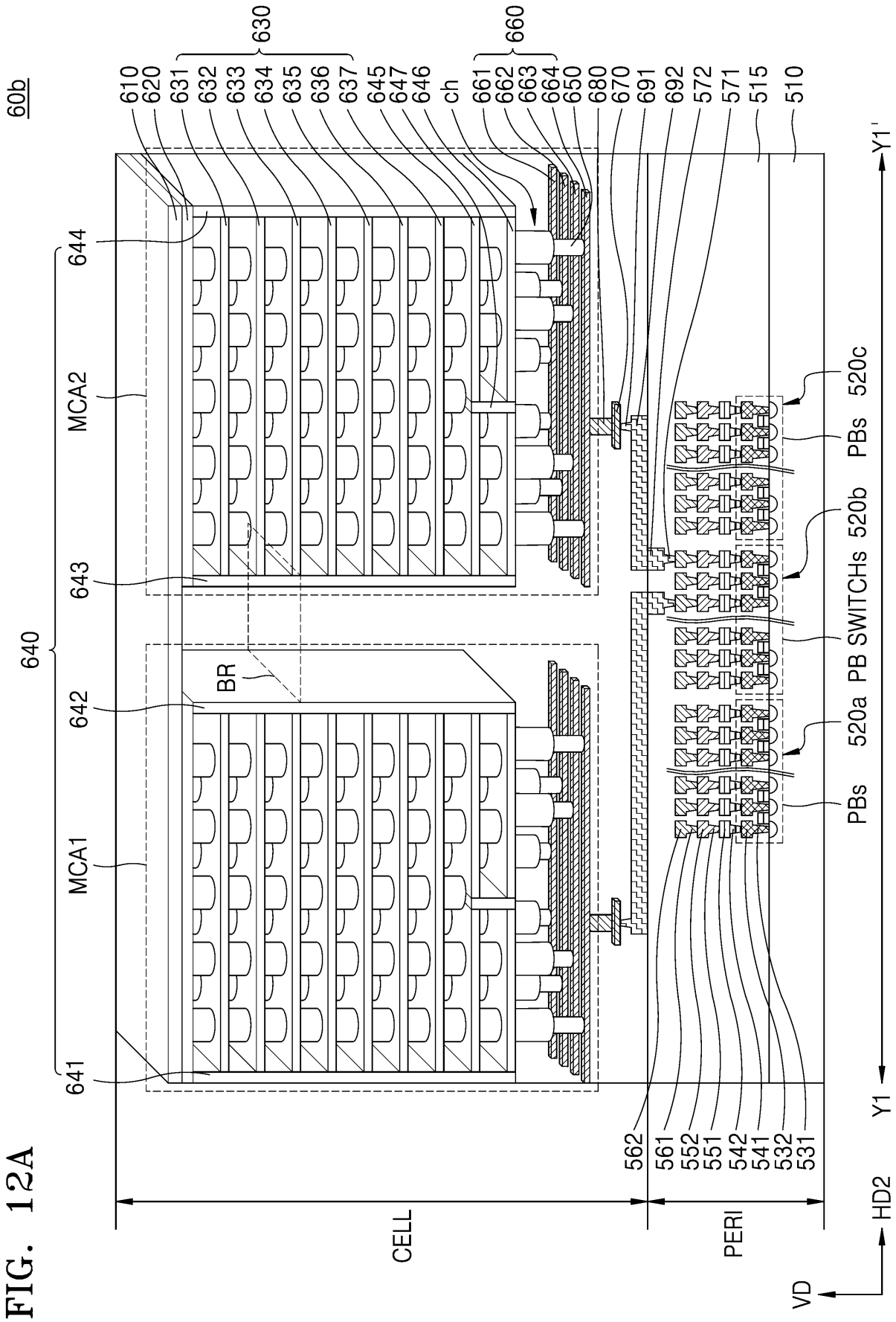

60b
640
644
MCA2
643
642
MCA1
641
BR
630
660
610
620
631
632
633
634
635
636
637
645
647
646
ch
661
662
663
664
650
680
670
691
692
572
571
515
510
520c
PBs
520b
SWITCHs
PB
520a
PBs
562
561
552
551
542
541
532
531
CELL
PERI
Y1
Y1'
HD2
VD

FIG. 12B

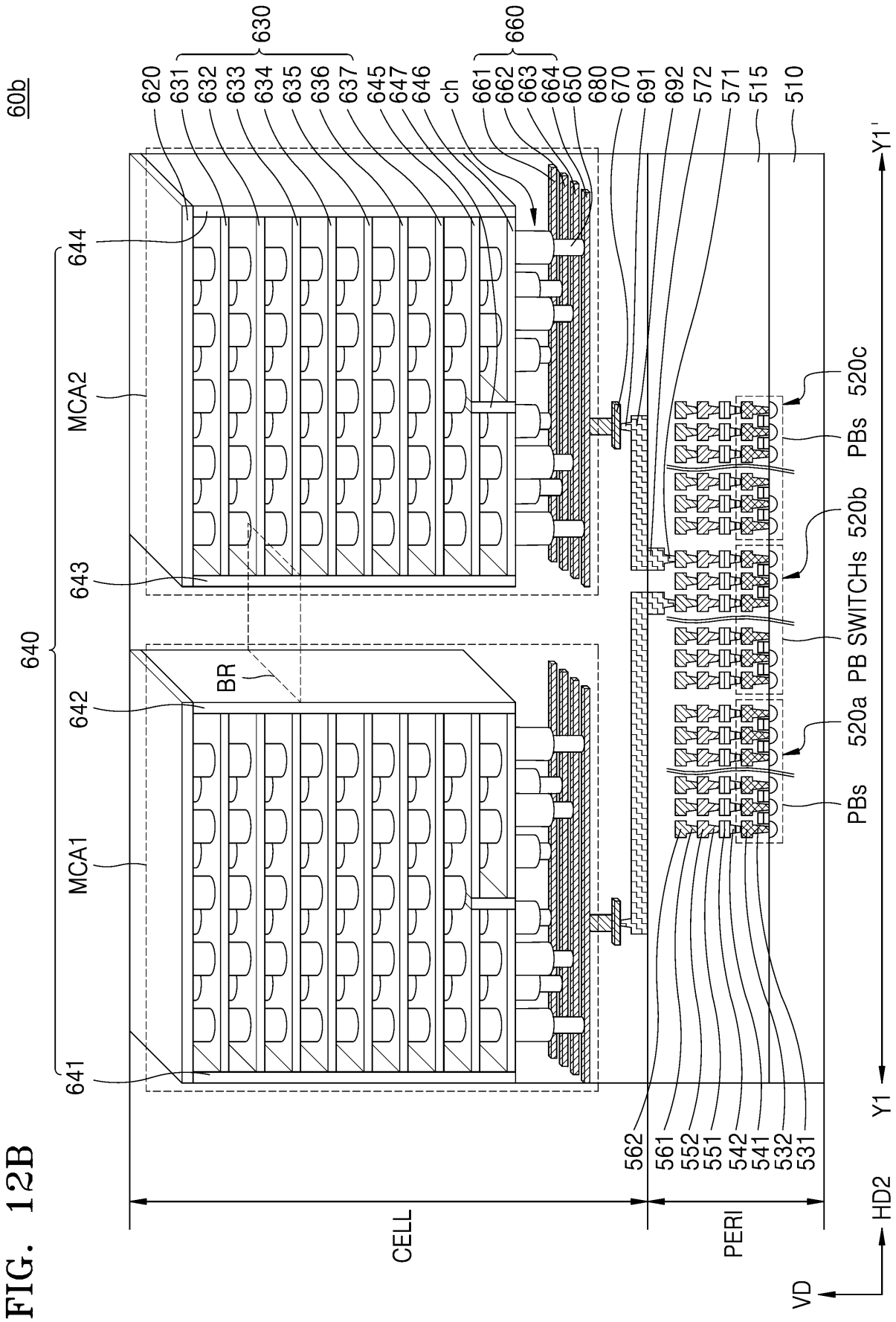

60b
620
631
632
633
634
635
636
637
630
645
647
646
ch
661
662
663
664
660
650
680
670
691
692
572
571
515
510
644
MCA2
643
640
642
BR
MCA1
641
562
561
552
551
542
541
532
531
520c
PBs
520b
SWITCHs
PB
520a
PBs
Y1'
Y1
HD2
VD
CELL
PERI

FIG. 13A

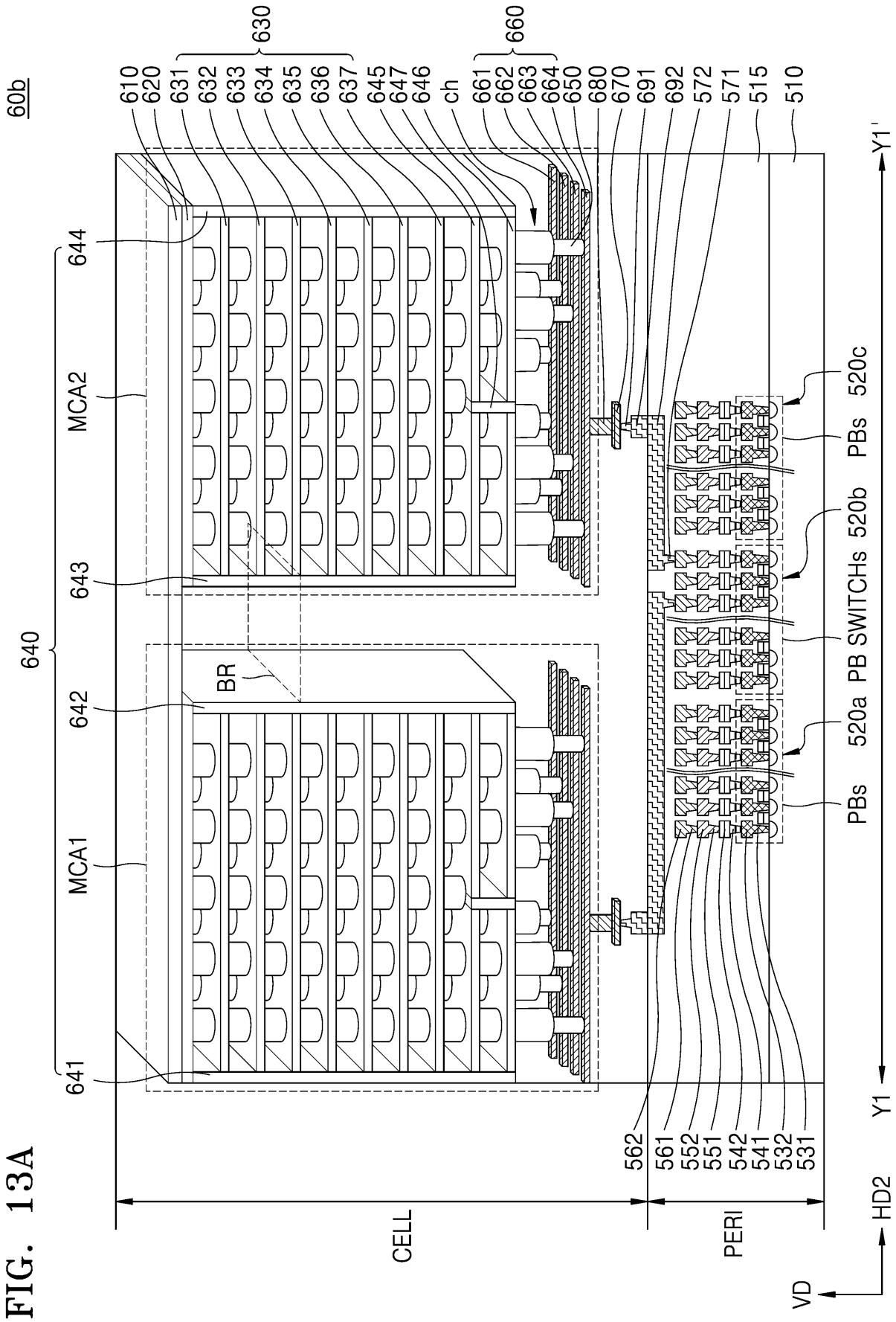

60b
640
644
MCA2
643
642
MCA1
641
BR
610
620
631
632
633
634
635
636
637
630
645
647
646
ch
661
662
663
664
660
650
680
670
691
692
572
571
515
510
520c
PBs
520b
SWITCHs
PB
520a
PBs
562
561
552
551
542
541
532
531
CELL
PERI
Y1
Y1'
HD2
VD

FIG. 13B

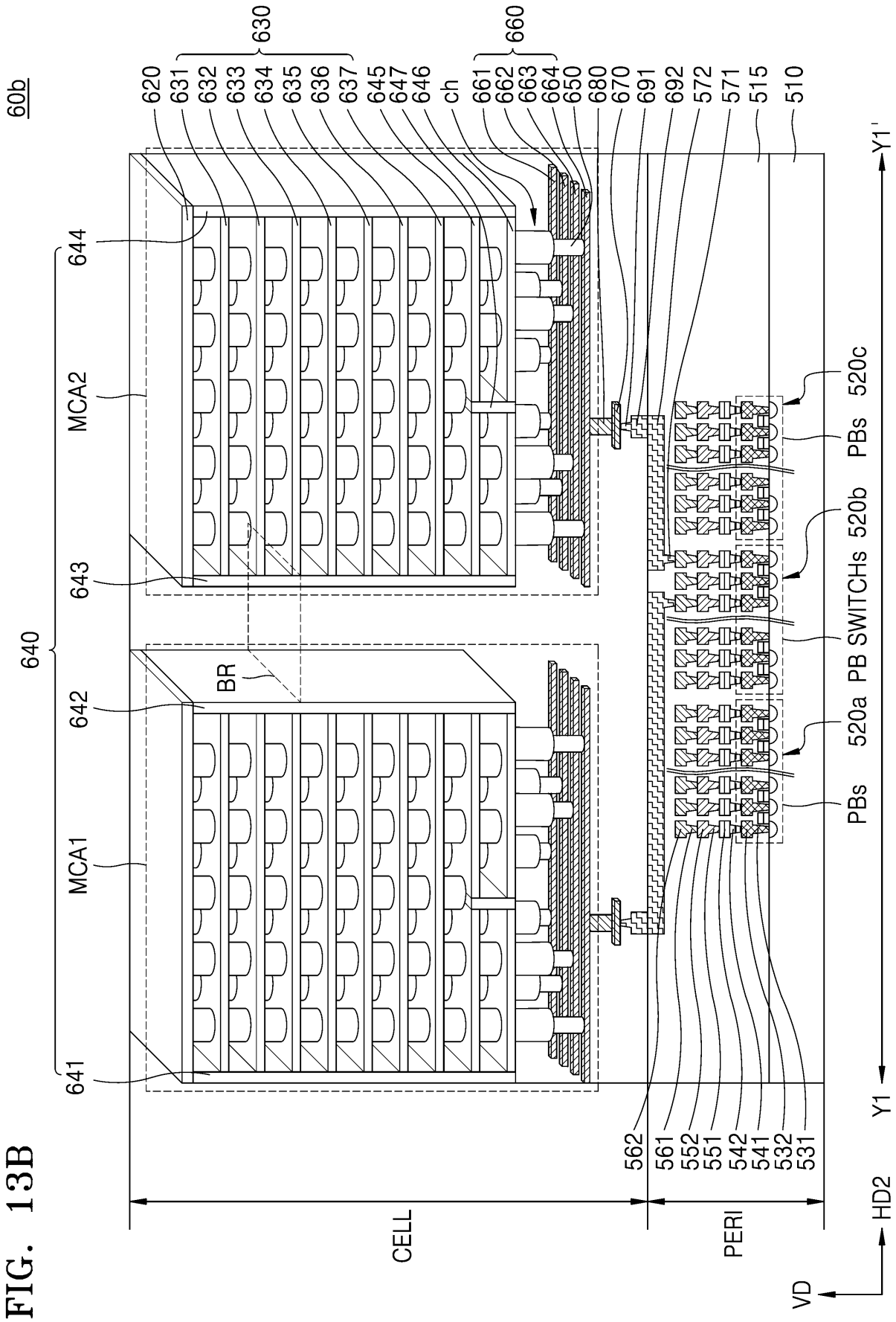

60b
620
631
632
633
634
635
636
637
630
645
647
646
ch
661
662
663
664
660
650
680
670
691
692
572
571
515
510
644
MCA2
643
640
642
BR
MCA1
641
520c
PBs
520b
SWITCHs
PB
520a
PBs
562
561
552
551
542
541
532
531
Y1'
Y1
HD2
VD
CELL
PERI

FIG. 14A

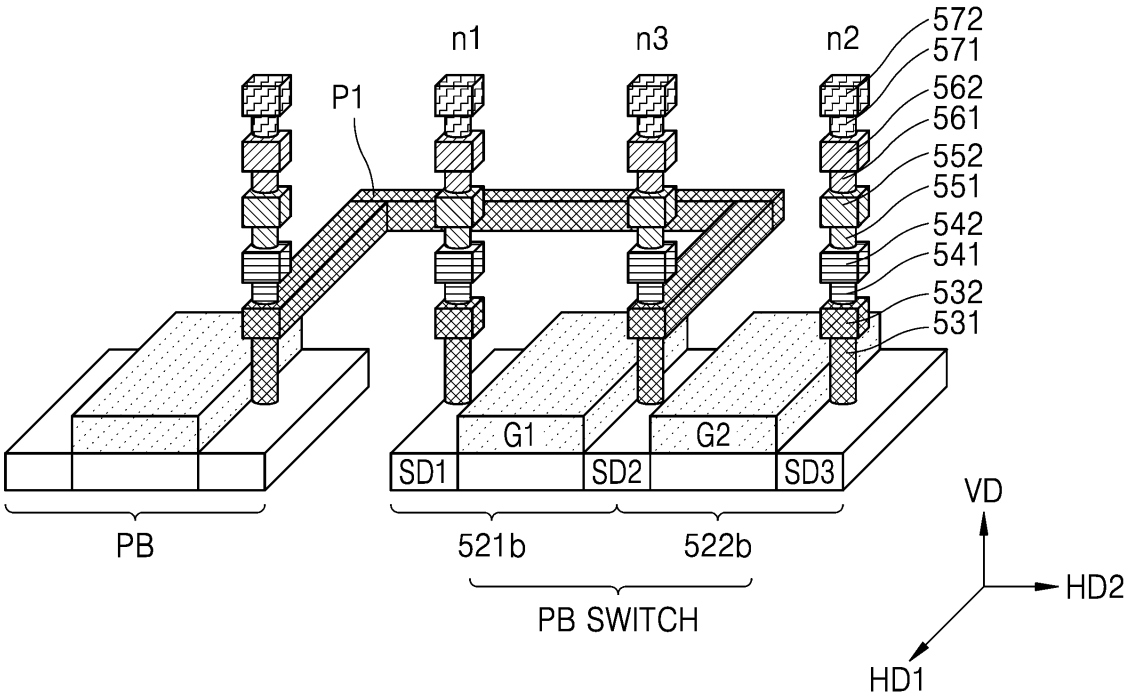

n1
n3
n2
572
571
562
561
552
551
542
541
532
531
P1
G1
G2
SD1
SD2
SD3
PB
521b
522b
PB SWITCH
VD
HD2
HD1

FIG. 14B

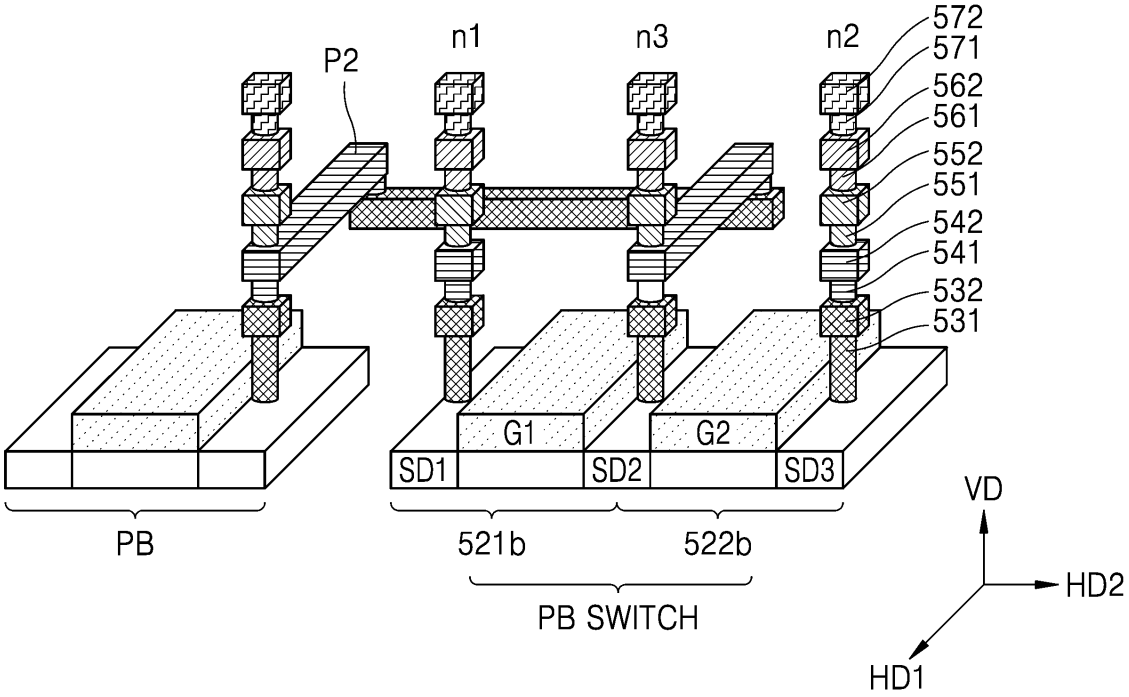

P2
n1
n3
n2
572
571
562
561
552
551
542
541
532
531
G1
G2
SD1
SD2
SD3
PB
521b
522b
PB SWITCH
VD
HD2
HD1

FIG. 14C

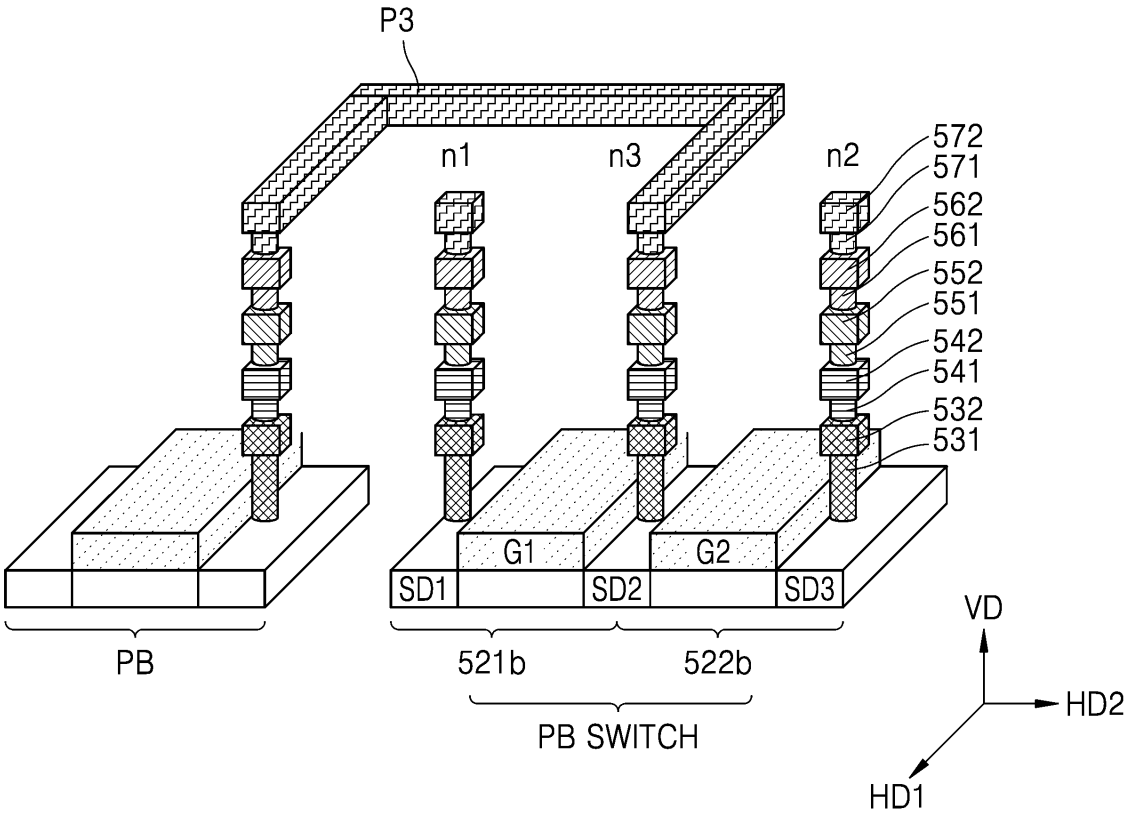

P3
n1
n3
n2
572
571
562
561
552
551
542
541
532
531
G1
G2
SD1
SD2
SD3
PB
521b
522b
PB SWITCH
VD
HD2
HD1

FIG. 14D

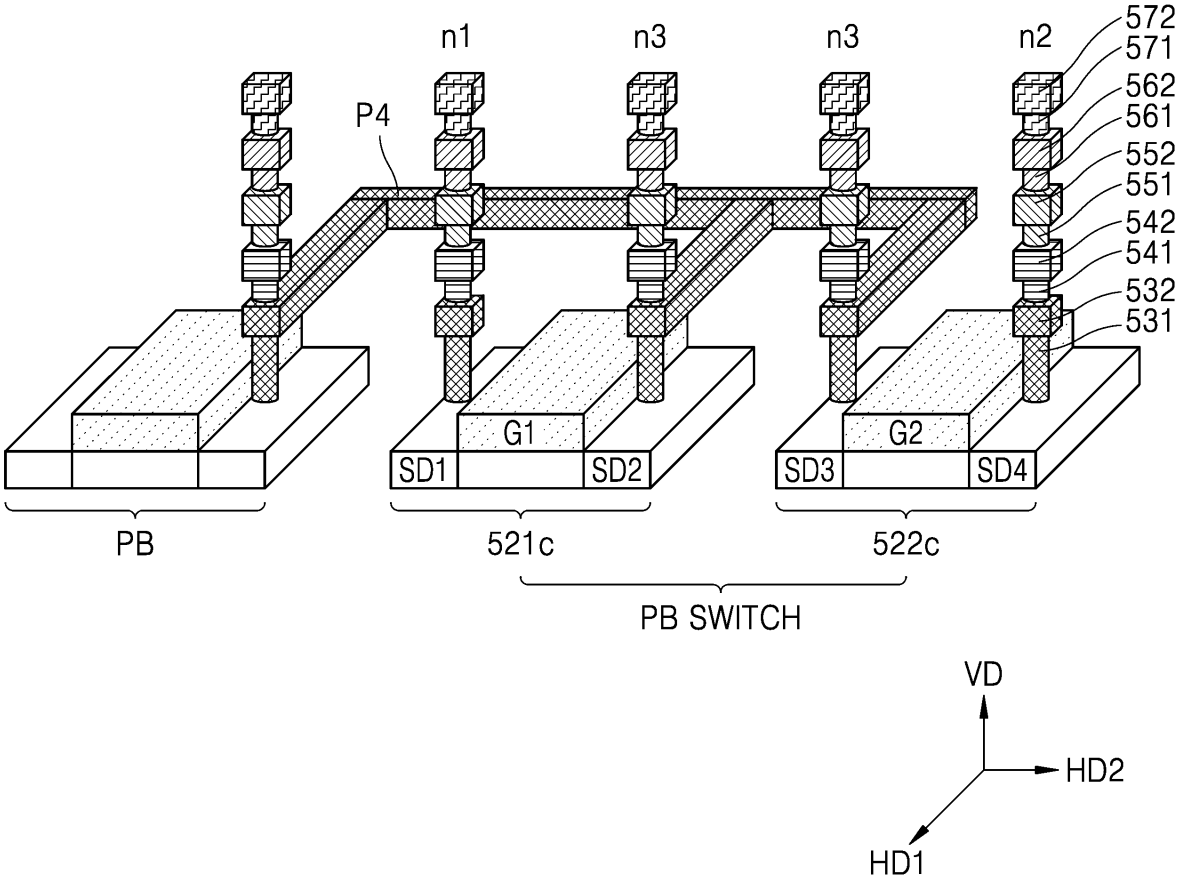

n1
n3
n3
n2
572
571
562
561
552
551
542
541
532
531
P4
G1
G2
SD1
SD2
SD3
SD4
PB
521c
522c
PB SWITCH
VD
HD2
HD1

FIG. 15A

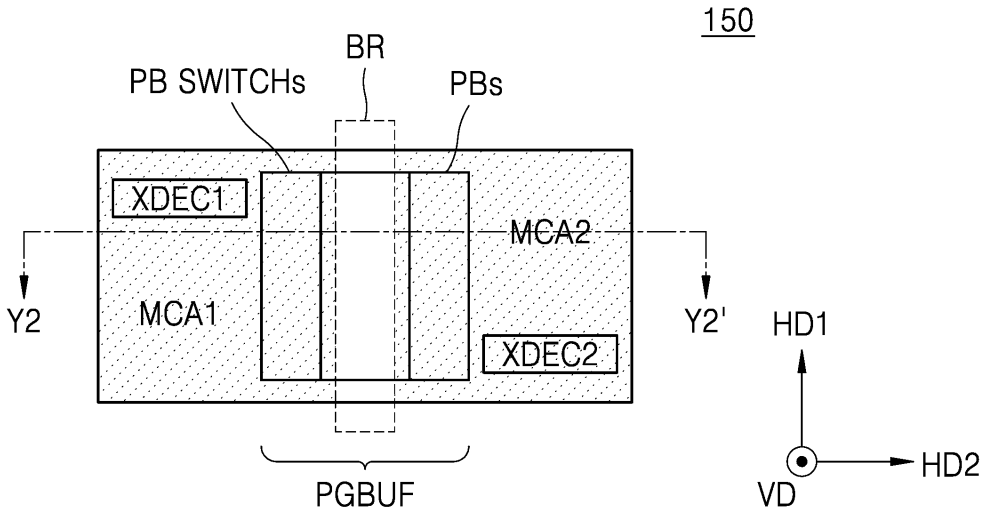

150
BR
PB SWITCHs
PBs
XDEC1
MCA2
Y2
MCA1
Y2'
XDEC2
HD1
HD2
VD
PGBUF

FIG. 15B

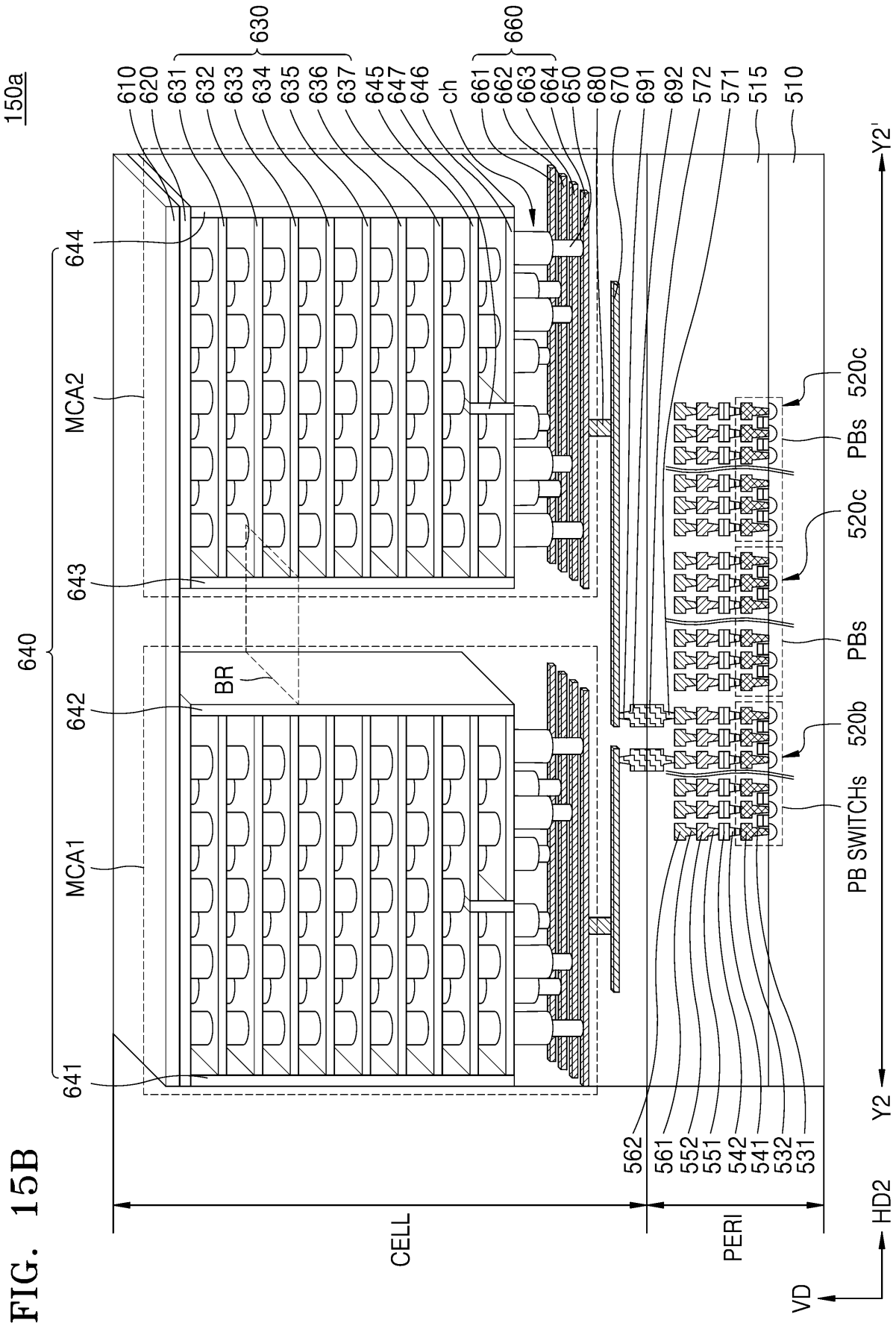

150a
640
630
660
610
620
631
632
633
634
635
636
637
645
647
646
ch
661
662
663
664
650
680
670
691
692
572
571
515
510
644
MCA2
643
642
BR
MCA1
641
520c
PBs
520c
PBs
520b
PB SWITCHs
562
561
552
551
542
541
532
531
CELL
PERI
Y2
Y2'
HD2
VD

FIG. 15C

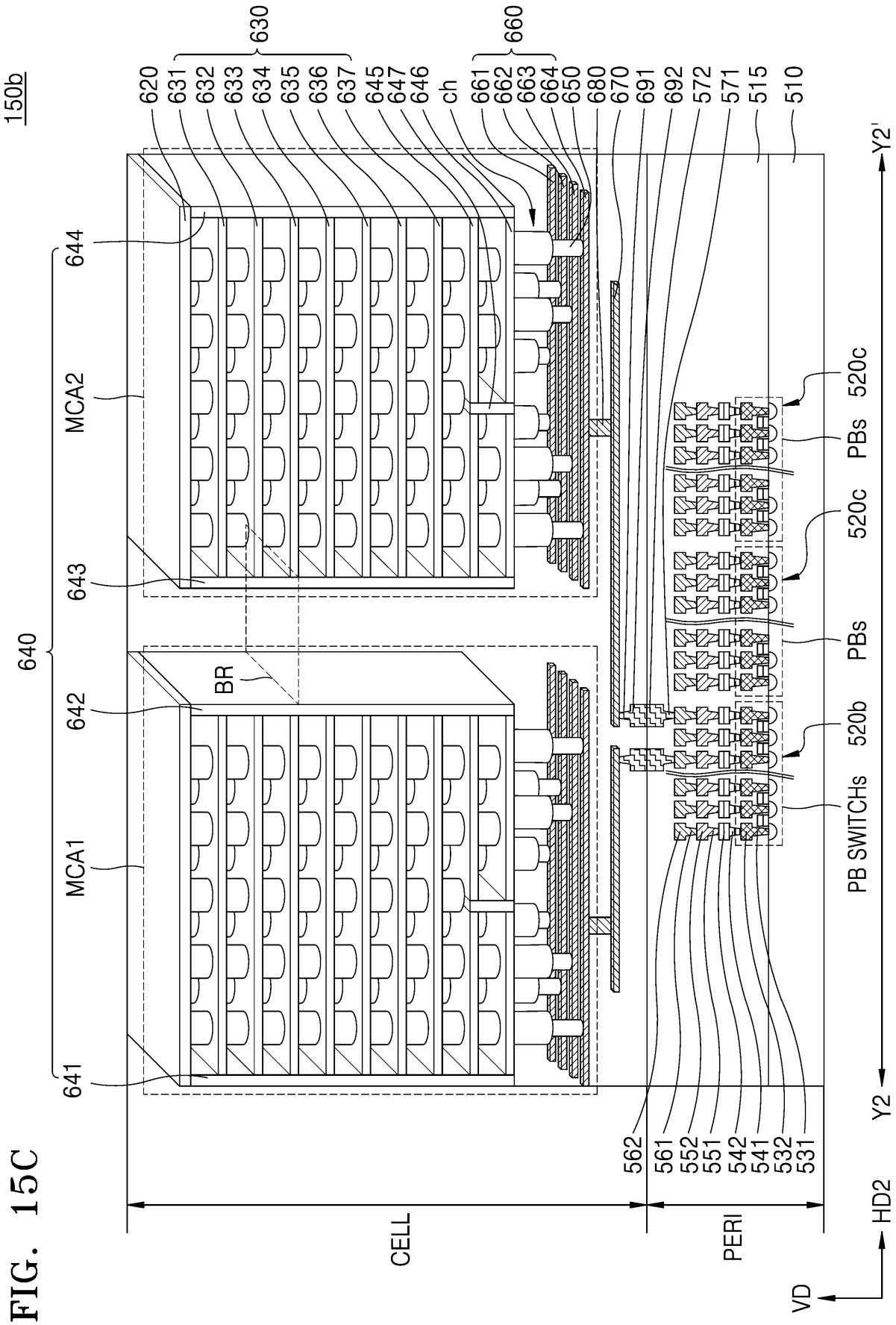

150b
620
631
632
633
634
635
636
637
630
645
647
646
ch
661
662
663
664
660
650
680
670
691
692
572
571
515
510
644
MCA2
643
640
642
BR
MCA1
641
520c
PBs
520c
PBs
520b
PB SWITCHs
562
561
552
551
542
541
532
531
CELL
PERI
Y2'
Y2
HD2
VD

FIG. 16A

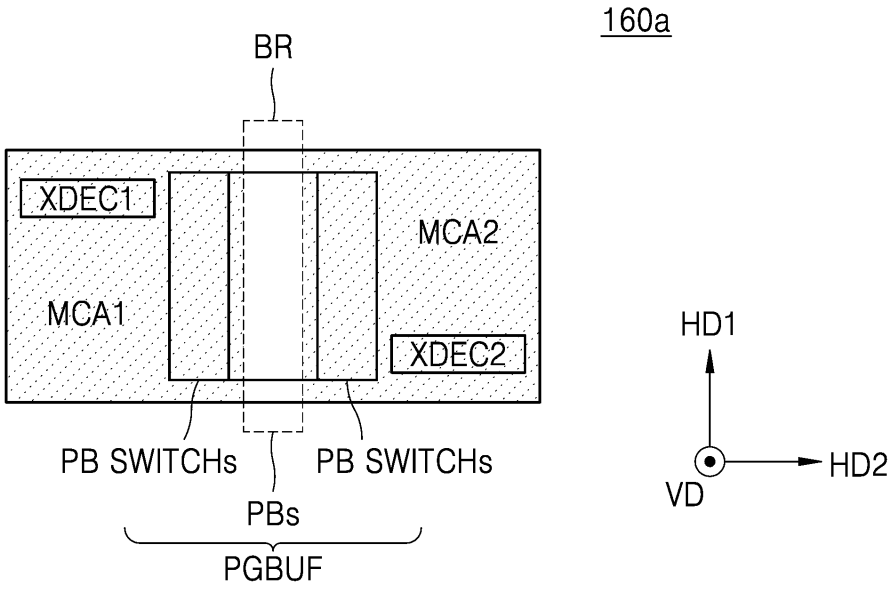

160a
BR
XDEC1
MCA2
MCA1
XDEC2
PB SWITCHs
PB SWITCHs
PBs
PGBUF
HD1
HD2
VD

FIG. 16B

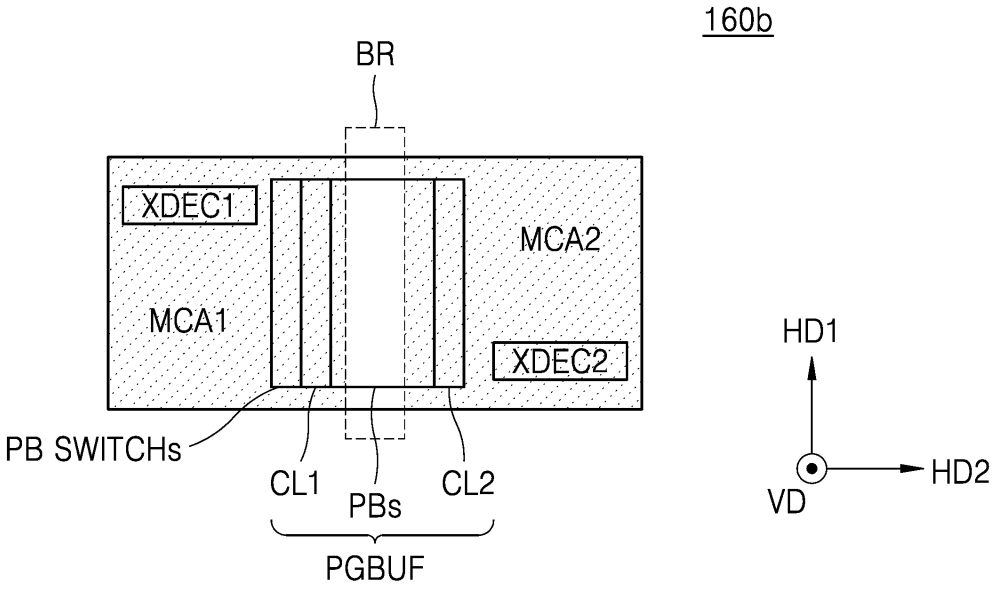

160b
BR
XDEC1
MCA2
MCA1
XDEC2
PB SWITCHs
CL1
PBs
CL2
PGBUF
HD1
HD2
VD

FIG. 16C

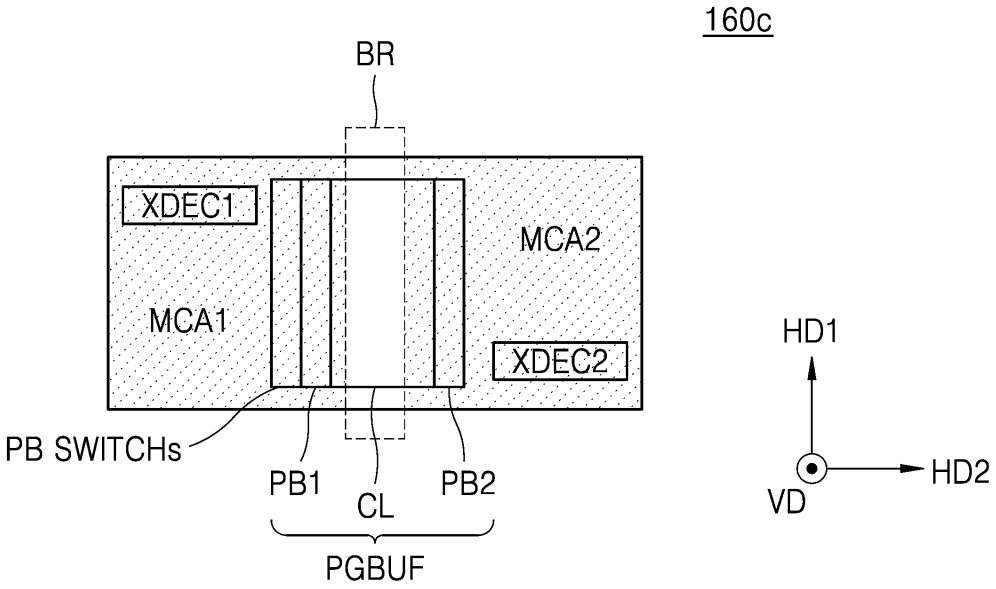

160c
BR
XDEC1
MCA2
MCA1
XDEC2
PB SWITCHs
PB1
CL
PB2
PGBUF
HD1
VD
HD2

FIG. 17A

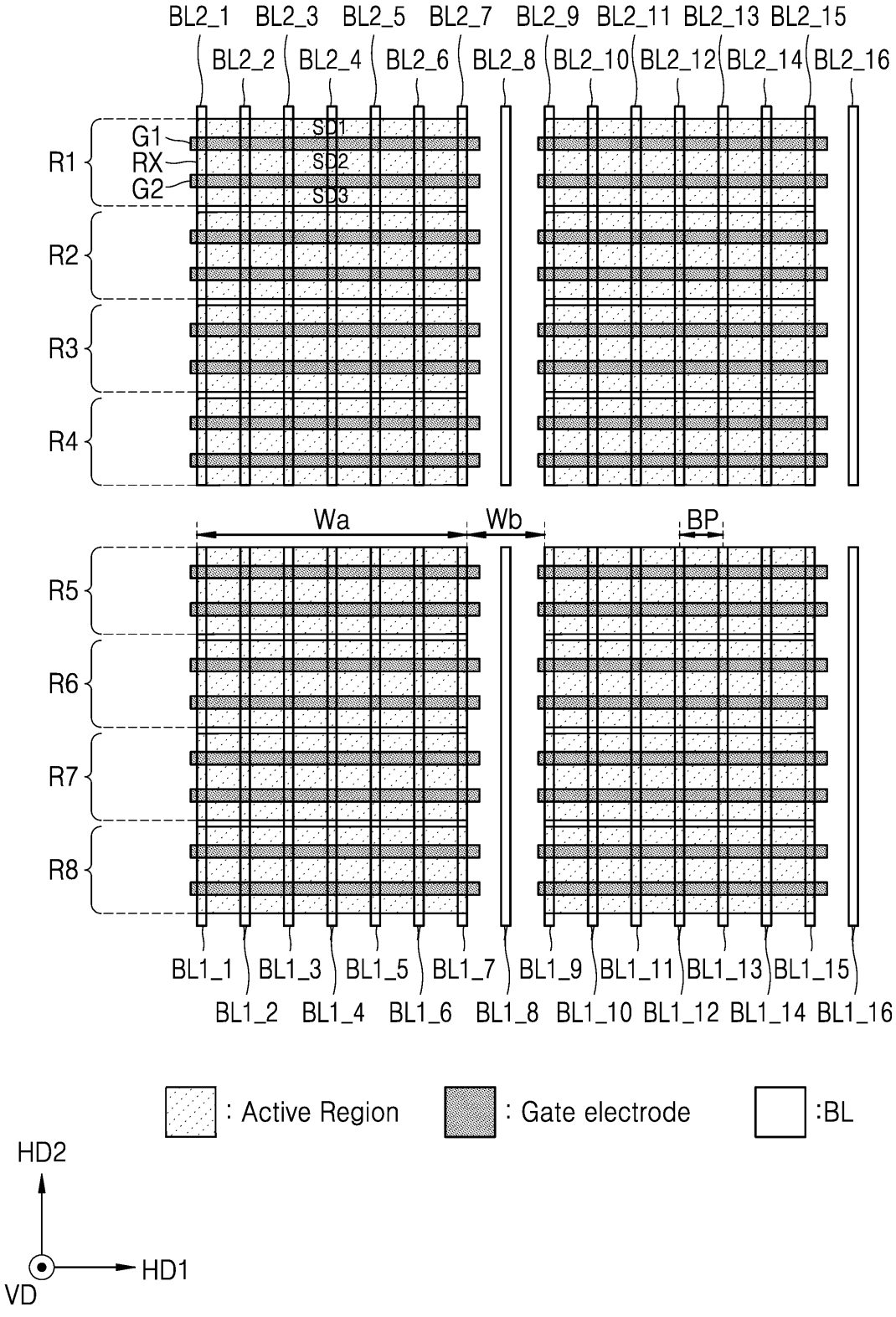

BL2_1
BL2_3
BL2_5
BL2_7
BL2_9
BL2_11
BL2_13
BL2_15
BL2_2
BL2_4
BL2_6
BL2_8
BL2_10
BL2_12
BL2_14
BL2_16
G1
RX
G2
SD1
SD2
SD3
R1
R2
R3
R4
Wa
Wb
BP
R5
R6
R7
R8
BL1_1
BL1_3
BL1_5
BL1_7
BL1_9
BL1_11
BL1_13
BL1_15
BL1_2
BL1_4
BL1_6
BL1_8
BL1_10
BL1_12
BL1_14
BL1_16
: Active Region
: Gate electrode
:BL
HD2
HD1
VD

FIG. 17B

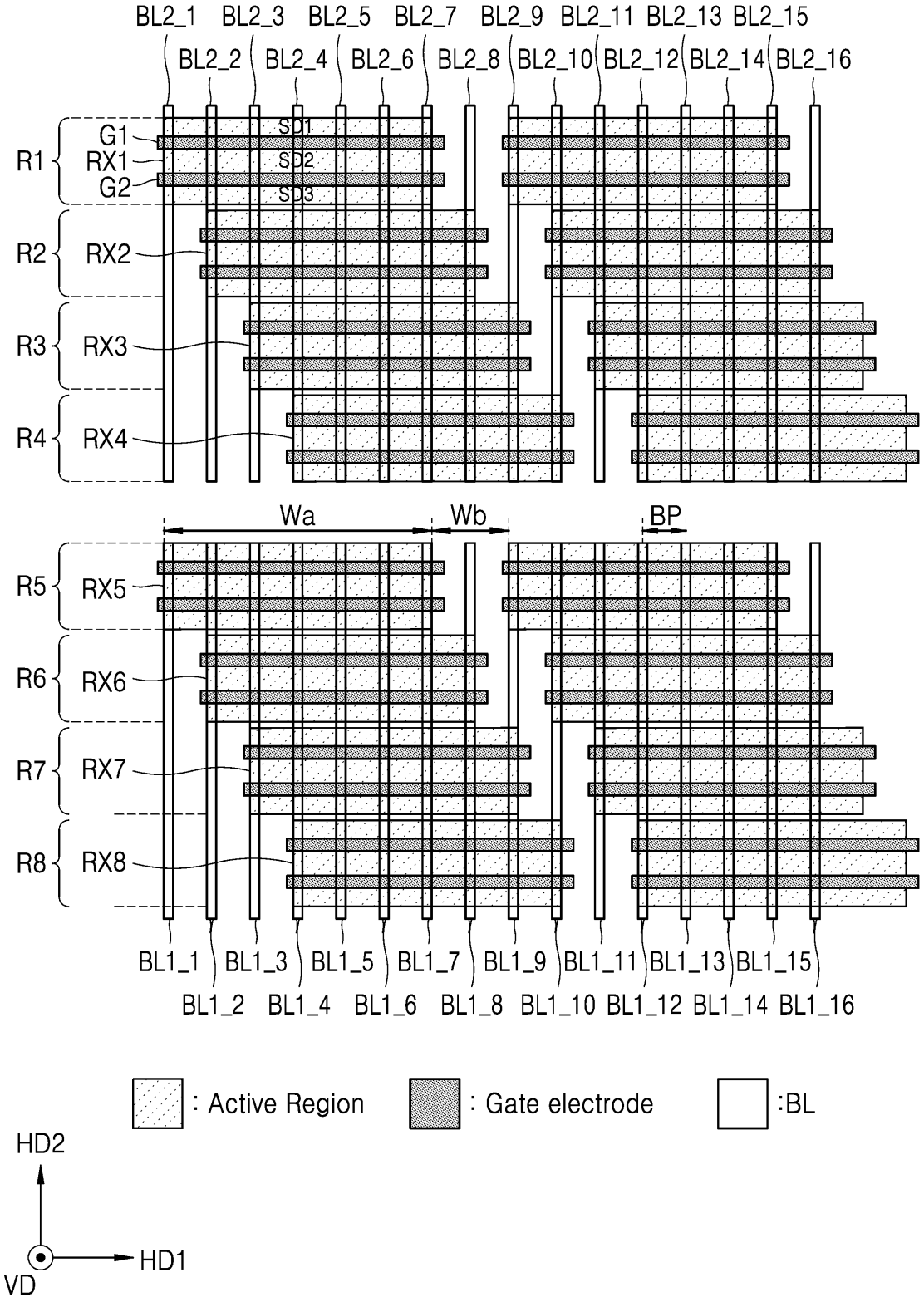

BL2_1
BL2_3
BL2_5
BL2_7
BL2_9
BL2_11
BL2_13
BL2_15
BL2_2
BL2_4
BL2_6
BL2_8
BL2_10
BL2_12
BL2_14
BL2_16
R1
G1
RX1
G2
SD1
SD2
SD3
R2
RX2
R3
RX3
R4
RX4
Wa
Wb
BP
R5
RX5
R6
RX6
R7
RX7
R8
RX8
BL1_1
BL1_3
BL1_5
BL1_7
BL1_9
BL1_11
BL1_13
BL1_15
BL1_2
BL1_4
BL1_6
BL1_8
BL1_10
BL1_12
BL1_14
BL1_16
: Active Region
: Gate electrode
:BL
HD2
HD1
VD

FIG. 18A

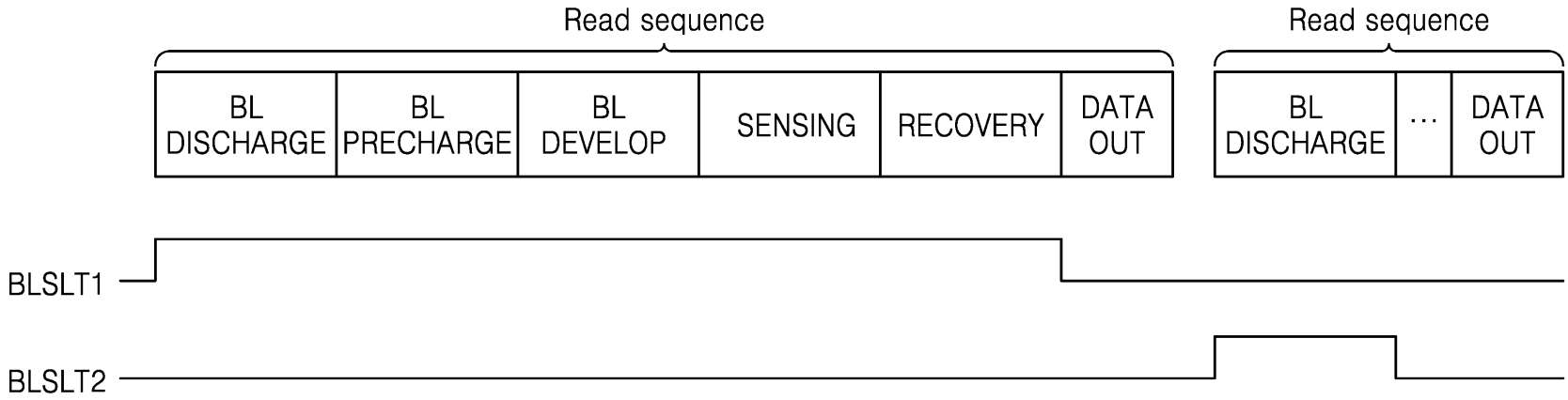

Read sequence
Read sequence
BL DISCHARGE
BL PRECHARGE
BL DEVELOP
SENSING
RECOVERY
DATA OUT
BL DISCHARGE
...
DATA OUT
BLSLT1
BLSLT2

FIG. 18B

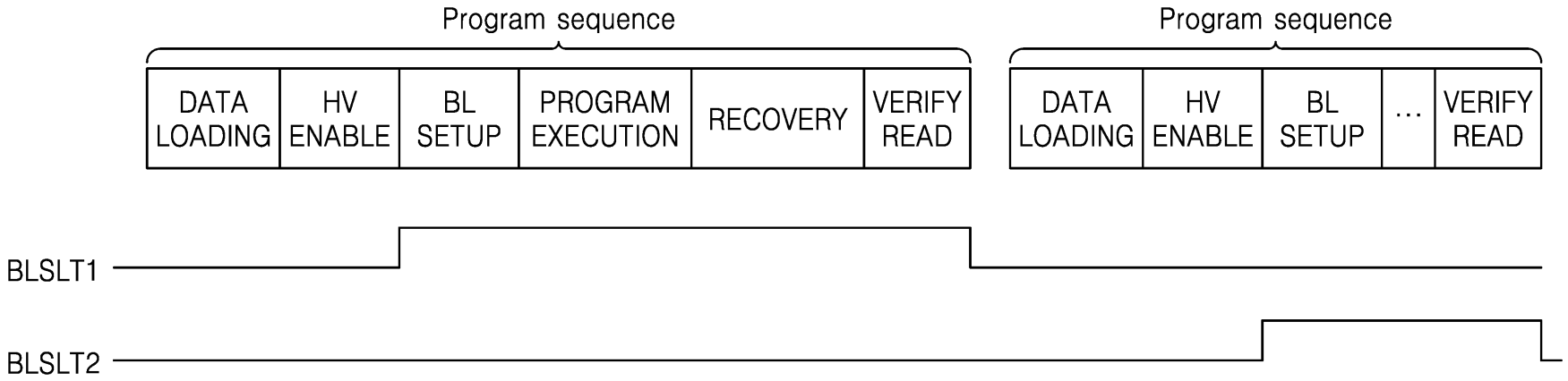
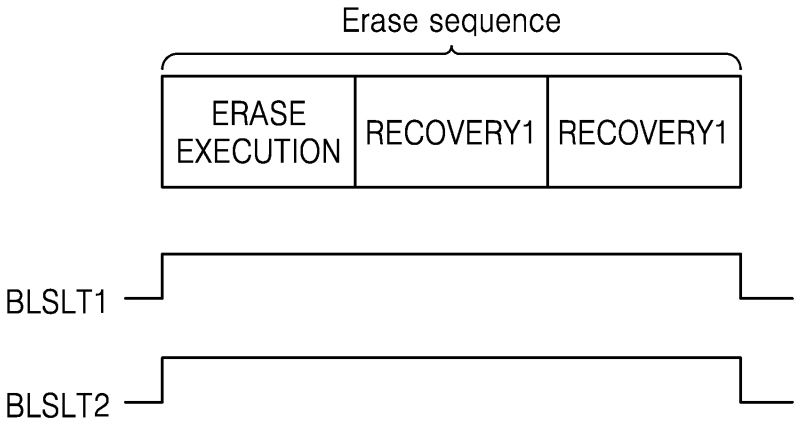

Program sequence
Program sequence
DATA LOADING
HV ENABLE
BL SETUP
PROGRAM EXECUTION
RECOVERY
VERIFY READ
DATA LOADING
HV ENABLE
BL SETUP
...
VERIFY READ
BLSLT1
BLSLT2

FIG. 18C


Erase sequence
ERASE EXECUTION
RECOVERY1
RECOVERY1
BLSLT1
BLSLT2