ABSTRACT

Method and Apparatus for Implementing A Four Stage Branch Resolution System in a Computer Processor.

A four stage branch instruction resolution system for a pipelined processor is disclosed. A first stage of the branch instruction resolution system predicts the existence and outcome of branch instructions within an instruction stream such that an instruction fetch unit can continually fetch instructions. A second stage decodes all the instructions fetched. If the decode stage determines that a branch instruction predicted by the first stage is not a branch instruction, the decode stage flushes the pipeline and restarts the processor at a corrected address. The decode stage verifies all branch predictions made by the branch prediction stage. Finally, the decode stage makes branch predictions for branches not predicted by the branch prediction stage. A third stage executes all the branch instructions to determine a final branch outcome and a final branch target address. The branch execution stage compares the final branch outcome and final branch target address with the predicted branch outcome and predicted branch target address to determine if the processor must flush the front-end of the microprocessor pipeline and restart at a corrected address. A final branch resolution stage retires all branch instructions. The retirement stage ensures that any instructions fetched after a mispredicted branch are not committed into permanent state.

(Figure 1)