POWER AMPLIFICATION WITH REDUCED GAIN VARIATION

ABSTRACT

A power amplifier can include an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level. The power amplifier can further include a bias circuit configured to provide a bias signal to the amplifying transistor, and a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor. The feedback circuit can include a resistance and a capacitance arranged in series. The power amplifier can further include a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier.

[Figure 2]