

## Avionics Video Source Simulator

### FIELD OF INVENTION

The invention relates broadly to an avionics video source simulator and to a method for avionics video source simulation.

### BACKGROUND

During the system integration phase of an aircraft upgrade programme, engineers commonly encounter problems with development items, such as the incompatibility of a newly developed mission computer to decode and display avionics video signals received from existing equipment installed in the aircraft. Often, such incompatibility issues surface during the final stage of the development programme, i.e. when final acceptance tests are carried out to ensure that the mission computer is able to interface seamlessly with all the existing equipment used in the aircraft. By then, the mission computer would have undergone extensive tests including environmental qualification tests. As a result, these tests may have to be repeated and they are not only time-consuming, but also involve significant costs.

The cause of such problems may not be associated with the failure of the mission computer to comply with its own specifications. Commonly, the cause is related to the unavailability of complete and accurate technical video interface data. For example, the specification for a particular avionics video signal may be too generalised and may contain inaccurate information regarding video amplitude, synchronisation level, aspect ratio etc. If the video interface card inside the mission computer is designed based on the inaccurate video information, it may have to undergo re-design and repeat the testing phase again, which affects delivery schedule.

Another problem encountered is the restriction imposed in obtaining the actual equipments used in an aircraft, for the purposes of testing in a lab. For instance, sensitive aircraft equipment, such as a targeting pod, a navigation pod, a training missile, a radar system, etc are not easily available. Often, repeated formal applications to obtain the equipments are required, and preparing such applications needs extensive documentation and processing time. Even after approval, such equipment may only be

available for a short duration. As several integration tests are involved before final acceptance, easy access to suitable video signal sources is very important to the development programme.

Also, interface data for avionics video signals used in an aircraft is not openly available, and it is difficult for a third party to verify the accuracy of such data without ready access to the actual equipment used in the aircraft.

In addition, there is a problem of mismatch in aspect ratio of video images that are displayed on a video monitor. For instance, many fighter aircrafts require video images with an aspect ratio of 1:1. Therefore, if standard video pattern generators with an aspect ratio of 4:3 are used, there will be a mismatch in the images displayed on the 1:1 monitor.

There is thus a need to have an avionics video source simulator that addresses one or more of the above disadvantages.

## **SUMMARY**

According to a first aspect of the present invention, there is provided an avionics video source simulator comprising: a decoder unit for decoding an input video signal into a digital video signal; a static video pattern generator; a converter unit for converting the digital video signal into an analogue avionics video format or for generating a static video pattern in the avionics video format based on control signals received from the static video pattern generator; a data storage unit having pre-stored therein a plurality of sets of parameters associated with different respective avionics video formats; and wherein the converter unit is controlled based on a selected one of the sets of parameters.

The avionics video formats may include air-to-ground missile (AGM) video, guided-bomb-unit (GBU) video, targeting pod video, navigation pod video, terrain following radar (TFR) video, radar video, forward looking infra red (FLIR) video, RS-170 video, RS-343 video, and standardisation agreement from NATO (STANAG) 3350 CLASS A/B/C video.

The input video signal may comprise a dynamic video signal from a video camera. The converter unit may convert the digital video signal corresponding to the dynamic video

signal into the analogue avionics video format at full frame rate of the dynamic video signal.

The input video signal may comprise a signal in PAL 625-lines TV system, NTSC 525-lines TV system, or RS-343 875-lines TV system.

The static video pattern generator may be operable to generate standard video patterns including one or more of a group consisting of a checker-board, a centre-cross, a circle, colour bars from society of motion pictures and television engineers (SMPTE), a grey scale, moving bars, and a multiburst.

The converter unit may be operable to provide the avionics video signals with different, selectable aspect ratios.

The aspect ratios may include 1:1 or 4:3.

The video source simulator may further comprise an impedance selector unit coupled to the output from the converter unit for providing the avionics video formats with different, selectable source impedances.

The source impedances may include 10 ohm, 16 ohm, 75 ohm or 93 ohm.

The converter unit may be operable to independently adjust a white level and a synchronisation level of the avionics video formats based on user selection.

The avionics video source simulator may further comprise one or more digital potentiometers for independently adjusting the white level and the synchronisation level of the avionics video formats.

The avionics video source simulator may further comprise a touch sensitive LCD user interface.

The avionics video source simulator may be operable to derive power from a portable notebook or a laptop computer power adapter, or battery pack.

According to a second aspect of the present invention, there is provided a method for avionics video source simulation, the method comprising the steps of decoding an input video signal into a digital video signal; converting the digital video signal into an analogue avionics video format; wherein the converter unit is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.

According to a third aspect of the present invention, there is provided a method for avionics video source simulation, the method comprising the step of generating a static video pattern in the avionics video format, wherein the pattern generating is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Embodiments of the invention will be better-understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 is a top view of an apparatus for simulating avionics video signals in accordance with an embodiment of the invention;

Figure 2 is an internal block diagram of the apparatus of Figure 1;

Figure 3 is a schematic block diagram of a field programmable gate array module used in Figure 2;

Figure 4 is a schematic block diagram of a power supply module used in Figure 2;

Figure 5 is a schematic block diagram of a video decoder module used in Figure 2;

Figure 6 is a schematic block diagram of a touch screen digitiser module used in Figure 2;

Figure 7 is a schematic block diagram of a liquid crystal display module used in Figure 2;

Figure 8 shows a menu displayed for selecting standard video patterns using liquid crystal display module of Figure 7;

Figure 9 shows a menu displayed for selecting the level of video signals using the liquid crystal display module of Figure 7;

Figure 10 is a schematic block diagram of a video digital-to-analogue converter module used in Figure 2;

Figure 11 is a schematic block diagram of a DC restoration and synchronisation pulse inserter module used in Figure 2;

Figure 12 a schematic block diagram of a video amplifier and output source impedance selector array module used in Figure 2;

Figure 13 shows a flowchart illustrating a method for avionics video source simulation according to an example embodiment; and

Figure 14 shows a flowchart illustrating a method for avionics video source simulation according to another example embodiment.

## **DETAILED DESCRIPTION**

Embodiments of the invention provide an avionics video source simulator that can generate avionics video signals to simulate the actual equipments used in an aircraft.

Example embodiments of the present invention provide an avionics video source simulator for generating pre-set video signals corresponding to one or more of the following avionics video formats:

- Air-to-Ground Missile (AGM) Video
- Guided-Bomb-Unit (GBU) Video
- Targeting Pod Video
- Navigation Pod Video
- Terrain Following Radar (TFR) Video
- Radar Video
- Forward Looking Infra Red (FLIR) Video
- RS-170 Video
- RS-343 Video
- Standardization Agreement from NATO (STANAG) 3350 CLASS A/B/C Video

Advantageously, the video signals of the above avionics signals are verified by probing the waveforms from representative equipments.

Embodiments of the present invention provide an avionics video source simulator for generating video signals with various aspect ratios. For example, the apparatus can simulate video signals from a navigation pod that has an aspect ratio of 4:3 or from a GBU system that has an aspect ratio of 1:1.

Embodiments of the present invention provide an avionics video source simulator having various source impedances. For example, the apparatus can provide video signals with a source impedance of 10 ohm, 16 ohm, 75 ohm or 93 ohm. For instance, the apparatus can provide static test patterns suitable for simulating AGM video signals that has a source impedance of 10 ohm or a Navigation Pod that has a source impedance of 93 ohm.

Embodiments of the present invention can provide an avionics video source simulator having provisions to adjust the white level and synchronisation level of video signals with ease. e.g. a user can increase or decrease synchronisation pulse level and/or white level of video signals using a touch screen.

Embodiments of the present invention can provide an avionics video source simulator having provisions to convert standard video signals into avionics video formats. For example, dynamic video (e.g. moving image) signals or video signals from a video camera (e.g. camcorder) can be converted into avionics formats.

Embodiments of the present invention can provide a lightweight and portable avionics video source simulator which can derive power e.g. from a portable notebook power adapter or battery pack.

Embodiments of the present invention can provide an avionics video source simulator that can be easily controlled by a user e.g. by touching the screen of an LCD panel.

#### **Acronyms used in this specification**

AGM – Air-to-Ground Missile

GBU – Guided Bomb Unit

FLIR – Forward Looking Infrared Red

JTAG – Joint Test Action Group

RGB – Red-Green-Blue  
DVD – Digital Versatile Disc or Digital Video Disc  
STANAG – Standardisation Agreement (abbreviation from North Atlantic Treaty Organisation)  
LCD – Liquid Crystal Display  
PAL – Phase Alternating Line  
NTSC – National Television System Committee  
DC – Direct Current  
PROMs – Programmable Read-Only Memories  
IEEE – Institute of Electrical and Electronics Engineers, Inc  
FPGA – Field Programmable Gate Array  
I<sup>2</sup>C – Inter-Integrated Circuit  
TV – Television  
SMPTE – Society of Motion Pictures and Television Engineers  
RISC – Reduced Instruction Set Computer  
RAM – Random Access Memory  
ASCII – American Standard Code for Information Interchange  
SPI – Serial Peripheral Interface  
DAC – Digital-to-Analogue Converter  
ITU-R – International Telecommunications Union - Radiocommunications  
RCA – Radio Corporation of America  
MMI – Man-Machine Interface  
PLL – Phase Lock Loop  
DCM – Digital Clock Manager  
ADC – Analogue-to-Digital Converter

Figure 1 is top view of an apparatus 100 for simulating avionics video signals in accordance with an embodiment of the invention.

The apparatus 100 has a housing 160. A power socket 110 and a programming port 120 are provided on one side of the apparatus 100. On a second side, the apparatus is provided with three input connectors 130 which are, for example, of the RCA type. The red, blue and green/monochrome video input signals are fed through the connectors 130. On a third side, the apparatus is provided with three output connectors 140, which are, for example, of the RCA type. The red, blue or green/monochrome video output video signals are fed through the output connectors 140. A monochrome liquid crystal display LCD panel 150 is provided on a top surface of the apparatus 100. The LCD panel 150 has a touch sensitive screen.

In the example implementation, the apparatus 100 has a dimension of 160mm (length) X 160mm (width) X 42mm (height). Furthermore, the apparatus is portable and has a weight of about 570 grams.

Figure 2 is a block diagram of the apparatus 100 of Figure 1.

An input voltage source with a voltage range of 15V to 20V is connected through a power socket 110. The input voltage can be derived from e.g. a portable notebook / laptop computer power adapter or battery pack.

The input voltage fed from the power socket 110 is fed to a power supply generator 220 for generating a plurality of voltages required for the various modules used in the apparatus 100. The power supply generator 220 can generate regulated DC voltages, such as +12V, +5V, +3.3V, +1.8V, +1.5V, -12V and -5V. The various voltages are regulated using, for example, switched mode DC-to-DC regulators.

A programming port 120 integral to the apparatus 100 is provided for programming the flash in-system configuration programmable read only memory (PROM) devices 216 using, for example, an IEEE 1149.1 test access port and a boundary-scan architecture, commonly referred to as JTAG.

The configuration PROMs 216 contain the complete configuration data and are operable to load the configuration data into a field programmable gate array FPGA 210 (explained later) during power-up mode. The configuration PROMs 216 are programmed through the programming port 120.

An input connector 130 integral to the apparatus 100 is provided for inputting dynamic video input signals (standard component RGB or monochrome formats) from an external video source, such as a video camera, DVD player etc.

An output connector 140 integral to the apparatus 100 is provided for outputting the video signals, for example, avionics signals with a monochrome video format (e.g. FLIR video) or a colour component RGB video format (e.g. STANAG 3350 CLASS C).

The apparatus 100 is integrally provided with a monochrome LCD 250 having a touch sensitive screen. The LCD has a graphic resolution of 128 X 128 on a 55 mm X 55 mm viewing area in the example implementation.

A video decoder 230 is provided for converting analogue video signals (e.g. PAL 625-lines TV system, NTSC 525-lines TV system, or RS-343 875-lines TV system) fed through the input connectors 130 into digital video data. The analogue video signal is digitised, without any loss of line or field rate, using the video decoder's internally generated sampling clock, which is locked and synchronised to the incoming video. The digital video data together with the synchronisation information is routed to the field programmable gate array FPGA module 210.

A clock source 236 provides two clock signals with oscillating frequencies of 100MHz and 27MHz. Both clock signals are used by the pixel clock generator 238.

The field programmable gate array FPGA 210 can be reprogrammed and reconfigured thereby reducing design risks and increasing adaptability to design changes when there is any amendment or addition to the avionics video formats. The FPGA 210 has a large number of system gates to implement a complex logic design. In the described example, the FPGA 210 is configured to implement a variety of functional modules indicated as separate boxes in Figure 2. More particular, the FPGA 210 is

programmed and configured to implement a touch screen controller 206, a liquid crystal display user menu controller 207, a digital potentiometer controller 214, a data multiplexer 228, the I<sup>2</sup>C bus controller 224, a static video pattern generator 226, a video synchronization pulse generator 242, a clock multiplexer 239, and the pixel clock generator 238. Based on the user-selected avionics video format that is desired as an output from the apparatus 100, the FPGA 210 is pre-programmed and configured utilizing a set of parameters stored in the configuration PROMs 216. More particular, the digital potentiometer controller 214, the video synchronisation pulse generator 242, and the pixel clock generator 238 are modified using pre-programmed parameter sets depending on the selected avionics video formats.

As will be appreciated by a person skilled in the art, the apparatus 100 thus advantageously provides an avionics video source simulator in which the output signal is generated depending on the chosen avionics video signal. More particular, the digital-to-analogue converter 260 will be controlled by the digital potentiometer controller 214 via a digital potentiometer 217, and by the pixel clock generator 238 via clock multiplexer 239. The DC restoration and synchronisation pulse inserter 270 will be controlled by the digital potentiometer controller 214 via a digital potentiometer 218, and by the video synchronisation pulse generator 242. The amplifier 280 will be controlled by the digital potentiometer controller 214 via a digital potentiometer 219.

An interrupt signal is sent to a touch screen controller 206 when the touch sensitive screen of a LCD 250 is touched by a pen or a finger of a user. The touch screen controller 206 is based on a soft-core microcontroller design and is operable to initiate a read cycle to obtain horizontal and vertical coordinates of a spot being touched by the user in order to interpret the menu item selected by the user.

A LCD user menu controller 207 based on a soft-core microcontroller design is provided to generate different menu pages stored inside the dedicated memory block of the FPGA 210. The LCD user menu controller 207 is operable to initialise the LCD 250 and to send relevant pixel data from dedicated memory blocks to the LCD 250.

An inter-integrated circuit (I<sup>2</sup>C) bus controller 224 is provided to program the internal registers of the video decoder 230. The I<sup>2</sup>C bus controller 224 is based on a soft-core

microcontroller design and can contain different sets of data to program the video decoder 230 to accept the various standard video signals. In an example embodiment, the I<sup>2</sup>C bus controller 224 can hold 6 different types of data corresponding to NTSC composite, PAL composite, RS-343 composite, NTSC RGB, PAL RGB and RS-343 RGB video signals. The number and standard of the video signals that are stored in the I<sup>2</sup>C bus controller 224 can be tailored to a user's requirement.

A pixel clock generator 238 is provided to generate different pairs of pixel clocks for setting the aspect ratio of the video signals. The pixel clock frequency can be set according a desired aspect ratio (e.g. 4:3 or 1:1). For example, the avionics video source simulator is operable to display video signals with an aspect ratio of 4:3 and 1:1 for each of a 625-lines, 525-lines and 875-lines video system. For a 625-line TV system, a pair of 30MHz and 22.22MHz clocks is generated for providing video signals with aspect ratio of 4:3 and 1:1, respectively. The aspect ratio of the video source simulator is important in testing the distortion of various video patterns on a display. For instance, a circle generated with an aspect ratio of 1: 1 will be displayed without any distortion on a display having the same aspect ratio of 1:1. However, a circle generated with a 4:3 aspect ratio will be distorted on a display with an aspect ratio of 1:1. By appropriately choosing the clocks for different video formats, the avionics video source simulator can generate video signals with the relevant same aspect ratio, thereby improving the accuracy of representation.

A static video pattern generator 226 is operable to generate video patterns that are commonly used for testing a video display. The patterns include checkerboard, centre-cross, circle, colour bars from society of motion pictures and television engineers (SMPTE), grey scale, moving bars, and multiburst.

A video synchronisation pulse generator 242 is operable to generate composite (which consists of both horizontal and vertical) synchronisation pulses. Furthermore, the video synchronisation pulse generator 242 is operable to instruct a synchronisation pulse inserter 270 to insert horizontal and vertical synchronisation pulses into an analogue video. The video synchronisation pulse generator 242 is also operable to set one of the three synchronisation pulse levels to a synchronisation pulse inserter 270. Therefore, synchronisation pulses with three different voltage levels can be obtained.

A clock multiplexer 239 is provided to the static video pattern generator 226, the video synchronisation pulse generator 242 and the digital-to-analogue converter 260 to switch between an internally generated clock from the pixel clock generator 238 and a clock from the video decoder 230. When a static video pattern is generated, the clock from pixel clock generator 238 is used. In case a dynamic video from an external video source is fed-in, the clock from the video decoder 230 is used.

A digital-to-analogue converter 260 is provided to convert the digital video data from FPGA 210 into its corresponding analogue video signals.

A first digital potentiometer 217 is provided to vary the white level of an analogue video signal generated from the Digital-to-Analogue Converter 260.

A second digital potentiometer 218 is provided to vary the synchronisation pulse level and the blanking level of the analogue video signals.

A third digital potentiometer 219 is provided to vary the overall video amplitude.

A digital potentiometer controller 214 based on a soft-core microcontroller design is operable to program digital potentiometers 217, 218, 219 to vary the white level, synchronisation pulse levels, and blanking level of video signals. The voltage level of the video signals, in an example embodiment, can be varied between +9V to -9V under no-load condition. The variation of white, synchronisation and blanking levels is advantageous because video signals of different video standards require different voltage levels. As the white and synchronisation pulse levels can be adjusted independently, a user can, for example, find out the minimum synchronisation level needed in order for the receiving equipment to lock to the incoming video signals.

A data multiplexer 228 is provided to switch between the internally generated video data from the static video pattern generator 226 and the video decoder 230. During static video pattern generation, video data from the static video pattern generator 226 is used. In case dynamic video signals from an external video source are fed-in for conversion into avionics video format, the video data from video decoder 230 is used.

A DC restoration and synchronisation pulse inserter block 270 is provided for performing two stages of video processing. Firstly, the blanking level of the analogue video is shifted according to the instructions from digital potentiometer controller 214 in FPGA 210. Secondly, composite synchronisation pulses are inserted into the analogue video as instructed by the video synchronisation pulse generator 242. It is possible to insert up to three independent sets of synchronisation levels into the analogue video signal.

A video amplifier block 280 is provided to amplify and buffer the output video signals. The amount of amplification needed is controlled by the digital potentiometer controller 214 via a digital potentiometer 219 and it is pre-programmed utilizing a set of parameters stored in the configuration PROMs 216 for different set of video formats.

A source impedance selector array 290 is provided to select different source impedances and it is controlled by the FPGA 210. For example, a user can select a source impedance of 10 ohm, 16 ohm, 75 ohm or 93 ohm. The value of the source impedance depends on the type of avionics video source being selected by the user. For instance, if an AGM video source is selected, a 10-ohm source impedance is selected. Choosing the correct source impedance helps in providing an accurate representation of the actual video images.

Figure 3 is a block diagram of the field programmable gate array module 210 used in Figure 2.

The FGPA 210 has three main blocks, namely a controller block 310, a video processing block 340 and a clock generation block 370.

The controller block 310 is made up of four controllers, namely a touch screen controller 206, an I<sup>2</sup>C bus controller 224, a digital potentiometer controller 214 and a LCD user menu controller 207. In an example embodiment, all the four controllers utilise a Picoblaze™ microcontroller 311, 313, 315, 317. The Picoblaze™ microcontroller is a compact, low cost, embedded 8-bit RISC device suitable for use in a Virtex-II type of FPGA 210. Each microcontroller 311, 313, 315, 317 can execute up to 1024 instructions using a single block of RAM inside the FPGA 210. In order to accommodate a complex

logic extending over 1024 instructions, the tasks performed by the processor block 310 are divided amongst the four controllers 206, 207, 214, 224.

The touch screen controller 206 is operable to control and read data that are input from a touch screen digitiser 240. It accepts a pen interrupt signal from the touch screen digitiser 240. If the pen interrupt is enabled by touching the LCD screen, an interrupt to the Picoblaze microcontroller is initiated, which, in turn, instructs a control word to be written to the touch screen digitiser 240 to initiate a conversion. The touch screen controller 206 determines a particular menu selected by the user and this information is also relayed to the other controllers 207, 214, 224.

The I<sup>2</sup>C bus controller 224 is operable to receive information from the touch screen controller 206 so as to initiate a correct I<sup>2</sup>C routine to program the video decoder 230. In an embodiment, six types of I<sup>2</sup>C routines are found inside the I<sup>2</sup>C bus controller, namely NTSC composite, NTSC RGB, PAL composite, PAL RGB, RS-343 composite and RS-343 RGB. The number and standard of the video signals that are stored in the I<sup>2</sup>C bus controller 224 can be tailored to a user's requirement.

The digital potentiometer controller 214 handles the serialisation of control bytes and delivery of data to the digital potentiometers 217, 218 and 219 via a 3-wire serial peripheral interface (SPI) bus.

The LCD user menu controller 207 is operable to initialise the liquid crystal display (LCD) and send pixel data to the LCD for display. The LCD is capable of displaying 128x128 dots and hence, 128x128 bits are needed to store each frame of a graphics data. In an embodiment, a Virtex-II 4000 series FPGA 210 containing 120 dedicated 18k-bit SelectRAM memory block (not shown) is used. Each SelectRAM is used to store one frame of graphics data. In an embodiment, a total of 8 SelectRAM memory blocks are needed for storing the various pages of the Man-Machine Interface (MMI). In addition, a SelectRAM memory is used to store the ASCII characters. A pointer address stored in the microcontroller 317 can display a particular ASCII character onto the LCD screen.

The video processing block 340 consists of a video synchronisation pulse generator 242, a static video pattern generator 226 and a multiplexer 228. In the embodiment, the

video synchronisation pulse generator 242 generates the synchronisation timing signals for different avionics video signals, such as AGM, GBU, FLIR, RS-343, PAL and NTSC. The multiplexer 228 is used to switch between the internally generated static video pattern from static video pattern generator 226 and the dynamic video data from the video decoder 230.

The static video pattern generator 226 produces commonly used video patterns for testing video systems. These patterns include checkerboard, centre-cross, circle, SMPTE colour bars, greyscale, moving bars and multiburst pattern.

A greyscale video pattern can be used for measuring luminance and non-linearity.

A colour bars pattern can be used for checking hue and colour saturation.

A multiburst pattern can be used for checking the frequency response of a video system by measuring the peak-to-peak amplitude of the packets.

A rectangle and circle test pattern can be used for checking the geometric distortion that may be introduced by a video system.

A checkerboard pattern can be used for measuring the power dissipation of a video system.

A moving bars pattern can be used for checking any motion artefacts introduced in a video signal.

In order to display video signals with an appropriate aspect ratio, a plurality of clock signals are provided in a clock generation block 370 via a multiplexer 239. For example, with two external clock oscillators, six different clocks can be generated using the digital clock managers (DCM) 372. For instance, 68MHz and 51MHz clocks are used to generate RS-343 video signals with 4:3 and 1:1 aspect ratio, respectively. Similarly, 30MHz and 22.22MHz clocks are used to generate PAL video signals in 4:3 and 1:1 aspect ratio, respectively. Likewise, 25MHz and 18.18MHz clocks are used to generate NTSC video signals in 4:3 and 1:1 aspect ratio, respectively.

The clock generation block 370 also supplies a 27MHz clock to the four microcontrollers 311, 313, 315, 317. Furthermore, the clock generation block 370 accepts the pixel clock from the video decoder 230 with an oscillating frequency of 27MHz for generating PAL/NTSC video signals or a 68.67MHz clock for generating RS-343 video signals.

Figure 4 is a block diagram of a power supply module used in Figure 2.

In an example embodiment, a DC input voltage of 18V is used to derive the voltages required for the internal operation of various components of the apparatus 100. In the embodiment, a plurality of commercially available integrated circuits (MAX8546 and MAX774/MAX775) are used to derive the voltages +12V, +5V, +3.3V, +1.8V, +1.5V, -12V and -5V.

In the embodiment, the regulated positive voltages of +5V, +12V, +3.3V, +1.8V and +1.5V are derived using MAX8546 step-down DC-to-DC converters 402, 404, 406, 408, 410, while the negative voltages are derived using MAX774/MAX775 inverting regulators 412, 414.

Figure 5 is a block diagram of a video decoder module 230 used in Figure 2.

In an example embodiment, a commercially available integrated circuit (ADV7401) is used to as a video decoder 230. The ADV7401 is a high-quality multi-format video decoder and graphics digitiser. The primary function of the video decoder 230 is to convert incoming analogue video signals 232 (static or moving pictures), without any loss of line or field information, into digital data 236 that are fed into the FPGA 210 for further processing.

In the embodiment, the video decoder 230 is operable to convert monochrome video signal in PAL or NTSC standard into digital signals in ITU-R BT.656 format (4:4:4 YCrCb). The video decoder 230 is also operable to decode a component RGB video signal in PAL or NTSC standard into a digital RGB (8:8:8) pixel output stream.

The internal phase lock loop (PLL) of the video decoder 230 can be programmed to lock to an incoming RS-343 875-line video signal. The video decoder 230 is capable of

sampling the 875-line video using a 68.67MHz pixel clock to decode the analogue video signal into digital data and into its relevant synchronisation pulses.

The video decoder 230 also supports a 'fast mode' I<sup>2</sup>C bus interface 234 that has a data rate of up to 400 kbits/s. The registers of the video decoder 230 are operable to be initialised and programmed by the FPGA 210 via I<sup>2</sup>C bus interface 234 to do an intended function. For example, the video decoder 230 can be programmed to decode RGB component video signals into digital RGB 8:8:8 data stream with a 27MHz pixel clock.

Figure 6 is a block diagram of a touch screen digitiser module used in Figure 2.

In an example embodiment, a commercially available integrated circuit (AD7873) is utilised as a touch screen digitiser 240. The touch screen digitiser 240 is a 12-bit successive approximation analogue to digital converter (ADC) with a synchronous serial interface and having low on-resistance switches for driving the touch screen of a LCD 250. The touch screen digitiser 240 is operable to capture a voltage difference between X+ and X- (602, 604), or Y+ and Y- (606, 608) inputs on its internal capacitor array and digitise the voltage difference. The output voltage level at PENIRQ\* 610 goes low when a touch screen connected to the touch screen digitiser 240 is touched by a pen or finger and this signal generates an interrupt to a Picoblaze™ microcontroller 311 (refer Figure 3), which, in turn, instructs a control word to be written to the touch screen digitiser 240 to initiate a conversion of input analogue position signals from touch screen. The serial interface of touch screen digitiser 240 comprises a conversion clock DCLK 616, a chip select signal CS\* 620, a BUSY signal 618, a data-in signal DIN 614 and a data-out signal DOUT 612.

Figure 7 is a block diagram of a liquid crystal display module 250 used in Figure 2.

In an example embodiment, a commercially available LCD (MTB-S000255FYHSGY) 250 is utilised. The MTB-S000255FYHSGY is packaged together with a touch screen 704 and a NJU6676 bit mapped LCD Driver 706. The bit mapped LCD driver comprises a 25,344 bits display data RAM, a microprocessor, an instruction decoder, and common segment drivers. Image data stored in the SelectRAMs of the LCD user menu generator 207 (refer Figure 3) are displayed on the LCD panel via the FPGA interface 708. The

touch screen digitiser 240 receives the position inputs via the 4-wire touch screen interface 702.

The LCD 250 is capable of displaying a 128 x 128 dots graphics character or 16 x 16 dots characters (8-character 8-line format).

Figure 8 shows a menu 800 displayed for selecting standard video patterns using liquid crystal display module of Figure 7. Other menus (not shown) are available for selecting the pre-set avionics video formats.

The menu 800 appears on the screen of the LCD 250 (refer Figure 7) when a user intends to select a video pattern. The menu has a header 802 and has an array of icons corresponding to a desired pattern. By touching a particular icon on the LCD screen, a user can select a circle 804, centre-cross 806, checkerboard 808, greyscale 810, multiburst 812 or moving bars 814. Alternatively, the user can select an external source by touching an icon 816 on the LCD screen or can go back to other menus by touching an icon 818 on the LCD screen.

Figure 9 shows a menu 900 displayed for selecting the level of video signals using the liquid crystal display module of Figure 7.

The menu 900 appears on the screen of the LCD 250 (refer Figure 7) when a user intends to increase or decrease white and synchronisation levels of video signal. The menu has a main-header 901, and two sub-headers 902, 904 and an array of icons. The menu also has information about the nominal level of the selected video signal 906. In order to increase the white level, the user touches an icon 908 on the LCD screen under the sub-header 902. To decrease the white level, a user touches an icon 910 on the LCD screen under the sub-header 902. Similarly, in order to increase the synchronisation level, the user touches an icon 912 on the LCD screen. Similarly, in order to decrease the synchronisation level, a user touches an icon 914 on the LCD screen. To go back to other menus, the user touches an icon 916 on the LCD screen.

Figure 10 is a block diagram of a video digital to analogue converter module 260 used in Figure 2.

In an example embodiment, a commercially available integrated circuit (ADV7123) is used as a digital-to-analogue converter 260. The digital-to-analogue converter 260 is operable to convert a 24-bit digital video data 1002, 1004, 1006 that are fed from the FPGA 210 (refer Figure 3) into the corresponding analogue RGB video data 1020, 1022, 1024. The data fed into the digital-to-analogue converter 260 via the FPGA interface 1028 consists of a 8-bit data corresponding to RED[0..7]1002, a 8-bit data corresponding to GRN[0..7]1004, and a 8-bit data corresponding to BLU[0..7]1006. In addition, the FPGA 210 provides blanking BLANK\* 1008, composite synchronisation CSYNC\* 1010 and pixel clock PCLK 1012 signals to the digital-to-analogue converter 260. The blanking signal BLANK\* 1008 is used to bring the analogue output signals 1020, 1022, 1024 to the blanking level. The pixel clock PCLK 1012 signal is used for latching the video data and the blanking signal 1008. In the embodiment, the CSYNC\* input is internally connected to the analogue green output 1022 and is tied to ground potential so that no synchronisation pulses are inserted onto the green video output 1022.

The analogue RGB output signals 1020, 1022, 1024, in the example embodiment, are routed to the DC Restoration and Synchronisation Pulse Inserter module 270 (refer Figure 2) via the DAC interface 1030.

The gain of the digital-to-analogue converter 260 is controlled by a digital potentiometer 217. In an example embodiment, a commercially available integrated circuit (AD8400) is used as the digital potentiometer 217. The AD8400 is a 1k-ohm, 256-position and digitally controlled variable resistor. The digital potentiometer 217 functions as a mechanical potentiometer or variable resistor. The FPGA 210 provides clock CLK 1014, chip select CS\* 1016 and serial data input SDI 1018 signals.

The resistance of digital potentiometer 217 can be updated through a SPI-compatible 3-wire, serial-input digital interface from the FPGA 210. The RSET 1026 value of the digital potentiometer 217 determines the magnitude of the analogue video output signals 1020, 1022, 1024.

Figure 11 is a block diagram of a DC restoration and synchronisation pulse inserter module 270 used in Figure 2.

In an example embodiment, a commercially available integrated circuit (EL 4390) is used as a triple current feedback video amplifier 1102 having a DC restore function. The DC restore function is activated by a control signal BACK PORCH 1108 from the FPGA 210 and upon activation, the video signals are restored to a reference blank level as determined by BLANK LEVEL 1110 of the digital potentiometer 218 (refer Figure 2).

The synchronisation and blanking levels of analogue video signals are controlled by a digital potentiometer 218. In an example embodiment, a commercially available integrated circuit (AD5263) is used as the digital potentiometer 218. The AD5263 is quad-channel, 256-position, digital potentiometer operable to be programmed by the FPGA 210 via a SPI-compatible, 3-wire serial interface. One channel is used to generate the video blanking level 1110 fed to the DC Restore amplifier 1102. The other three channels are used to generate different synchronisation levels 1112, 1114, 1116 that are embedded into the green video output signal 1120 at a video multiplexer 1104. A commercially available integrated circuit (AD8174) is used as a 4:1 video multiplexer 1104. The timing at which the green video input and the synchronisation level inputs are switched is determined by the FPGA 210 through a MUX\_A [0..1] 1122 signal.

Figure 12 a block diagram of a video amplifier 280 and output impedance module 290 used in Figure 2.

In an example embodiment, a plurality of commercially available integrated circuits (HA-5020) is used as video amplifiers 1202, 1204, 1206 in the amplifier block 280 (refer to Figure 2). The video amplifiers 1202, 1204, 1206 have a wide bandwidth and high slew-rate and are suitable for video applications. The gain of each video amplifier 1202, 1204, 1206 is determined by a feedback resistor  $R_f$  (not shown) and a gain resistor  $R_g$  1201, 1202, 1203. The value of each of the  $R_f$  is fixed, whereas the value of each  $R_g$  1201, 1202, 1203 is programmable via digital potentiometers (e.g. commercially available AD5290) 1208, 1210, 1212 in the digital potentiometer 3 block 219 (refer to Figure 2). Each of the digital potentiometers 1208, 1210, 1212 receives its control data from the FPGA 210 via a SPI-compatible, 3-wire serial interface.

In the embodiment, an array of commercially available S114-5 double-pole-double-throw mechanical relays (1220, 1222, 1224, 1226, 1228, 1230) is used to select the

appropriate impedance for the video output signals. The mechanical relays (1220, 1222, 1224, 1226, 1228, 1230) have low inter-contact capacitance and low contact-circuit losses (e.g. a maximum contact resistance of 0.1 ohm). The appropriate output impedance (e.g. 10 ohm, 16 ohm, 75 ohms, 95 ohms) is selected through the RELAY\_CONTROL [0..1] signals 1240 from the FPGA 210.

The avionics video source simulator described above can help in alleviating the problems encountered during aircraft testing and integration by providing reliable lab and field test signals which are not possible with commercially available pattern generators. As the avionics video source simulator can simulate signals from the actual aircraft equipments, the need to obtain sensitive avionics equipments is eliminated or reduced.

By using the avionics video source simulator to test procured equipment such as a mission computer, fewer verification tests are needed using actual avionics equipments. Video interface problem can therefore be identified much earlier in the programme. Inevitably, system integration is made easier resulting in a faster delivery schedule and reduced costs.

The avionics video source simulator can also help engineers during the design of development item – video/graphics card, intended for processing avionics video signals from avionics equipments. With the avionics video source simulator, hardware design engineers can design and confirm that a prototype video/graphics card is capable of handling the avionics video signals, prior to the design and assembly of the actual video/graphics card. Design problems can therefore be rectified during the early stage of the development programme.

Figure 13 shows a flowchart 1300 illustrating a method for avionics video source simulation according to an example embodiment. At step 1302, an input video signal is decoded into a digital video signal. At step 1304, the digital video signal is converted into an analogue avionics video format, wherein the converting is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.

Figure 14 shows a flowchart 1400 illustrating a method for avionics video source simulation. At step 1402, a static video pattern in the avionics video format is generated, wherein the pattern generating is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

**CLAIMS**

1. An avionics video source simulator comprising:
  - a decoder unit for decoding an input video signal into a digital video signal;
  - a static video pattern generator;
  - a converter unit for converting the digital video signal into an analogue avionics video format or for generating a static video pattern in the avionics video format based on control signals received from the static video pattern generator;
  - a data storage unit having pre-stored therein a plurality of sets of parameters associated with different respective avionics video formats; and
  - wherein the converter unit is controlled based on a selected one of the sets of parameters.
2. The avionics video source simulator of claim 1, wherein the avionics video formats include air-to-ground missile (AGM) video, guided-bomb-unit (GBU) video, targeting pod video, navigation pod video, terrain following radar (TFR) video, radar video, forward looking infra red (FLIR) video, RS-170 video, RS-343 video, and standardisation agreement from NATO (STANAG) 3350 CLASS A/B/C video.
3. The avionics video source simulator of any one of claims 1 to 2, wherein the input video signal comprises a dynamic video signal from a video camera.
4. The avionics video source simulator of claim 3, wherein the converter unit converts the digital video signal corresponding to the dynamic video signal into the analogue avionics video format at full frame rate of the dynamic video signal.
5. The avionics video source simulator of any one of the preceding claims, wherein the input video signal comprises a signal in PAL 625-lines TV system, NTSC 525-lines TV system, or RS-343 875-lines TV system.
6. The avionics video source simulator of any one of the preceding claims, wherein the static video pattern generator is operable to generate standard video patterns including one or more of a group consisting of a checker-board, a centre-cross, a circle, colour bars from society of motion pictures and television engineers (SMPTE), a grey scale, moving bars, and a multiburst.

7. The avionics video source simulator of any one of the preceding claims, wherein the converter unit is operable to provide the avionics video signals with different, selectable aspect ratios.
8. The avionics video source simulator of claim 7, wherein the aspect ratios include 1:1 or 4:3.
9. The avionics video source simulator of any one of the preceding claims, further comprising an impedance selector unit coupled to the output from the converter unit for providing the avionics video formats with different, selectable source impedances.
10. The avionics video source simulator of claim 9, wherein the source impedances include 10 ohm, 16 ohm, 75 ohm or 93 ohm.
11. The avionics video source simulator of any one of the preceding claims, wherein the converter unit is operable to independently adjust a white level and a synchronisation level of the avionics video formats based on user selection.
12. The avionics video source simulator of claim 11, further comprising one or more digital potentiometers for independently adjusting the white level and the synchronisation level of the avionics video formats.
13. The avionics video source simulator of any one of the preceding claims, further comprising a touch sensitive LCD user interface.
14. The avionics video source simulator of any one of the preceding claims, operable to derive power from a portable notebook or a laptop computer power adapter, or battery pack.
15. A method for avionics video source simulation, the method comprising the steps of:
  - decoding an input video signal into a digital video signal;
  - converting the digital video signal into an analogue avionics video format;

wherein the converter unit is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.

16. A method for avionics video source simulation, the method comprising the step of generating a static video pattern in the avionics video format, wherein the pattern generating is controlled based on a selected one of pre-stored sets of parameters associated with different respective avionics video formats.