

## ABSTRACT

The writing address supply part **210** supplies writing addresses for writing the bits forming bit sequences corresponding to the header **H** contained in a frame to be transmitted or stored and bit sequences corresponding to the data **D**, into the operating memory **220**. The reading address supply part **230** alternately supplies to the operating memory **220** a plurality of addresses for reading a plurality of continuous bits corresponding to the header **H** from the operating memory **220**, and an address for reading 1 bit corresponding to the data **D** from the operating memory **220**, and reads the bit sequence such that the bits forming the bit sequence corresponding to the header **H** are scattered and arranged within the bit sequence forming the data **D**, from the operating memory. In accordance with such an interleaving device, it is possible to individually randomize frames according to their constituent data, and it is possible to transmit the bits that make up such data in a format which is most suited for said data.