METHOD FOR FORMING A POROUS DIELECTRIC MATERIAL LAYER IN A SEMICONDUCTOR DEVICE AND DEVICE FORMED

Field of the Invention

The present invention generally relates to a method for forming a dielectric material layer in an electronic structure and the structure formed and more particularly, relates to a method for forming a porous dielectric material layer in an electronic structure by first forming a non-porous dielectric material layer then partial curing, patterning, and final curing the layer at a higher temperature than that used in the partial curing to transform the non-porous dielectric material into a porous dielectric material, and electronic structure formed by such material.

Background of the Invention

In the recent development of semiconductor devices, the continuing miniaturization of the devices demands the use of electronic materials of more superior properties. For instance, the dielectric material used as an insulating layer in a semiconductor device, must have a lower dielectric constant in order to provide a smaller signal propagation delay. It is

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therefore important to provide electronic materials that have superior insulating properties, such as a reduced dielectric constant for current and future semiconductor device applications.

One of the solutions in providing a dielectric material layer that has improved insulating property, i.e. a lower dielectric constant, is to use a dielectric material that contains voids. A void-filled, or porous dielectric material has a lower dielectric constant than the fully dense void-free version of the same material. However, problems arise in utilizing porous dielectric materials, i.e. when these materials are first formed in an electronic device and then are subjected to a patterning process by reactive ion etching (RIE). The very nature of the desirable porous structure of these materials subject them to excessive etching when exposed to etch gasses utilized in the reactive ion etching process. One solution proposed to solve this problem is to select low-k dielectric materials that have closed porosity. However, any attempt to slice a closed pore material exposes open pores on a new cut surface. Thus, the pores exposed in such a new cut surface would still be subjected to attack by the etch gas used in the reactive ion etching process for patterning the dielectric material layer.

It is therefore an object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure that does not have the drawbacks or shortcomings of the conventional methods.

It is another object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure that is not subjected to attack by reactive ion etching gases during a patterning process.

It is a further object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure by first forming a non-porous dielectric material layer, patterning the layer in a reactive ion etching process and then forming pores in the dielectric material layer.

It is another further object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure by first patterning a non-porous dielectric material layer and then forming pores after the patterning process.

It is still another object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure by first depositing a non-porous dielectric material layer, partially curing the layer at a first low temperature, patterning the non-porous dielectric material layer, and then forming pores and transforming the material layer into a porous structure at a second high curing temperature.

It is yet another object of the present invention to provide a method for forming a porous dielectric material layer in an electronic structure by transforming a dual-phase material into a single-phase, void-filled material at a high curing temperature.

It is still another further object of the present invention to provide an electronic structure that has a layer of porous dielectric material formed therein wherein the layer of porous material has a porosity between about 0.1 vol. % and about 50 vol %.

It is yet another further object of the present invention to provide an electronic structure that has a layer of porous dielectric material formed therein for electrical

insulation wherein the porous dielectric material has a dielectric constant between about 1 and about 3.

Summary of the Invention

In accordance with the present invention, a method for forming a dual damascene interconnect in a semiconductor structure and the structure formed are disclosed.

In a preferred embodiment, a method for forming a dual damascene interconnect in a semiconductor structure can be carried out by the steps of:

providing a pre-processed semiconductor structure;

depositing a layer of a non-porous dielectric material that contains a pore-forming agent on top of said pre-processed semiconductor structure;

depositing a mask layer on said non-porous dielectric material;

forming a cavity for a dual damascene interconnect in said non-porous dielectric material;

filling said cavity for dual damascene interconnect with an electrically conductive metal;

removing said mask layer by an etch process;

curing said semiconductor structure at a temperature sufficiently high so as to volatilize said pore-forming agent from said non-porous dielectric material and forming a porous dielectric material;

planarizing said semiconductor structure; and

depositing a dielectric material layer on top of the semiconductor structure.

In another preferred embodiment, a method for forming a dual damascene interconnect in a semiconductor structure may be carried out by the operating steps of:

providing a pre-processed semiconductor structure;

depositing a layer of a non-porous dielectric material that contains a pore-forming agent on top of said pre-processed semiconductor structure;

depositing a mask layer on said non-porous dielectric material, said mask layer being permeable to said pore-forming agent;

forming a cavity for a dual damascene interconnect in said non-porous dielectric material;

filling said cavity for dual damascene interconnect with an electrically conductive metal;

planarizing said semiconductor structure;

curing said semiconductor structure at a temperature sufficiently high such that said pore-forming agent from said non-porous dielectric material escapes through said mask layer forming a porous dielectric material; and

depositing a dielectric material layer on top of the semiconductor structure.

The present invention is further directed to an electronic structure that has a layer of porous dielectric material formed therein for electrical insulation which includes a pre-processed electronic substrate, a layer of porous

dielectric material that has a porosity between about 0.1 vol. % and about 50

vol. % formed and patterned on the pre-processed electronic substrate, and a conductive metal filling the pattern formed in the layer of porous dielectric material.

In the electronic structure that has a layer of porous dielectric material formed therein for electrical insulation, the porous dielectric material has a dielectric constant of between about 1 and about 3, or preferably between about 1.3 and about 2.6. The conductive metal forms an interconnect between two conductive regions in the electronic structure, the conductive metal may also form an interconnect in a single damascene structure in a semiconductor device, or a dual damascene structure in a semiconductor device. The conductive metal may be copper, aluminum, or other metals such as silver, gold and alloys thereof.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will become apparent from the following detailed description and the appended drawings in which:

Figure 1 is a process flow chart for the present invention novel method for forming a porous dielectric material layer in a single damascene interconnect structure.

Figure 2 is an enlarged, cross-sectional view of a present invention semiconductor structure with an ILD layer and a hard mask layer formed on top.

Figure 3 is an enlarged, cross-sectional view of the present invention structure of Figure 2 with a photoresist layer formed and patterned on top.

Figure 4 is an enlarged, cross-sectional view of the present invention structure of Figure 3 with the hard mask layer patterned.

Figure 5 is an enlarged, cross-sectional view of the present invention semiconductor structure of Figure 4 with the ILD layer patterned and the photoresist layer removed.

Figure 6 is an enlarged, cross-sectional view of the present invention semiconductor structure of Figure 5 with a liner layer deposited and copper plated to fill the via opening.

Figure 7 is an enlarged, cross-sectional view of the present invention semiconductor structure of Figure 6 with the copper layer planarized and a cap layer deposited on top.

Figure 8 is an enlarged, cross-sectional view of the present invention semiconductor structure of Figure 7 after a high temperature anneal to convert the ILD to a porous material.

Detailed Description of the Preferred Embodiment

The present invention discloses a method for forming a dielectric material layer in an electronic structure, and more particularly, discloses a method for forming a porous dielectric material layer in an electronic structure by first forming a non-porous dielectric material layer and then partially curing, patterning, and finally curing the layer at a higher temperature than the partial curing temperature to transform the non-porous dielectric material into a porous dielectric material.

The method can be carried out by first providing a pre-processed semiconductor wafer, depositing a layer of non-porous dielectric material on top of the pre-processed semiconductor wafer, curing the semiconductor wafer at a first temperature of not higher than 350°C, defining and patterning the layer of non-porous dielectric material, and curing the semiconductor wafer at a second temperature higher than the first temperature to transform the non- porous dielectric material into a porous dielectric material. In the preferred embodiment method shown

below, the non-porous dielectric material is substantially a dual-phased material, while the porous dielectric material is substantially a single-phased material. The non-porous dielectric material may further be a physical mixture of a thermally labile material and a thermally stable material.

The present invention method may further be used to form a void-filled dielectric material layer in an electronic structure by first providing an electronic structure that has devices built on top, depositing a layer of a dual-phase dielectric material consisting of a thermally stable material and a thermally labile material on top of the electronic structure, annealing the electronic structure at a first temperature high enough to set and solidify the thermally stable material, but below the volatilization temperature of the thermally labile material, photolithographically defining and patterning the dual-phase dielectric material, and annealing the electronic structure at a second temperature not less than the volatilization temperature of the thermally labile material forming a single phase, void-filled dielectric material. A suitable range for the first annealing temperature may be between about 100°C and about 350°C, a suitable temperature for the second annealing step may be greater than the first temperature.

The invention further discloses an electronic structure that has a layer of porous dielectric material formed therein for electrical insulation which includes a pre-processed electronic substrate, a layer of porous dielectric material that has a porosity between about 0.1 vol. % and about 50 vol. % formed and patterned on the pre-processed electronic substrate, and a conductive metal filling the pattern formed in the layer of porous dielectric material. The porous dielectric material may have a dielectric constant between about 1 and about 3, and preferably between about 1.3 and about 2.6. The conductive metal filling the pattern may be copper, aluminum, silver or gold forming a single damascene or a dual damascene interconnect structure.

The present invention method therefore provides a process which eliminates the problem of the porous structure being etched by reactive ion etching gases during a dielectric material patterning process. The present invention method patterns the porous material prior to driving out the second phase polymeric material such that the problem of uncontrolled etch rates can be avoided. By utilizing the present invention novel method, structures can be built with porous low k materials such as Dendriglass or porous SiLK®-type materials. The problem

occurred in the conventional method is solved by taking advantage of the properties of the porous material prior to driving out the second phase material, i.e. the pore-forming agent, (also known as porogen) since the film is homogeneous and does not etch away in an uncontrolled manner.

Dendriglass is a chemical composition containing MSSQ (methyl-silsesquioxane) and various amounts of a second phase polymeric material, i.e. a pore-forming agent. Dendriglass can be made into a porous film with a dielectric constant in a range between about 1.3 and about 2.6 depending on the amount of the second phase material added to the film. The word "about" used in this writing indicates a range of values of $\pm$ 10% from the average value given. The second phase polymeric material, or the pore- forming agent, is a material that is usually a long chained polymer which can be decomposed and volatilized and driven from the matrix material, i.e. MSSQ, after the film has been cured in a first curing process.

The present invention method can be carried out by first spin-coating a film onto the surface of a silicon wafer and then hot plate curing the film at 200°C, or at a curing temperature of less than 350°C. The film formed is a mixture of MSSQ with an embedded pore-forming agent throughout the film.

The film is usually deposited to a thickness between about 100 nm and about 1000 nm, or preferably between about 300nm and about 600 nm. A hard mask material is then deposited on top of the silicon wafer. The hard mask material may be formed of SiO_2, Al_2O_3, Si_3N_4, SiC and SiCOH. The hard mask layer is used as an etch stop and pattern replication during photolithography and as a polish stop during chemical mechanical polishing (CMP). The hard mask can be composed of more than one layer of material, however, the total thickness is usually less than 250 nm.

A photoresist layer is then applied on top of the wafer and exposed and cured at a temperature of about 200°C. Next, the hard mask layer is etched in a plasma etching process to remove the hard mask in regions defined by the mask in regions on top of the Dendriglass material. Since the Dendriglass film has only been partially cured at the lower temperature, there is no pore formation for attack by the reactive ion gases. Finally, the completely etched structure is heated to a temperature higher than the first temperature, or preferably higher than 400°C to 450°C, for a time period long enough to drive out the second phase polymeric material from the Dendriglass resulting in a porous low-k dielectric film. The usual metal deposition process then proceeds with layers of barrier metal/seed Cu/plated Cu.

The void content in the final porous dielectric film is between about 0.1 vol. % and

about 50 vol. %, or preferably between about 5 vol. % and about 30 vol. % . The final curing temperature should be higher than 250°C, and preferably about 400°C to 450°C.

The present invention novel method can be carried out without the application of the hard mask, i.e. the non-porous Dendriglass material can be covered with a photoresist layer directly, which is then exposed and cured as in the previously described preferred embodiment. In this alternate embodiment, the Dendriglass film is patterned in a suitable plasma gas and then the photomask layer is removed. The patterned Dendriglass film is then heated to a temperature higher than 400°C to 450°C to drive out the second phase polymeric material forming a porous film. Finally, a hard mask film is deposited conformally onto the Dendriglass layer by a technique such as chemical vapor deposition (CVD) which coats both the top surface and the trench and via sidewalls. The hard mask layer can be formed by any of the previously described materials and serves to coat both the top Dendriglass surface required for CMP etch stop, and the via and trench sidewalls required to prevent diffusion pathways into the Dendriglass. A preclean step to preferentially sputter etch any hard mask material at the bottom of the trench can be optionally used prior to

depositing the metal layers. The usual metal deposition processes can then proceed which include the deposition of barrier metal/seed Cu/plated Cu.

The second phase polymeric material, or the porogen material, can be a polystyrene, polymethyl methacrylate or a poly- caprolactone based material. The weight average molecular weight of such polymeric materials ranges between about 2,000 and about 140,000. The decomposition temperature of such polymeric materials is about ≥ 250°C.

Referring now to Figure 1, wherein a process flow chart utilizing the present invention novel method for forming a single- damascene interconnect structure is shown. The processing steps 10~60 can be referenced to Figures 2~8, respectively. In the first step of the process, as shown in step 10 of Figure 2, a semiconductor wafer 70 that has a metal conductive layer 12 deposited on top is first spin-coated with an ILD layer 14 of a silicon oxide material. On top of the ILD layer 14, is then deposited a hard mask layer 16 by a chemical vapor deposition, (CVD) technique. The hard mask can be formed of a suitable material chosen from SiO_2, Al_2O_3, Si_3N_4, SiC, SiCOH or other suitable hard mask material. The purpose of the hard mask layer 16 is to act both as an etch stop and as a pattern

replication layer, during CMP and during photolithography, respectively. The hard mask layer 16 may further be formed by more than one layer of material, even though the total thickness should be less than 250 nm. The metal conductive layer 12 may be suitably formed of a high electrical conductivity material such as copper, or aluminum or alloys thereof.

In the next step of the process, shown in step 20 of Figure 1 and Figure 3, a photoresist layer 18 is applied to the top of the hard mask layer 16, exposed and then cured at a temperature in the order of 200°C. Hard mask layer 16 is then etched in a plasma etching process to remove the mask in those regions defined by the mask on top of the ILD layer 14. In the conventional method, this is the step where the porosity of the Dendriglass causes its demise, since the reactive gases used in etching the hard mask also attack the Dendriglass® and thus leaving behind a glass material with a high dielectric constant, $k \geq 4.0$. The etching step for the hard mask is shown as Step 30 in Figure 1 and in Figure 4.

The non-porous ILD layer 14 is then removed in regions defined in the mask by using a suitable plasma etching method. This is shown in Step 40 of Figure 1 and in Figure 5. The resist layer 18 is further removed after the etching of the ILD layer 14

for the opening 42. As shown in step 35 of Figures 1 and 8, the completely etched structure 70 is then heated to a temperature higher than 250°C, and preferably in the 400° to 450°C range for a time period long enough to drive out the second phase polymeric material, i.e. the porogen material from the Dendriglass resulting in a porous low-k dielectric film. The conversion of the ILD layer from non-porous to porous is therefore accomplished in step 40, or in Figure 5.

In the next step of the process, i.e. step 50 shown in Figure 1 and in Figure 6, a liner material deposition is first conducted to form a liner layer 52 on top of the hard mask layer 16. The liner layer 52 may be deposited of a material such as TaN, TiN, Ti, Ta, or various combinations for achieving adhesion and diffusion barrier properties. On top of the liner layer 52, is normally deposited a copper seed layer, (not shown) by sputtering to facilitate the subsequent electroplating of copper in filling the via opening 72. After the via opening 52 is filled with copper 54, the electronic structure 70 is planarized by a chemical mechanical polishing method to achieve a planar surface 56 on top of the copper via 54. The porogen may be driven out at this point

if desired, as shown in step 65 of Figure 1. A cap layer 58 of an insulating material such as silicon carbide or silicon nitride is then deposited on top to prevent diffusion and to protect the electronic device 70 from mechanical abrasion or other damages.

The present invention novel method for forming a porous dielectric material layer can further be used to form a dual damascene interconnect in a semiconductor structure. The process for forming the dual damascene interconnect in a semiconductor structure can be carried out by incorporating a hard mask layer on top of a non-porous dielectric layer and then, either removing the hard mask layer prior to volatilizing a pore-forming agent or leaving the hard mask layer in the semiconductor structure when the hard mask utilized is permeable to the pore-forming agent.

For instance, in the first method of forming a dual damascene interconnect with a non-permeable hard mask layer, after a layer of a non-porous dielectric material that contains a pore- forming agent is deposited on top of a pre-processed semiconductor structure, a hard mask layer is formed on top of the non-porous dielectric material. A cavity for a dual damascene interconnect in the non-porous dielectric material is then formed, and filled with an electrically conductive metal to form the via and line for the dual damascene interconnect. The

hard mask layer is then removed by an etching process, of either dry or wet etching, prior to a curing process conducted at a temperature sufficiently high, i.e. higher than 250°C, as to volatilize the pore-forming agent from the non-porous dielectric material, thus forming a porous dielectric material for the dual damascene interconnect.

Alternatively, when a hard mask layer is formed which is permeable to the pore-forming agent contained in the non-porous dielectric material, the hard mask layer may be left inside the semiconductor structure during the curing process conducted at high temperature since the pore-forming agent volatilizes and escapes through the permeable hard mask layer. After the formation of the porous dielectric material layer, the semiconductor structure may be planarized and an insulating material layer, i.e. a cap layer, may be deposited on top as a diffusion barrier and protection from abrasion or other physical damages.

A suitable hard mask layer that is permeable to the pore- forming agent may be selected from SiCOH, methyl silsesquioxane (MSSQ), hydrogen silsesquioxane (HSQ) and diamond-like carbon (DLC). A suitable thickness for the permeable hard mask layer should be less than 250 nm.

The present invention method may further be carried out by incorporating the porosity as preformed particulates on the molecular size scale, i.e. to spin-on a solution with insoluble, cross-linked, thermally liable particulates. In this case, the process could be started with a dense two phase material instead of a single phase homogeneous material. The patterning and burnout would be the same as previously stated.

The present invention novel method for forming a porous dielectric layer in a semiconductor structure and the structure formed by the method have been amply described in the above description and in the appended drawings of Figures 1~8.

While the present invention has been described in an illustrative manner, it should be understood that the terminology used is intended to be in a nature of words of description rather than of limitation.

Furthermore, while the present invention has been described in terms of a preferred and alternate embodiment, it is to be appreciated that those skilled in the art will readily

apply these teachings to other possible variations of the inventions.

In addition, the fabrication scheme exemplified for the Dendriglass (porous MSSQ) can be practiced using any other porous dielectric films wherein the remnant material is a higher thermal stability organic material, silica, hydrogen silsesquioxane benzocyclobutene or combinations thereof.

The embodiment of the invention in which an exclusive property or privilege is claimed are defined as follows.

Claims

1. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation comprising:

a pre-processed electronic substrate,

a layer of porous dielectric material having a porosity between about 0.1 vol. % and about 50 vol. % formed and patterned on said pre-processed electronic substrate, and

a conductive metal filling said pattern formed in said layer of porous dielectric material.

2. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said porous dielectric material having a dielectric constant between about 1 and about 3.

3. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said porous dielectric material preferably having a dielectric constant between about 1.3 and about 2.6.

4. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said conductive metal forms an interconnect between two conductive regions in said electronic structure.

5. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said conductive metal forms an interconnect in a single damascene structure in said electronic structure.

6. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said conductive metal forms an interconnect in a dual damascene structure in said electronic structure.

7. An electronic structure having a layer of porous dielectric material formed therein for electrical insulation according to claim 1, wherein said conductive metal is Cu or Al.

8. A method for forming a dual damascene interconnect in a semiconductor structure comprising the steps of:

providing a pre-processed semiconductor structure;

depositing a layer of a non-porous dielectric material that contains a pore-forming agent on top of said pre-processed semiconductor structure;

depositing a mask layer on said non-porous dielectric material;

forming a cavity for a dual damascene interconnect in said non-porous dielectric material;

filling said cavity for dual damascene interconnect with an electrically conductive metal;

removing said mask layer by an etch process;

curing said semiconductor structure at a temperature sufficiently high so as to volatilize said pore-forming agent from said non-porous dielectric material and forming a porous dielectric material;

planarizing said semiconductor structure; and

depositing a dielectric material layer on top of the semiconductor structure.

9. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8, wherein said non-porous dielectric material is selected from the group consisting of methyl-silsesquioxane (MSSQ), benzocyclobutene, hydrogen silsesquioxane (HSQ), silica and aromatic thermoset polymers such as SiLK® or Flare®.

10. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8, wherein said pore-forming agent is a polymeric material.

11. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8, wherein said mask layer is selected from the group consisting of SiO_2, Al_2O_3, Si_3N_4, SiC and SiCOH.

12. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8, wherein said mask layer is deposited to a thickness of not greater than 100 nm.

13. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8 further comprising the step of removing said mask layer by a dry etching or a wet etching technique.

14. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8 further comprising the step of curing said semiconductor structure at a temperature greater than 250°C.

15. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8 further comprising the step of depositing said layer of non-porous dielectric material that contains a pore-forming agent by a spin coating technique to a thickness between about 100 nm and about 1,000 nm.

16. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 8, wherein said porous dielectric material formed has a porosity between about 0.1 vol. % and about 50 vol. %.

17. A method for forming a dual damascene interconnect in a semiconductor structure comprising the steps of:

providing a pre-processed semiconductor structure;

depositing a layer of a non-porous dielectric material that contains a pore-forming agent on top of said pre-processed semiconductor structure;

depositing a mask layer on said non-porous dielectric material, said mask layer being permeable to said pore-forming agent;

forming a cavity for a dual damascene interconnect in said non-porous dielectric material;

filling said cavity for dual damascene interconnect with an electrically conductive metal;

planarizing said semiconductor structure;

curing said semiconductor structure at a temperature sufficiently high such that said pore-forming agent from said non-porous dielectric material escapes through said mask layer forming a porous dielectric material; and

depositing a dielectric material layer on top of the semiconductor structure.

18. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17 further comprising the step of depositing a non-porous dielectric material that contains a pore-forming agent by a spin coating technique.

19. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17 further comprising the step of depositing a non-porous dielectric material that contains a pore-forming agent to a thickness between about 100 nm and about 1,000 nm.

20. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17, wherein said non-porous dielectric material is selected from the group consisting of methyl-silsesquioxane (MSSQ), benzocyclobutene, hydrogen silsesquioxane (HSQ), silica and aromatic thermoset polymers such as SiLK® and Flare®.

21. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17, wherein said pore-forming agent is a material of polymeric nature that volatilizes at a temperature higher than 250°C.

22. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17, wherein said mask layer being permeable to said pore-forming agent is selected from the group consisting of SiCOH, methyl silsesquioxane (MSSQ), hydrogen silsesquioxane (HSQ) and diamond-like carbon (DLC).

23. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17 further comprising the step of depositing said mask layer to a thickness of less than 100 nm.

24. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17 further comprising the step of curing said semiconductor structure at a temperature greater than 250°C.

25. A method for forming a dual damascene interconnect in a semiconductor structure according to claim 17 further comprising the step of forming said porous dielectric material that contains between about 0.1 vol. % and about 50 vol. % porosity.