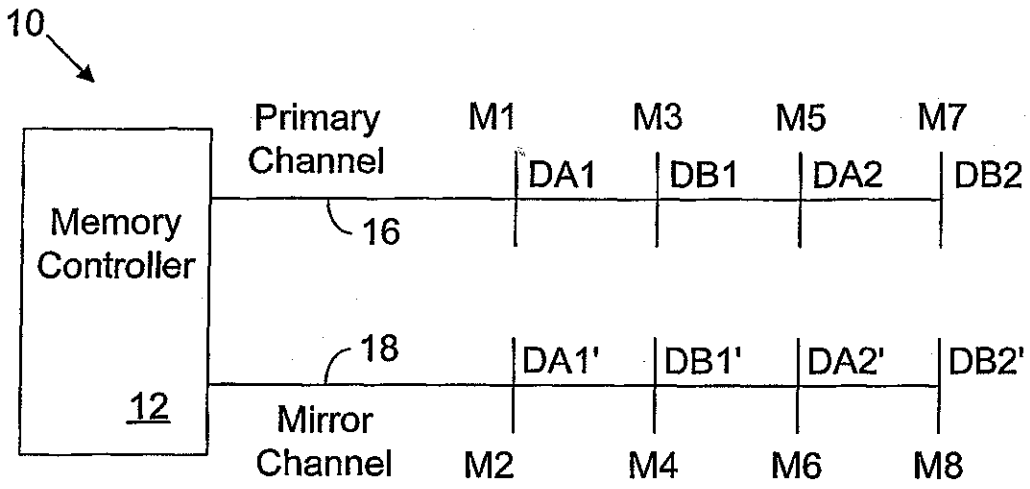

FIG. 1
(Prior Art)

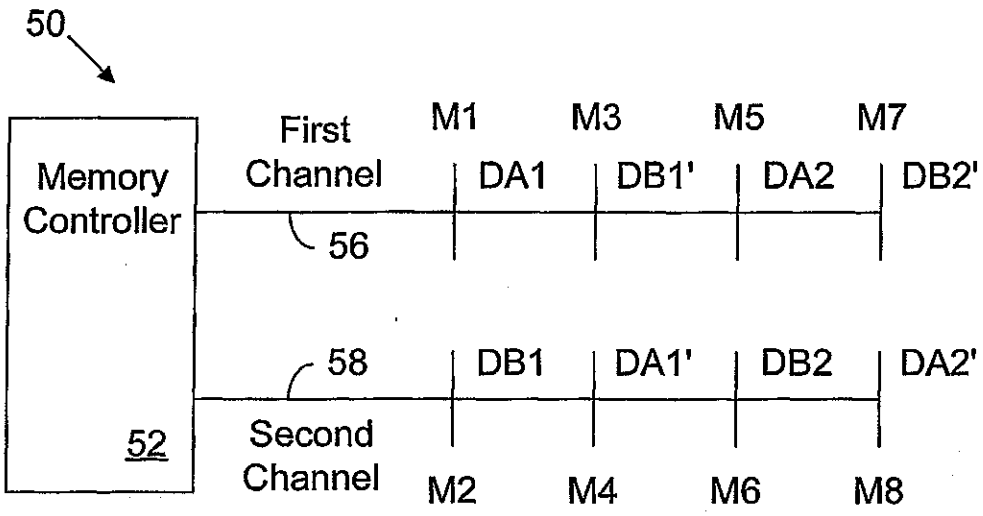

FIG. 2

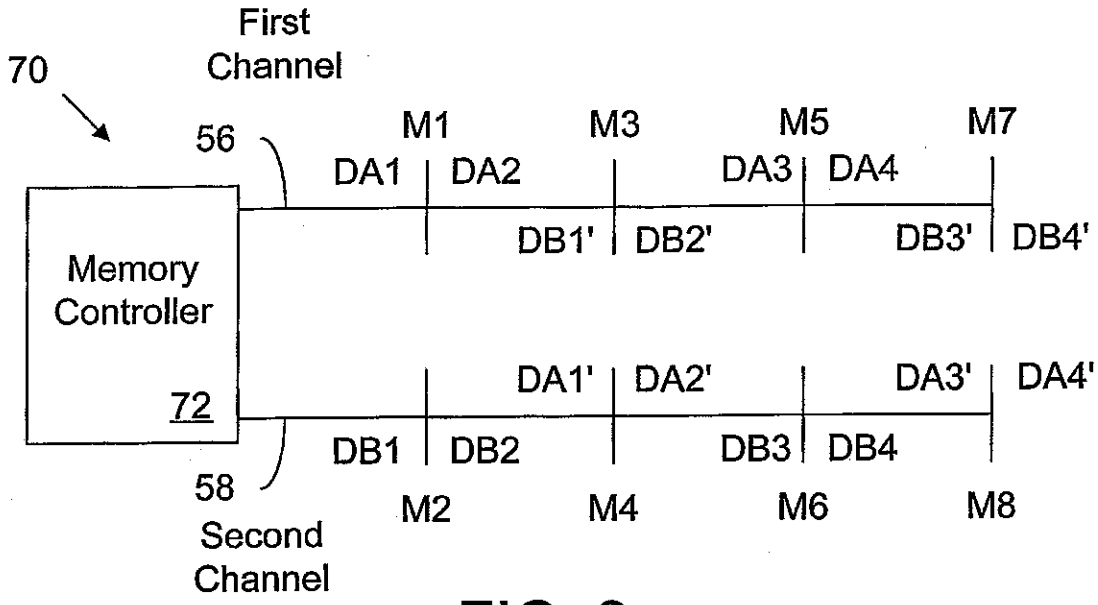
70
First
Channel
56
M1
M3
M5
M7
DA1
DA2
DA3
DA4
DB1'
DB2'
DB3'
DB4'
Memory
Controller
72
DA1'
DA2'
DA3'
DA4'
DB1
DB2
DB3
DB4
58
Second
Channel
M2
M4
M6
M8

FIG. 3

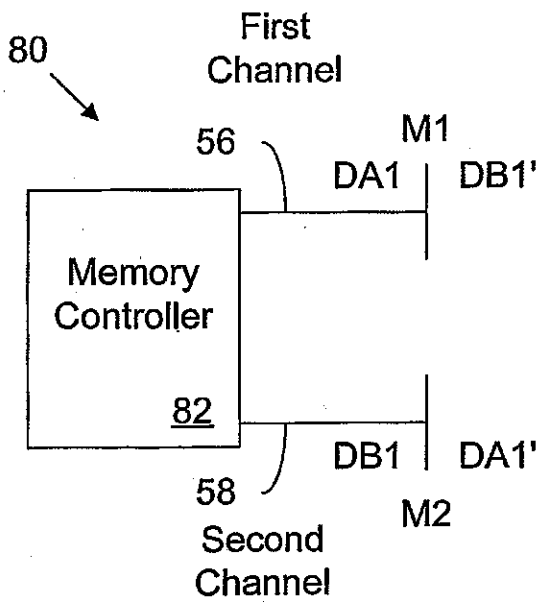
80
First
Channel
56
M1
DA1
DB1'
Memory
Controller
82
DB1
DA1'
58
M2
Second
Channel

FIG. 4

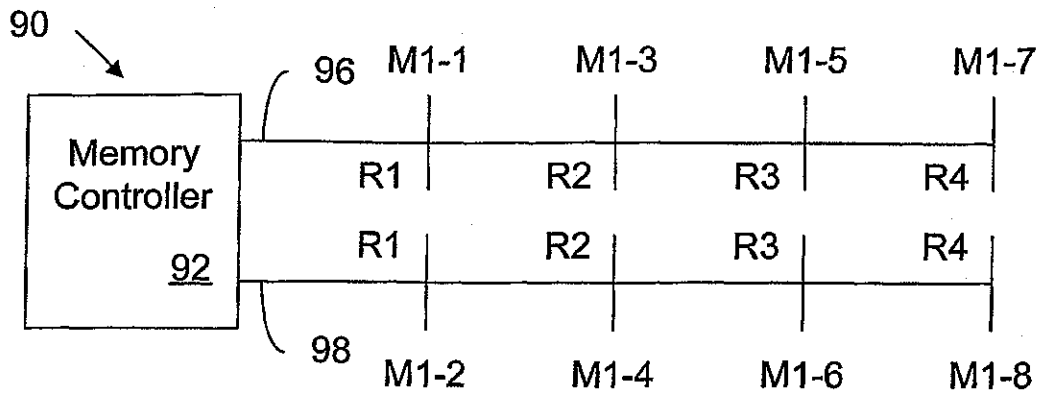

FIG. 5

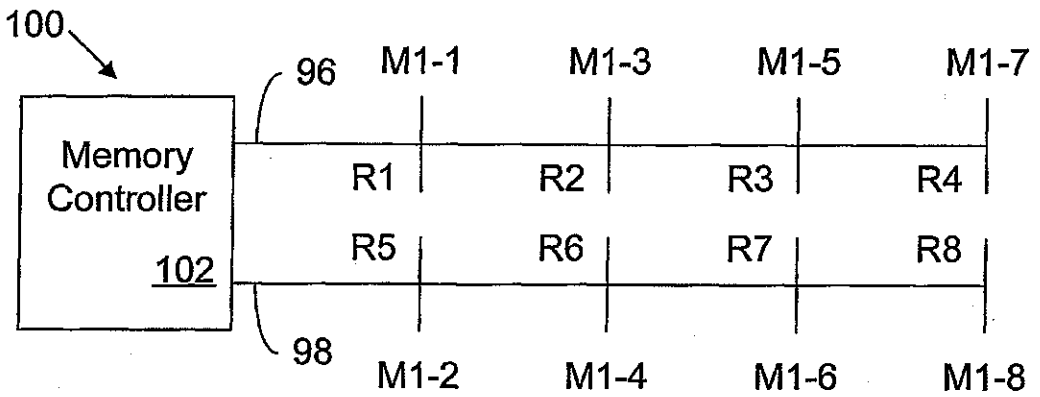

FIG. 6

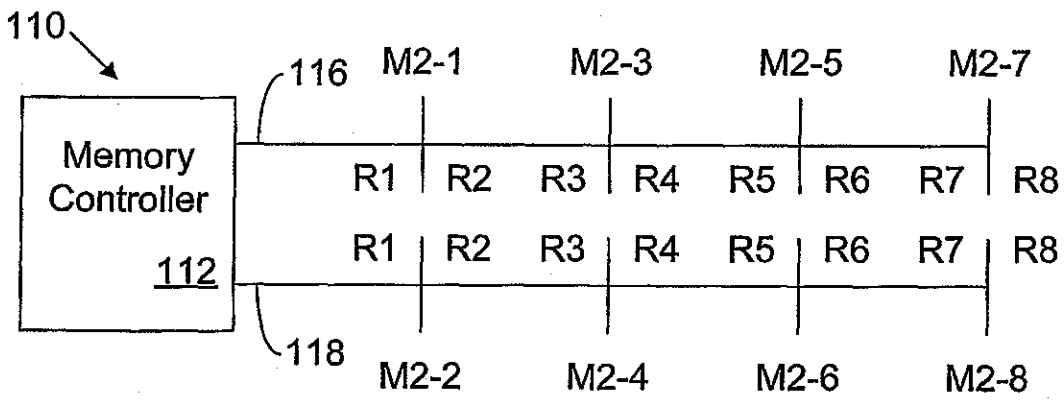

FIG. 7

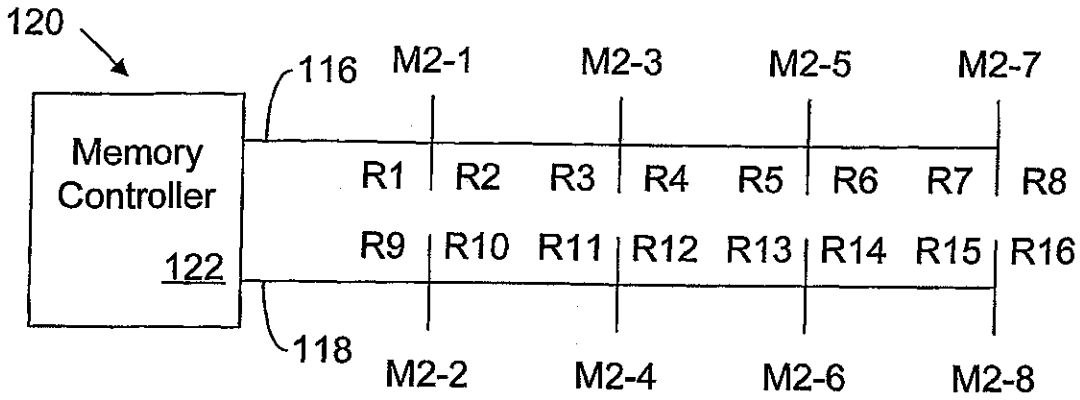
120
116
M2-1
M2-3
M2-5
M2-7
Memory Controller
122
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
118
M2-2
M2-4
M2-6
M2-8

FIG. 8

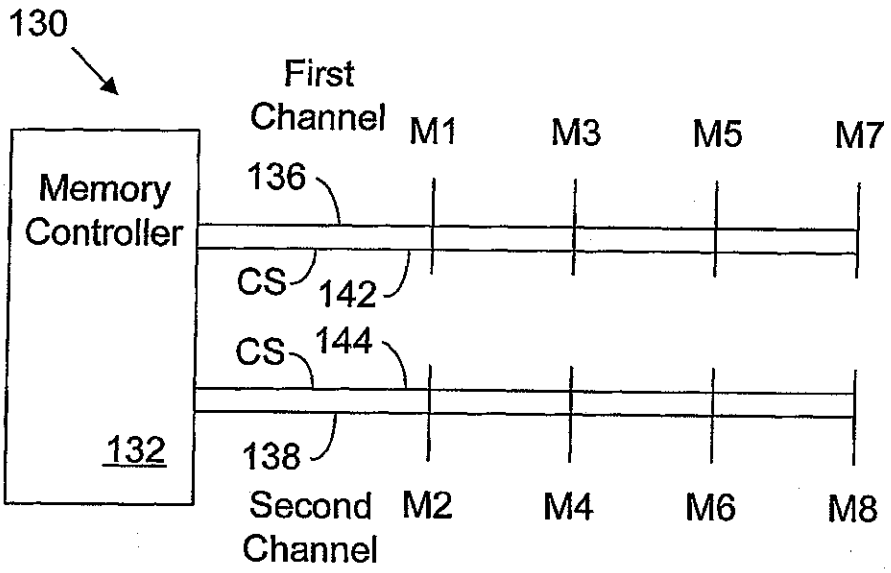
130
First Channel
M1
M3
M5
M7
Memory Controller
136
CS
142
CS
144
132
138
Second Channel
M2
M4
M6
M8

FIG. 9

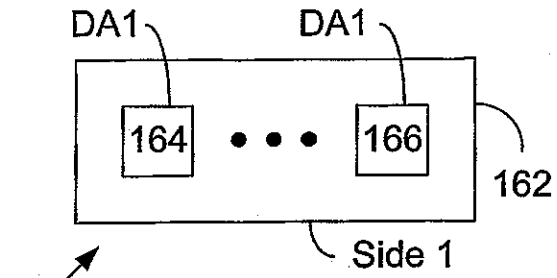

FIG. 10

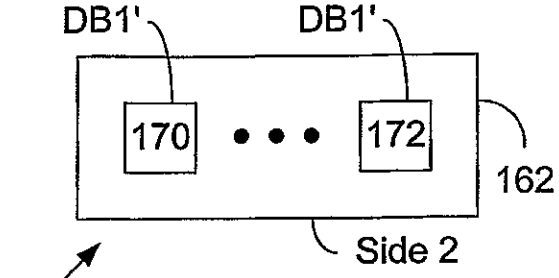

FIG. 11

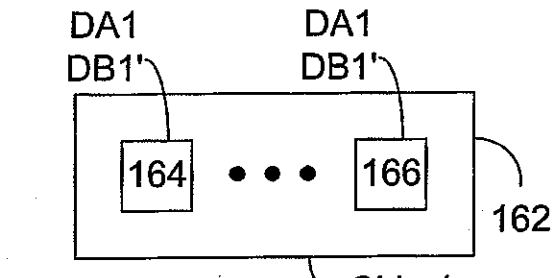

FIG. 12

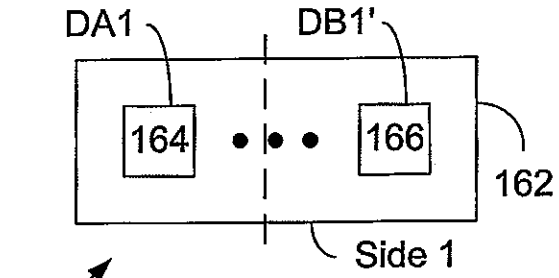

FIG. 13

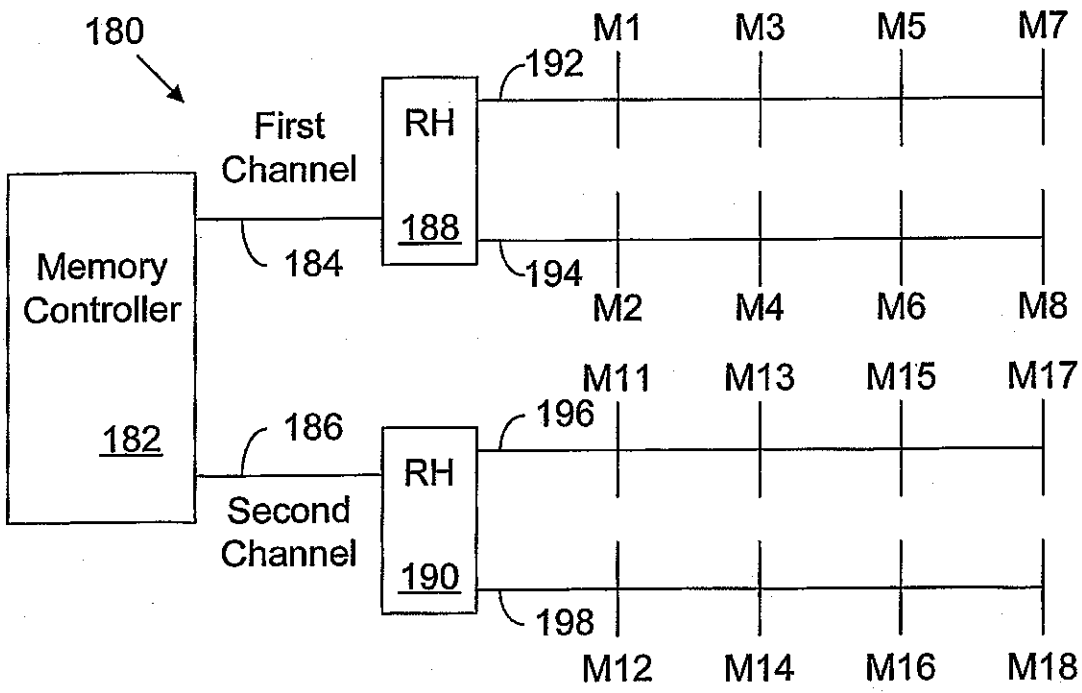

FIG. 14

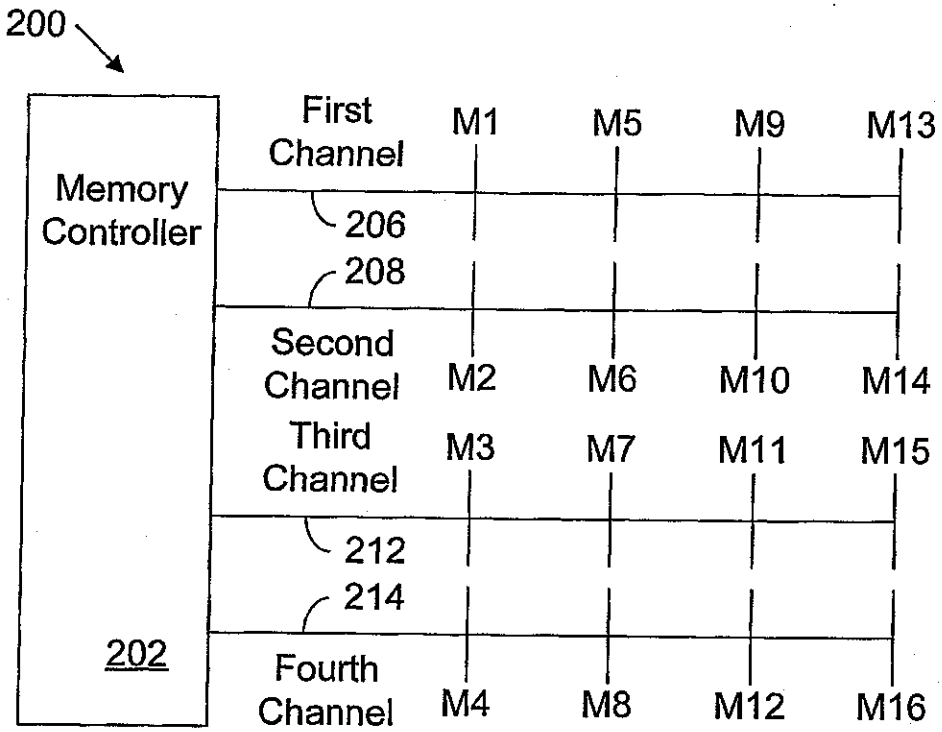
200
Memory Controller
202
First Channel
206
208
Second Channel
Third Channel
212
214
Fourth Channel
M1
M5
M9
M13
M2
M6
M10
M14
M3
M7
M11
M15
M4
M8
M12
M16

FIG. 15

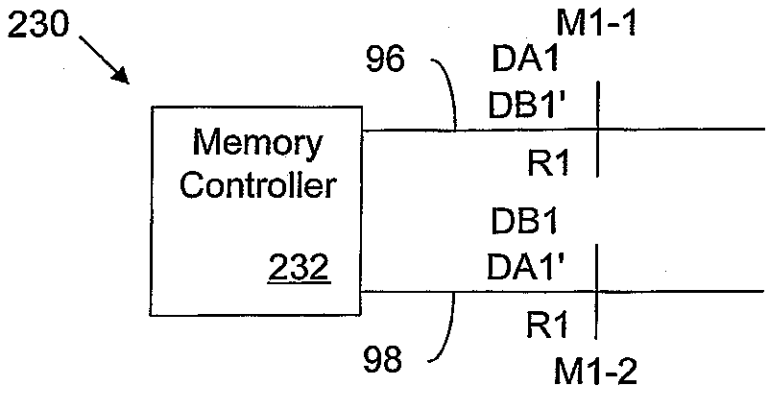

FIG. 16

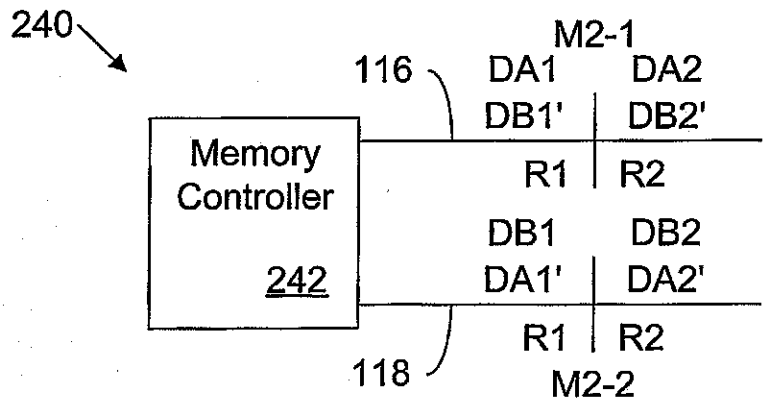

FIG. 17

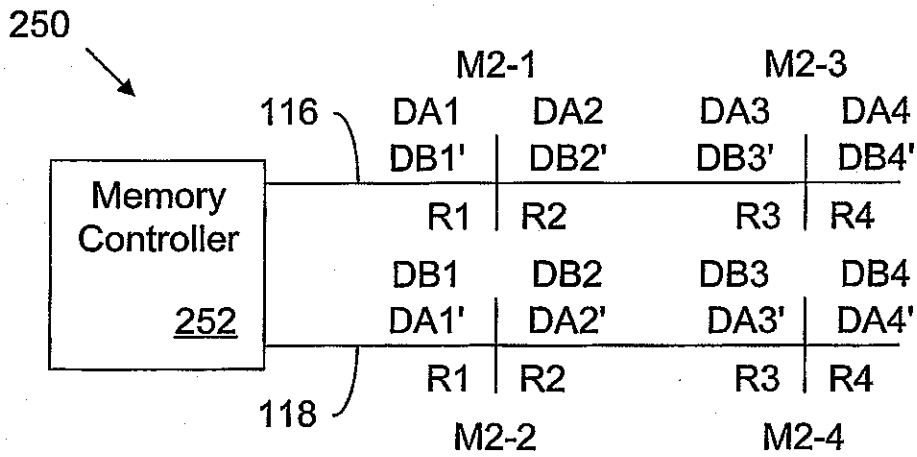

FIG. 18

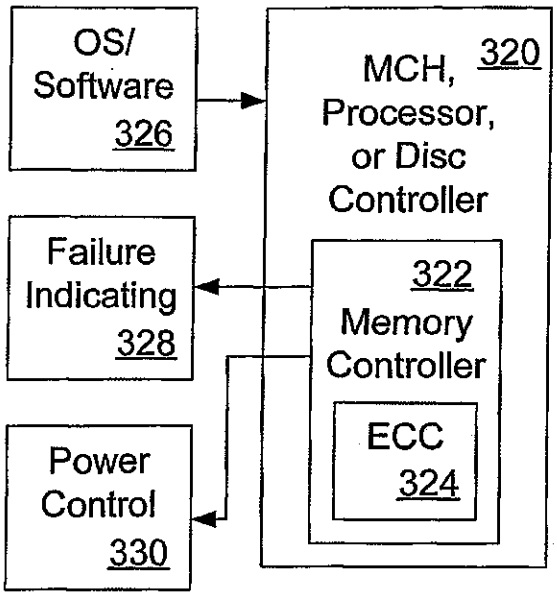

FIG. 19

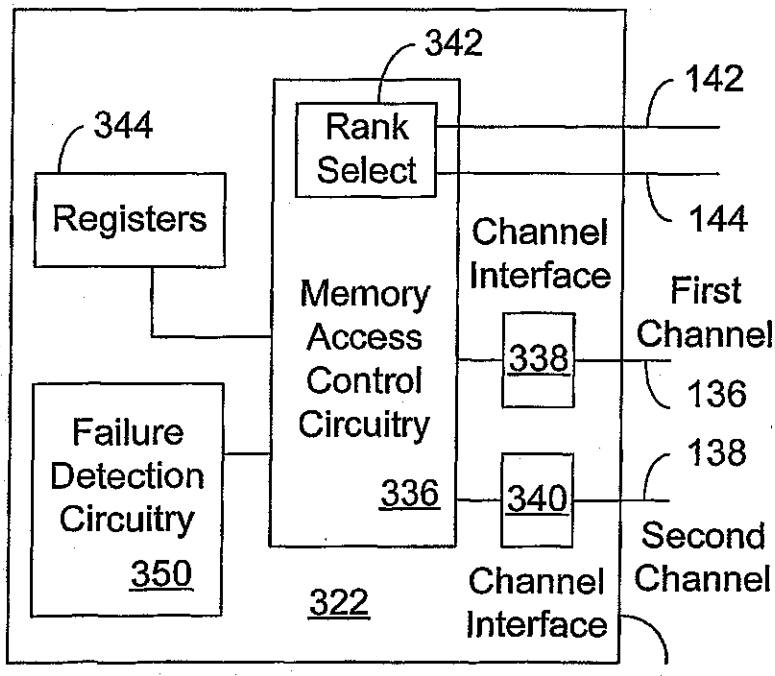

FIG. 20

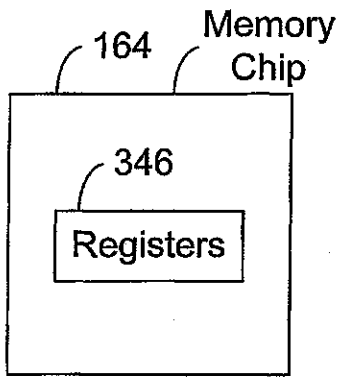

FIG. 21

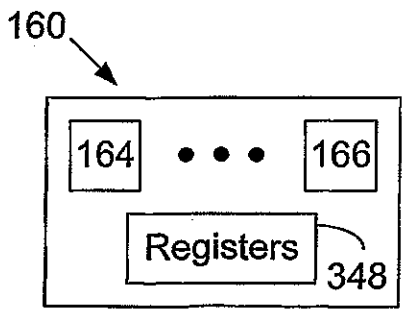

FIG. 22

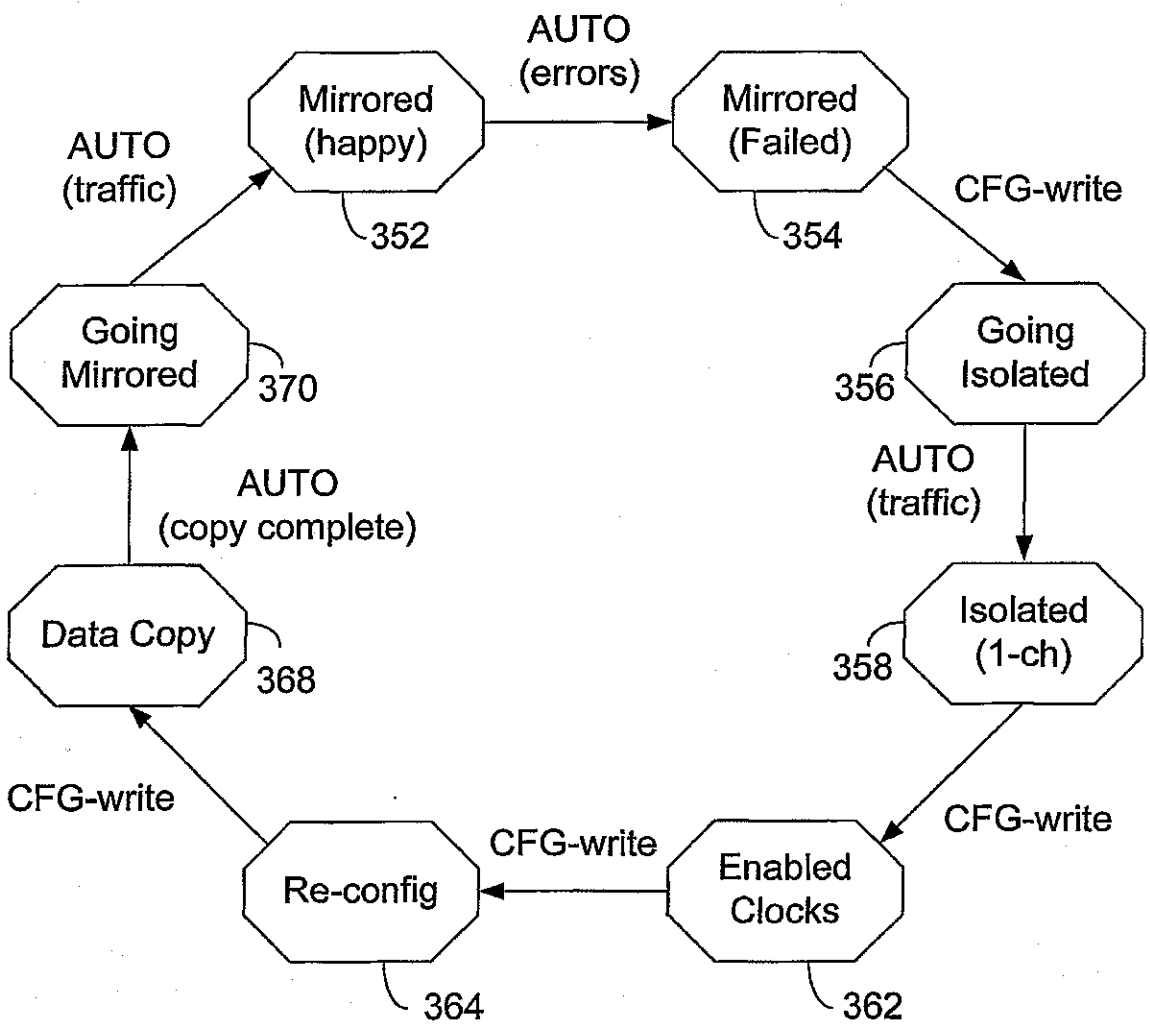
Mirrored (happy)
352
AUTO (errors)
Mirrored (Failed)
354
CFG-write
Going Isolated
356
AUTO (traffic)
Isolated (1-ch)
358
CFG-write
Enabled Clocks
362
CFG-write
Re-config
364
CFG-write
Data Copy
368
AUTO (copy complete)
Going Mirrored
370
AUTO (traffic)

FIG. 23