

UTILIZING ELECTROCHEMICAL ANALYTICAL METHODS TO MEASURE
PLATING BATH BREAKDOWN PRODUCTS SUCH AS MPSA TO DETECT
CHEMISTRY PROBLEMS PRIOR TO HAVING AN IMPACT ON WAFER LEVEL
PROCESS PERFORMANCE

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BACKGROUND

[0001] Microelectronic devices such as semiconductor devices are generally fabricated on and/or in substrates or wafers. In a typical fabrication process, one or more layers of metal or other conductive materials are formed on a wafer in an electroplating processor. The processor may have a bath of electrolyte held in vessel or bowl, with one or more anodes in the bowl. The wafer itself may be held in a rotor in a head movable into the bowl for processing and away from the bowl for loading and unloading. A contact ring on the rotor generally has a large number of contact fingers that make electrical contact with the wafer.

15 [0002] Many advanced microelectronic devices include through silicon via (TSV) features. A TSV is a vertical electrical interconnection usually passing completely through the wafer or die, which may or may not actually be made of silicon. TSV features are used to create three dimensional electronic structures and packages by providing electrical connections between vertically stacked semiconductor dies. Use of TSV's allows for very high-density integrated circuits. The electrical characteristics of the interconnections are also improved because generally TSV's are shorter and less inductive than alternative interconnections. This results in faster device operation and reduced effects from undesirable inductive or capacitive characteristics of the interconnections.

25 [0003] TSV's tend to have high aspect ratios, as they are essentially tall narrow micro-scale columns of metal, generally copper, formed in a hole in silicon or other substrate material. TSV's may be formed by electroplating copper from the bottom up. Achieving proper fill of the TSV is technically challenging for several reasons, including the micro-scale dimensions of the TSV, high aspect ratios, and other factors.

30 [0004] Historically, the processes and chemistries used for plating fill of TSV have exhibited instability as the plating bath ages, which directly affects the microelectronic manufacturing process. Since the plating bath is generally still within specification at failure, the reason for bath failure has not been well understood.

[0005] Accordingly, improved systems and methods for controlling quality of electroplating a wafer with TSV features are needed.

SUMMARY

[0006] In one aspect, a method of controlling quality of electroplating a wafer
5 having one or more through silicon via (TSV) features includes placing a wafer in contact with a bath, where the bath includes an accelerator, and one or more suppressing components, such as a suppressor or leveler, passing electrical current from one or more anodes through the bath and through a conductive layer on the wafer, monitoring a voltage of the one or more anodes by one or more computer processors, and declaring an upcoming
10 failure event of the bath based on a predetermined threshold of voltage by the one or more computer processors.

[0007] In some embodiments, the upcoming failure event is determined by detecting an inflection point in the voltage. In some embodiments, the predetermined threshold is based on a slope of change in the voltage. In some embodiments, the upcoming
15 failure event occurs when the slope of the change in voltage is greater than the predetermined threshold. In some embodiments, the predetermined threshold is a slope of about 0.1 or less.

[0008] In some embodiments, the method further includes remedying the bath before the upcoming failure event. In some embodiments, remedying the bath comprises
20 replacing the bath. In some embodiments, remedying the bath comprises controlling formation of 3-mercaptopropanesulfonic acid (MPSA). In some embodiments, controlling formation of MPSA comprises reducing the MPSA in the bath to a concentration of less than about 10 ppm. In some embodiments, remedying the bath comprises stopping the electroplating until a predetermined time has elapsed. In some embodiments, the
25 predetermined time is between about 8 to about 30 hours.

[0009] In some embodiments, the upcoming failure event of the bath comprises a concentration of greater than about 1.0 ppm of 3-mercaptopropanesulfonic acid (MPSA). In some embodiments, the upcoming failure event of the bath comprises a drop or an oscillation of the voltage. In some embodiments, the upcoming failure event of the bath
30 comprises formation of one or more gaps in the one or more TSV features, underfilling of the one or more TSV features, or a combination thereof.

[0010] In another aspect, disclosed herein is a method of electroplating a wafer with one or more through silicon via (TSV) features, the method including placing a wafer

into contact with a bath, wherein the bath comprises an accelerator, and one or more suppressing components, such as a suppressor or leveler, passing electrical current from one or more anodes through the bath and through a conductive layer on the wafer, monitoring a voltage of the one or more anodes, and declaring an upcoming failure event of the bath based on an inflection point in the voltage by the one or more computer processors.

[0011] In some embodiments, the upcoming failure event of the bath includes a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA). In some embodiments, the upcoming failure event of the bath includes formation of one or more gaps in the one or more TSV features, underfilling of the one or more TSV features, or a combination thereof.

[0012] In yet another aspect, disclosed herein is a method of electroplating a wafer with one or more through silicon via (TSV) features, the method including placing a wafer in contact with a bath, wherein the bath comprises an accelerator one or more suppressing components, such as a suppressor or leveler, passing electrical current from one or more anodes through the bath and through a conductive layer on the wafer, monitoring a voltage of the one or more anodes, and declaring an upcoming failure event of the bath based on a slope in the change in voltage being greater than a predetermined threshold of the voltage.

[0013] In some embodiments, the predetermined threshold is a slope is about 0.1 mV/s or less.

[0014] In some embodiments, the upcoming failure event of the bath comprises the bath having a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA).

[0015] This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This summary is not intended to identify key features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

DESCRIPTION OF THE DRAWINGS

[0016] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0017] FIGURE 1A is a perspective view of an example processor in accordance with the present technology;

[0018] FIGURE 1B is a cross-sectional view of the processor shown in FIG. 1, in accordance with the present technology;

5 [0019] FIGURE 2 is an auxiliary tool, in accordance with the present technology.

[0020] FIGURES 3A-3B are graphs of voltages for multiple baths with and without the presence of 3-mercaptopropanesulfonic acid (MPSA), in accordance with the present technology;

10 [0021] FIGURES 4A-4C are graphs of voltages for baths with an increased age, in accordance with the present technology;

[0022] FIGURE 5 is a graph of voltages for multiple remedied baths, in accordance with the present technology;

[0023] FIGURE 6 is a method for controlling quality of a bath, in accordance with the present technology; and

15 [0024] FIGURE 7 is another method for controlling quality of a bath, in accordance with the present technology.

DETAILED DESCRIPTION

[0025] The systems and methods described herein are directed towards declaring (or predicting) an upcoming event of bath failure and remedying the bath even before such a failure occurs. In this manner, the bath may be replaced before the quality of the electroplating process degrades, allowing for reduced waste, increased TSV quality, and saved time.

20 [0026] Detection of upcoming failure events of a bath has been a challenge in TSV plating baths. As used herein, bath failure can be defined in several ways. For example, in some embodiments, bath failure or insufficient quality can be defined as a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA). In some embodiments, bath failure is determined based on a drop or an oscillation of a detected voltage as described herein. In some embodiments, bath failure exhibits itself when one or more gaps in the one or more TSV features are formed, one or more TSV features are underfilled, or a combination thereof. In practice, there is a common trend that a fresh bath performs well, but with continued reductive plating (to 0.45 A Hr/L) the bath is more likely to fail.

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[0027] The conventional way to detect an ongoing bath failure (i.e., not an upcoming failure event) is to plate a wafer in the tool and perform X-ray imaging/cross section imaging using focused ion beam (FIB) to detect voids in TSVs. However, wafer availability for imaging is usually limited. This is an expensive and time-consuming process.

[0028] A chrono-potentiometric method was developed for detecting bath failure, as explained in US Pat. Pub. No. 20140262794A1, the entire contents of which are hereby incorporated by reference. Bath failure was determined to be caused by domination of an accelerator in the bath. Accordingly, suppression is lost over plating time, leading to conformal growth and voids in the TSV features.

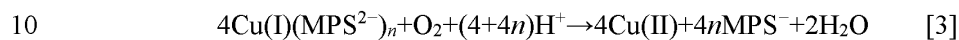
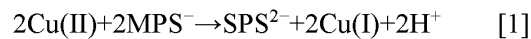
[0029] In one form of a bench top method, a chrono-potentiometric measurement with a long-time scale (3600 seconds) was used to detect bath failure. The one-hour time scale allows for adsorption kinetics for organic additives during the plating step to be fully accounted for. In general, plating the TSV takes between 10-180 minutes (e.g., for 3×50 to SOx 150 features). A fresh bath is highly suppressive immediately after immersion of the Cu-plated Pt electrode with a final potential at 3600 s from first use of the bath, around -240 mV. This voltage may be measured with anodes disposed in the bath, as shown and explained in FIGs. 1A-2. In the context of this specification, suppression refers to the combined suppressing effect of the suppressor and the leveler in the bath.

[0030] Organic additives are conventionally included in the plating bath to improve quality of TSV plating. A suppressor additive (usually a high-molecular-weight polyalkene glycol such as PEG) adsorbs strongly on the Cu cathode surface, in the presence of chloride ions, to form a film that sharply increases the over-potential for Cu deposition. An accelerator additive counters the suppressive effect of the suppressor to provide the accelerated deposition within trenches and vias needed for bottom-up filling. SPS (sodiumsulfopropyl disulfide) has been used as an accelerator. MPSA (3-mercaptopropylsulfonic acid) is a known bi-product or breakdown product of SPS. A leveler additive, such as amine and heterocyclic compounds, is also used in TSV plating. The leveler is also a strong suppressor.

[0031] The chrono-potentiometric measurements of the bath samples demonstrated quick adsorption of suppressor and leveler to the electrode surface, followed by replacement of the suppressor and leveler by the accelerator. With continuous reductive plating, up to 0.347 A Hr/L, the bath becomes less suppressive (about 25 mV less) than the

fresh bath. This is because the SPS (accelerator) is reduced to MPSA or Cu (I) thiolate, which facilitates Cu deposition. When the bath is aged to 0.45 A Hr/L, test data shows an increased rate of displacement of suppressor and leveler by accelerator and competitive adsorption or oscillation behavior. This oscillation behavior correlates directly with failure of the bath.

[0032] The key chemical reactions describing the oxidative thiol-disulfide relationship at the root of the instability are:



[0033] In a bench method, a bath sample of 200 ml was taken from the bath of a processor (such as a processor 20) having a total electrolyte volume of about 80 L. The term processor in this context refers to a processor for electroplating wafers with TSV features. In some embodiments, the processor includes a rotor in a head. The head may be lowered to position a wafer on the rotor into contact with catholyte in the bowl above a membrane. In some embodiments, anolyte and one or more anodes are in the bowl below the membrane. An agitator or paddle may optionally be provided in or at the top of the bowl. In some embodiments, a processor for electroplating with a different configuration may be used.

[0034] A three-electrode potentiostat was used to pass a constant current through the sample, while monitoring potential over time. Electrical potential gradually rose from about -250 mV to about -180 mV until about 2000 seconds when the potential spiked up to about -110 mV and then dropped rapidly back down to about -250 mV at about 2400 seconds. A TSV test wafer plated with this bath after 2400 seconds showed voids.

[0035] In existing plating processors designed for TSV applications, the plating process tends to be unstable, with under-filled TSVs and/or voids occurring in TSVs after running even a relatively small number of wafers in a fresh bath. This instability is linked to the presence of accelerator SPS and its by-product MPSA in the bath, leading to field depolarization or loss of suppression, with electrical current shifted from the vias or trenches to the field or top surface of the wafer. In the context of this specification, suppression refers to the suppressing effect of a suppressor alone, the suppressing effect of a leveler alone, and the combined suppressing effect of the suppressor and the leveler.

[0036] In a tool or system scale set up, a test wafer having a copper blanket seed layer may be loaded into the processor. The potential of each anode in the processor may be monitored to sense changes in the bath chemistry and the onset of TSV voids or under fill can be detected. An oscillation or drop in cell voltage occurs when surface suppression is lost or reduced. If this occurs while a TSV is still filling with copper, voiding or under fill will result. In some embodiments, voiding is the primary failure mode. Less common overfill and underfill failure modes may also occur, especially if the failure occurs near the end of the process when the TSV feature is already largely completed. In this case, slight underfill may occur.

10 [0037] However, the chrono-potentiometric process has drawbacks. For example, the method described above only detects bath failure, not upcoming failure events of the bath. With the novel methods disclosed herein, upcoming failure events of the bath may be declared prior to bath failure, allowing for the bath to be remedied before the electroplating process is affected and before defects in TSV start occurring.

15 [0038] FIG. 1A is a perspective view of an example processor in accordance with the present technology. FIG. 1B is a cross-sectional view of the processor shown in FIG. 1A, in accordance with the present technology. FIGs. 1A-1B show an example of a processor 20 which may be provided with a bath failure detection system. In some embodiments, the processor 20 has a rotor 24 in a head 22. The head 22 may be lowered to position a wafer 40 on the rotor 24 into contact with catholyte in the bowl 26 above a membrane 32. In some embodiments, anolyte and one or more anodes 28 are in the bowl 26 below the membrane 32. An agitator or paddle 36 may optionally be provided in or at the top of the bowl 26.

25 [0039] In operation, the processor controller 50 monitors the voltage of each anode 28. Upon detection of an abrupt change in voltage, the controller declares that an upcoming failure event of the bath has occurred. The controller 50 may then sound an alert or alarm, and optionally shut down. In some embodiments, this function may be added to the processor 20 via software used in programming the controller 50. The methods described above may be used in processors with or without a membrane 32.

30 [0040] As described, the electroplating system for processing a wafer 40 having TSV features may include a bowl 26 for holding a bath of electrolyte and one or more anodes 28 in the bowl 26. In some embodiments, a wafer holder 36 has a contact ring 34 configured to make electrical contact with the wafer 40, with a cathode (not pictured in

FIGs. 1A-1B) electrically connected to the contact ring 34. A voltage monitor may monitor voltage between one or more of the anodes 28 and the contact ring 34. The controller 50 may be linked to the voltage monitor, with the controller 50 declaring an upcoming failure event of the bath based on a change in voltage, as described in detail herein.

5 **[0041]** FIG. 2 is an auxiliary tool 100, in accordance with the present technology. In some embodiments, in lieu of, or in addition to the controller 50 and/or the voltage monitor of the processor 20, an external, auxiliary tool 100 may be used. In some embodiments, the auxiliary tool 100 is configured to monitor the voltage between the one or more anodes 28 that are electrically coupled to the wafer 40. The processor 20 of the
10 auxiliary tool 100 includes suitable bath, analogous to the bath explained with reference to FIGs. 1A and 1B. The anodes 28 and wafer 40 are shown in dashed lines as they are internal to processor 20. In some embodiments, the wafer 40 is optional, and the electrical measurements can be completed with another set of electrodes 27 in place of the wafer. In some embodiments, a computing device 90 is communicatively coupled to the processor
15 20, such as through a wireless connection or a wired connection. In some embodiments, the auxiliary tool collects the voltage measurements of its independent anodes (or electrodes) 27, either through the controller 50, or directly from the anodes 27 themselves. This can allow the auxiliary tool 100 to run independently of whether a wafer 40 is being processed in the chamber. This also allows for use of a lower current and longer times than
20 the wafer recipe making for a more sensitive bath analysis.

[0042] In some embodiments, the auxiliary tool 100 may also function as a voltage monitor. In some embodiments, the auxiliary tool 100 includes a computing device 90 that is a desktop computer, laptop, tablet, or the like. In some embodiments, the computing device 90 is configured to display the measured voltage, such as shown in FIGs.
25 3A-5.

[0043] In operation, the auxiliary tool 100 receives the voltage measured by the one or more anodes 28. In some embodiments, the auxiliary tool 100 also includes a voltage monitor. In such embodiments, the auxiliary tool 100 monitors the voltage of the independent electrodes 27 and provides an alert when an upcoming failure event is
30 detected, as described herein.

[0044] As used herein, the phrase “one or more controllers” refers to the controller 50 of the processor 20, computing device 90, the auxiliary tool 100, or a combination thereof. In some embodiments, only the controller of the processor 50 may

be used. Similarly, in other embodiments, only the computing device 90 may be used. In yet further embodiments, the controller 50 of the processor 20 and the computing device 90 may be used together to monitor voltage and/or declare an upcoming failure event.

[0045] FIGs. 3A-3B are graphs of voltages for multiple baths with and without the presence of 3-mercaptopropanesulfonic acid (MPSA), in accordance with the present technology. On the horizontal axis of both FIGs. 3A-3B is time in seconds. On the vertical axis is voltage (V_f (V vs. Ref.)). Each line on the graph represents a tested bath. The curved arrow shown in the bottom left corner of FIGs. 3A-3B represents increasing MPSA concentration.

[0046] FIG. 3A shows two failing baths (dotted line and dashed line) and two baths that have not failed (dot-dash line and solid line). The solid line represents a bath having no MPSA. As shown, the solid line maintains a steady slope at a first time d_2 and a second time D_2 . The solid line (i.e., bath having no MPSA) does not exhibit an inflection point at either the first time d_2 or the second time D_2 . As shown in the bottom right hand insert of FIG. 3A, this results in properly filled TSV features.

[0047] In contrast, the dashed line represents a bath having a high MPSA concentration (such as between about 1.0ppm and 10 ppm of MPSA). While the voltage at a first time d_1 maintains a small slope with respect to increasing time axis, at a second time D_1 there is an inflection point. As used herein, the term inflection point is defined as a point of a curve at which a change in the direction of curvature occurs. Mathematically speaking, a second derivative of the voltage over time is zero or close to zero at the inflection point. Here, there is an inflection point at D_1 , which indicates an upcoming failure event of the bath. As the bath was not remedied after the inflection point, the bath then fails, as shown by the voltage drop. As shown in the top right insert, such a failure of the bath results in underfilling of the TSV feature of a wafer. Methods described herein can detect the upcoming failure event of the bath (i.e., the inflection point in the monitored voltage and/or a slope in voltage exceeding a predetermined threshold), which then enables remedying the bath, as described herein, to prevent the underfilling shown in FIG. 3A.

[0048] FIG. 3B shows four additional baths as traces, including three baths that failed (the thin dashed line, the dot-dash line, and the thick dashed line) and one bath that did not fail (the solid line). As MPSA increases, the bath is more likely to fail, as explained above. As shown in FIG. 3B, in each bath that failed, inflection points were present in their respective monitored voltages at respective times D_1 , D_2 , and D_4 . In contrast, the solid

line representing the bath that did not fail does not exhibit an inflection point along the entire timeline of the plating.

[0049] Further, in some embodiments, an upcoming event of bath failure may be detected before an inflection point is detected. In some embodiments, the upcoming event of bath failure may be determined by comparing monitored voltage to a predetermined threshold. In some embodiments, the predetermined threshold is based on a slope of change in the voltage. Accordingly, an upcoming event of bath failure may be declared when the slope of the change in voltage is greater than the predetermined threshold. As shown in FIG. 3B, in each bath that failed, slopes greater than the predetermined threshold were detected as the slopes S1, S2, and S3.

[0050] In some embodiments, the predetermined threshold is a slope of 0.1 mV/s or less. In some embodiments, the predetermined threshold is a slope of 0.05 mV/s or less. In some embodiments, the predetermined threshold is a slope of 0.025 mV/s or less.

[0051] In each case, the slopes shown as S1, S2, and S3 exceeded the predetermined threshold. For example, in some embodiments, the predetermined threshold is a slope of 0.1 mV/s units or less. In each shown bath, the slopes shown as S1, S2, and S3 are all about 3 mV/s

[0052] Because none of the baths with indications of an upcoming failure event were remedied in FIG. 3B, in each case, the bath failed, resulting in underfilling or voids in the TSV features, as explained herein.

[0053] When other conditions are similar, smaller TSV features fill faster than larger TSV features. The number of wafers that may be plated before a predicted bath failure may be influenced by the plating time for each wafer, which is determined at least in part by feature size. Therefore, cumulative plating time may be identified as a key factor in predicting bath failure, as opposed to the number of wafers plated.

[0054] FIGs. 4A-4C are graphs of voltages for baths with an increased age, in accordance with the present technology. As used herein, the voltages referred to are measurements from the anodes inside the bath, as explained in FIGs. 1A-2. The age of the bath may directly correlate with an increased possibility of an upcoming failure event of the bath. On the horizontal axis of both FIGs. 3A-3B is time in seconds. On the vertical axis is voltage (V_f (V vs. Ref.)). Each line on the graph represents a tested bath. The curved arrow shown in the bottom left corner of FIGs. 3A-3B represents increasing bath age.

[0055] FIG. 4A is a graph of voltages from multiple baths shown as traces. Plotted are three examples of bath failure (thin dashed line, thick dashed line, dotted line) and multiple examples of baths that did not fail (solid lines). While baths that did fail and baths that did not fail had similar slopes at first times d1, d2, when the bath represented by the thick dashed line failed, an inflection point at second time D1 was present, and a slope of the monitored voltage S1 exceeded a predetermined voltage slope threshold. In contrast, the slope ES of the non-failing bath remained below the predetermined voltage threshold. As shown in FIG. 4A, as the age of the bath increased, it was more likely for the bath to fail. As none of the failing baths were remedied after detecting the upcoming failure event of the bath, the baths eventually failed, resulting in underfilling of the TSV feature as shown in the center insert in FIG. 4A. In contrast, the baths that did not fail continued to perform by resulting in the properly filled TSV features, as shown in the right side insert of FIG. 4A. The legend of the proper/improper TSV fill features is shown in FIG. 3A above.

[0056] FIG. 4B is another graph of increasing bath age, showing two baths that failed (dotted line, dashed line), and three baths that did not fail (thin solid line, thick solid line, dot-dashed line). In each case of the failing baths, while the initial slopes of the lines at first time d1 and d2 were under the predetermined threshold for the voltage slope, eventually the voltage spiked, resulting in a slope greater than the predetermined slope thresholds S1 and S2, respectively. Further, both failing baths also exhibit inflection points at second times D1, D2. As shown in the right side insert of FIG. 4B, when the bath represented by the dotted line failed, multiple TSV features were underfilled. In contrast, the non-failing bath represented by the thin solid line maintained a slope under the predetermined threshold at second time d3. The slope ES of the thin solid line was also under the predetermined threshold, therefore also resulting in properly filled TSVs.

[0057] FIG. 4C is another graph of baths having increasing bath age. Only one bath failed, represented by the solid black line. As shown, at first, the voltage of each of the baths had a slope shown at times d1, d2 and d3, respectively, below a predetermined threshold. However, as time progressed, the voltage of the bath represented by the solid black line jumps, and the slope S1 becomes greater than the predetermined voltage slope threshold. This bath failure correlates with the underfill of the one or more TSV features, as shown in the insert on the right side of the graph. Further, an inflection point D1 is also present. In contrast, the baths that did not fail maintained a slope ES below the predetermined threshold.

[0058] FIG. 5 is a graph of voltages for multiple remedied baths, in accordance with the present technology. In some embodiments, when an upcoming failure event is declared by the system, the system may remedy the bath prior to bath failure. In such cases, electroplating can continue at a high standard of quality, without causing underfilling or voids in TSV features. In such cases, when the bath is remedied, bath age does not affect the quality of the bath.

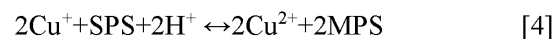
[0059] On the horizontal axis is time in seconds. On the vertical axis is voltage (V_f (V vs Ref)). As shown, when the bath is remedied, no voltage spikes (i.e., voltage having a slope greater than a predetermined threshold) or inflection points are shown. Baths may be remedied in multiple ways, as explained herein.

[0060] In some embodiments, the method disclosed herein includes remedying the bath before the upcoming failure event. In some embodiments, remedying the bath includes replacing the bath.

[0061] Instability of the bath correlates with formation of MPSA, a strong accelerator, during reductive plating. This results in poor bottom-up fill, poor suppression in the field and in the trenches. In some embodiments, remedying the bath includes controlling formation of 3-mercaptopropanesulfonic acid (MPSA). It may be difficult to maintain a constant concentration of MPSA throughout the plating process. However, MPSA may be mitigated in several ways.

[0062] MPSA can be minimized with bleed and feed (30%), where the bath is constantly being refreshed. This removes MPSA from the bath continuously, so that the MPSA concentration remains generally stable.

[0063] By reducing sulfuric acid concentration, H^+ ion availability is reduced. This may affect the SPS breakdown rate. By reducing both the H^+ availability and the SPS, the equilibrium concentration of MPSA is effectively reduced via the chemical reaction:



[0064] In some embodiments, controlling formation of MPSA includes reducing the MPSA in the bath to a concentration of less than about 1.0 ppm. In some embodiments, controlling formation of MPSA includes reducing the MPSA in the bath to a concentration of less than about 5.0 ppm. In some embodiments, controlling formation of MPSA includes reducing the MPSA in the bath to a concentration of less than about 10 ppm.

[0065] MPSA may also be controlled by idle time recovery. By allowing the bath to sit idle, MPSA will oxidize or convert back to SPS. In some embodiments, remedying

the bath includes stopping the electroplating until a predetermined time has elapsed. In some embodiments, the predetermined time is between about 8 to about 30 hours.

[0066] Purging the bath also removes MPSA. This may be performed by bubbling clean dry air up through the bath. Deplating or running the plating process with reverse
5 polarity also removes MPSA.

[0067] In some embodiments, delaying or avoiding bath failure resulting from MPSA may be achieved with current pulsing. In standard plating processes current is continuous. This results in continuous formation of MPSA or Cu(I) thiolate, a complexing group, by combining Cu(I) ions with MPSA thiolate group. This causes the bath to become
10 highly accelerator-dominated over time, resulting in under fill due to decreased suppression on the fields.

[0068] By pulsing the current during the plating process, using short pulses or long pulses, formation of MPSA is controlled. The pulsing may be negative, that is, current may be pulsed to a negative current from a positive or plating current, or the pulsing may
15 be positive, that is pulsing of positive plating current or going to an open circuit potential. Cross-over pulsing may also be used via pulsing with constant current and constant voltage. The pulsing may be done at regular intervals in a POR process. This may help to maintain bath stability by knocking MPSA off of the copper surface and increasing bath suppression. Pulsing may also be performed with no wafer present. Current density ramping may also
20 be used to reduce the effect of MPSA and restore bath stability.

[0069] FIG. 6 is an example method 600 for controlling quality of a bath, in accordance with the present technology. In some embodiments, the method 600 may be carried out with a processor (such as processor 20). In some embodiments, the processor includes a controller (such as controller 50) and one or more anodes (such as one or more
25 anodes 28). Upon detection of an abrupt change in voltage, the controller determines that an upcoming failure event of the bath may have occurred. The controller may then sound an alert or alarm, and optionally shut down the processor. In some embodiments, this function may be added to the processor via software used in programming the controller. In other embodiments, the method 600 may be carried out with an auxiliary tool (such as
30 auxiliary tool 100), a computing device (such as computing device 90) and one or more electrodes (such as electrodes 27) of the auxiliary tool.

[0070] In block 605, a wafer (such as wafer 40) is placed into contact with a bath. In some embodiments, the bath includes an accelerator, a leveler, and a suppressor. In

some embodiments, one or more anodes are located in the bath. In some embodiments, block 605 may be skipped, such as when the auxiliary tool is utilized to determine bath health independent of the wafer.

5 [0071] In block 610, an electrical current is passed from the one or more anodes (or the one or more electrodes of the auxiliary tool) through the bath and through a conductive layer on the wafer (if present). In some embodiments, the wafer includes one or more TSV features.

10 [0072] In block 615, the voltage of the one or more anodes (or one or more electrodes) is monitored. In some embodiments, this is done with the controller of the processor. In some embodiments, this is done with one or more computer processors. In other embodiments, this is done with the computing device of the auxiliary tool.

15 [0073] In block 620, an upcoming failure event of the bath based on an inflection point in the monitored voltage is declared. In some embodiments, the inflection point determines that the bath is about to fail (i.e., the bath is close in time to a point where TSVs will start having failures).

[0074] Optionally, in block 625, the bath may be remedied before the failure occurs. In some embodiments, remedying the bath includes replacing the bath, stopping the electroplating process until the bath has a concentration of MPSA of 10 ppm or lower, or applying current to the bath as disclosed herein.

20 [0075] FIG. 7 is another example method 700 for controlling quality of a bath, in accordance with the present technology. In some embodiments, the method 700 may be carried out with a processor (such as processor 20). In some embodiments, the processor includes a controller (such as controller 50) and one or more anodes (such as one or more anodes 28). Upon detection of an abrupt change in voltage, the controller determines that
25 an upcoming failure event of the bath may have occurred. The controller may then sound an alert or alarm, and optionally shut down. In some embodiments, this function may be added to the processor via software used in programming the controller. In other embodiments, the method 600 may be carried out with an auxiliary tool (such as auxiliary tool 100), a computing device (such as computing device 90) and one or more electrodes
30 (such as electrodes 27) of the auxiliary tool.

[0076] In block 705, a wafer (such as wafer 40) is placed into contact with a bath. In some embodiments, the bath includes an accelerator, and a leveler and/or suppressor. In some embodiments, one or more anodes are located in the bath. In some embodiments,

block 605 may be skipped, such as when the auxiliary tool is utilized to determine bath health independent of the wafer.

[0077] In block 710, an electrical current is passed from the one or more anodes (or the one or more electrodes of the auxiliary tool) through the bath and through a
5 conductive layer on the wafer (if present). In some embodiments, the wafer includes one or more TSV features.

[0078] In block 715, the voltage of the one or more anodes (or the one or more electrodes of the auxiliary tool) is monitored. In some embodiments, this is done with the controller of the processor. In some embodiments, this is done with one or more computer
10 processors. In other embodiments, this is done with the computing device of the auxiliary tool.

[0079] In block 720, an upcoming failure event of the bath based on the voltage exceeding a predetermined threshold. In some embodiments, the predetermined threshold is based on a slope of change in the voltage. In some embodiments, the upcoming failure
15 event of the bath occurs when the slope of the change in voltage is greater than the predetermined threshold. In some embodiments, the predetermined threshold is a slope of about 0.1 mV/s or less.

[0080] Optionally, in block 725, the bath may be remedied before the failure occurs. In some embodiments, remedying the bath includes replacing the bath, stopping
20 the electroplating process until the bath has a concentration of MPSA of 10 ppm or lower, or applying current to the bath as disclosed herein.

[0081] It should be understood that methods 600 and 700 should be interpreted as merely representative. In some embodiments, process blocks of methods 600 and 700 may be performed simultaneously, sequentially, in a different order, or even be omitted,
25 without departing from the scope of this disclosure.

[0082] The present application may reference quantities and numbers. Unless specifically stated, such quantities and numbers are not to be considered restrictive, but representative of the possible quantities or numbers associated with the present application. Also, in this regard, the present application may use the term “plurality” to reference a
30 quantity or number. In this regard, the term “plurality” is meant to be any number that is more than one, for example, two, three, four, five, etc. The terms “about,” “approximately,” “near,” etc., mean plus or minus 5% of the stated value. For the purposes of the present disclosure, the phrase “at least one of A, B, and C,” for example, means (A), (B), (C), (A

and B), (A and C), (B and C), or (A, B, and C), including all further possible permutations when greater than three elements are listed.

[0083] Embodiments disclosed herein may utilize circuitry in order to implement technologies and methodologies described herein, operatively connect two or more components, generate information, determine operation conditions, control an appliance, device, or method, and/or the like. Circuitry of any type can be used. In an embodiment, circuitry includes, among other things, one or more computing devices such as a processor (e.g., a microprocessor), a central processing unit (CPU), a digital signal processor (DSP), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), or the like, or any combinations thereof, and can include discrete digital or analog circuit elements or electronics, or combinations thereof.

[0084] An embodiment includes one or more data stores that, for example, store instructions or data. Non-limiting examples of one or more data stores include volatile memory (e.g., Random Access memory (RAM), Dynamic Random Access memory (DRAM), or the like), non-volatile memory (e.g., Read-Only memory (ROM), Electrically Erasable Programmable Read-Only memory (EEPROM), Compact Disc Read-Only memory (CD-ROM), or the like), persistent memory, or the like. Further non-limiting examples of one or more data stores include Erasable Programmable Read-Only memory (EPROM), flash memory, or the like. The one or more data stores can be connected to, for example, one or more computing devices by one or more instructions, data, or power buses.

[0085] In an embodiment, circuitry includes a computer-readable media drive or memory slot configured to accept signal-bearing medium (e.g., computer-readable memory media, computer-readable recording media, or the like). In an embodiment, a program for causing a system to execute any of the disclosed methods can be stored on, for example, a computer-readable recording medium (CRMM), a signal-bearing medium, or the like. Non-limiting examples of signal-bearing media include a recordable type medium such as any form of flash memory, magnetic tape, floppy disk, a hard disk drive, a Compact Disc (CD), a Digital Video Disk (DVD), Blu-Ray Disc, a digital tape, a computer memory, or the like, as well as transmission type medium such as a digital and/or an analog communication medium (e.g., a fiber optic cable, a waveguide, a wired communications link, a wireless communication link (e.g., transmitter, receiver, transceiver, transmission logic, reception logic, etc.). Further non-limiting examples of signal-bearing media include, but are not limited to, DVD-ROM, DVD-RAM, DVD+RW, DVD-RW, DVD-R, DVD+R, CD-ROM,

Super Audio CD, CD-R, CD+R, CD+RW, CD-RW, Video Compact Discs, Super Video Discs, flash memory, magnetic tape, magneto-optic disk, MINIDISC, non-volatile memory card, EEPROM, optical disk, optical storage, RAM, ROM, system memory, web server, or the like.

5 **[0086]** The detailed description set forth above in connection with the appended drawings, where like numerals reference like elements, are intended as a description of various embodiments of the present disclosure and are not intended to represent the only embodiments. Each embodiment described in this disclosure is provided merely as an example or illustration and should not be construed as preferred or advantageous over other
10 embodiments. The illustrative examples provided herein are not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. Similarly, any steps described herein may be interchangeable with other steps, or combinations of steps, in order to achieve the same or substantially similar result. Generally, the embodiments disclosed herein are non-limiting, and the inventors contemplate that other embodiments within the
15 scope of this disclosure may include structures and functionalities from more than one specific embodiment shown in the figures and described in the specification.

[0087] In the foregoing description, specific details are set forth to provide a thorough understanding of exemplary embodiments of the present disclosure. It will be apparent to one skilled in the art, however, that the embodiments disclosed herein may be
20 practiced without embodying all the specific details. In some instances, well-known process steps have not been described in detail in order not to unnecessarily obscure various aspects of the present disclosure. Further, it will be appreciated that embodiments of the present disclosure may employ any combination of features described herein.

[0088] The present application may include references to directions, such as
25 “vertical,” “horizontal,” “front,” “rear,” “left,” “right,” “top,” and “bottom,” etc. These references, and other similar references in the present application, are intended to assist in helping describe and understand the particular embodiment (such as when the embodiment is positioned for use) and are not intended to limit the present disclosure to these directions or locations.

30 **[0089]** The present application may also reference quantities and numbers. Unless specifically stated, such quantities and numbers are not to be considered restrictive, but exemplary of the possible quantities or numbers associated with the present application. Also, in this regard, the present application may use the term “plurality” to reference a

quantity or number. In this regard, the term “plurality” is meant to be any number that is more than one, for example, two, three, four, five, etc. The term “about,” “approximately,” etc., means plus or minus 5% of the stated value. The term “based upon” means “based at least partially upon.”

5 **[0090]** The principles, representative embodiments, and modes of operation of the present disclosure have been described in the foregoing description. However, aspects of the present disclosure, which are intended to be protected, are not to be construed as limited to the particular embodiments disclosed. Further, the embodiments described herein are to be regarded as illustrative rather than restrictive. It will be appreciated that
10 variations and changes may be made by others, and equivalents employed, without departing from the spirit of the present disclosure. Accordingly, it is expressly intended that all such variations, changes, and equivalents fall within the spirit and scope of the present disclosure as claimed.

[0091] While illustrative embodiments have been illustrated and described, it will
15 be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

CLAIMS

We claim:

1. A method of controlling quality of electroplating a wafer having one or more through silicon via (TSV) features, the method comprising:
 - placing a wafer in contact with a bath, wherein the bath comprises an accelerator and a leveler, a suppressor, or a combination thereof;
 - passing electrical current from one or more anodes through the bath and through a conductive layer on the wafer;
 - monitoring a voltage of the one or more anodes by one or more controllers; and
 - declaring an upcoming failure event of the bath based on a predetermined threshold of voltage by the one or more controllers.
2. The method of Claim 1, wherein the upcoming failure event is determined by detecting an inflection point in the voltage.
3. The method of Claim 1, wherein the predetermined threshold is based on a slope of the voltage.
4. The method of Claim 3, wherein the upcoming failure event occurs when the slope of the voltage is greater than the predetermined threshold.
5. The method of Claim 3, wherein the predetermined threshold is a slope of about 0.1 mV/s or less.
6. The method of Claim 1, further comprising:
 - remedying the bath before the upcoming failure event takes place.
7. The method of Claim 6, wherein remedying the bath comprises replacing the bath.
8. The method of Claim 6, wherein remedying the bath comprises controlling formation of 3-mercaptopropanesulfonic acid (MPSA).
9. The method of Claim 8, wherein controlling formation of MPSA comprises reducing the MPSA in the bath to a concentration of less than about 1.0 ppm

10. The method of Claim 6, wherein remedying the bath comprises stopping the electroplating until a predetermined time has elapsed.

11. The method of Claim 10, wherein the predetermined time is between about 8 to about 30 hours.

12. The method of Claim 1, wherein the upcoming failure event of the bath occurs when a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA).

13. The method of Claim 1, wherein the upcoming failure event of the bath occurs when a drop or an oscillation of the voltage is detected.

14. The method of Claim 1, wherein the upcoming failure event of the bath occurs when one or more voids are formed in the one or more TSV features, one or more TSV features is underfilled, or a combination thereof.

15. A method of electroplating a wafer with one or more through silicon via (TSV) features, the method comprising:
passing electrical current from one or more electrodes through a bath;
monitoring a voltage of the one or more anodes; and
declaring an upcoming failure event of the bath based on an inflection point in the voltage by one or more controllers.

16. The method of Claim 15, wherein the upcoming failure event of the bath occurs when the bath has a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA).

17. The method of Claim 15, wherein the upcoming failure event of the bath occurs when one or more voids in the one or more TSV features are formed, one or more TSV features are underfilled, or a combination thereof.

18. A method of electroplating a wafer with one or more through silicon via (TSV) features, the method comprising:
passing electrical current from one or more electrodes through a bath;
monitoring a voltage of the one or more anodes; and

declaring an upcoming failure event of the bath based on a slope of the voltage being greater than a predetermined threshold.

19. The method of Claim 18, wherein the slope is about 0.1 mV/s or less.

20. The method of Claim 18, wherein the upcoming failure event of the bath occurs when the bath has a concentration of greater than about 10 ppm of 3-mercaptopropanesulfonic acid (MPSA).