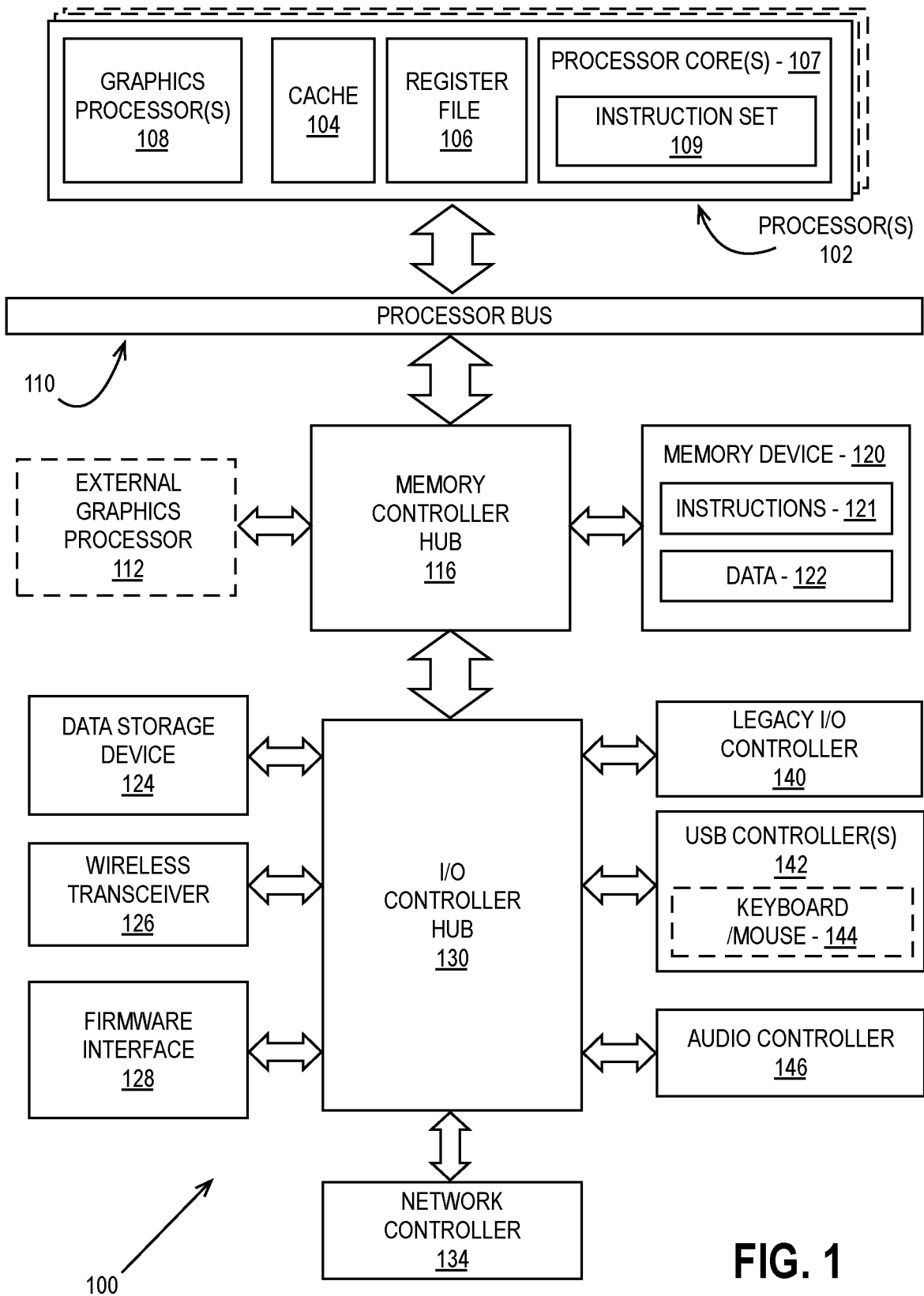


**FIG. 1**

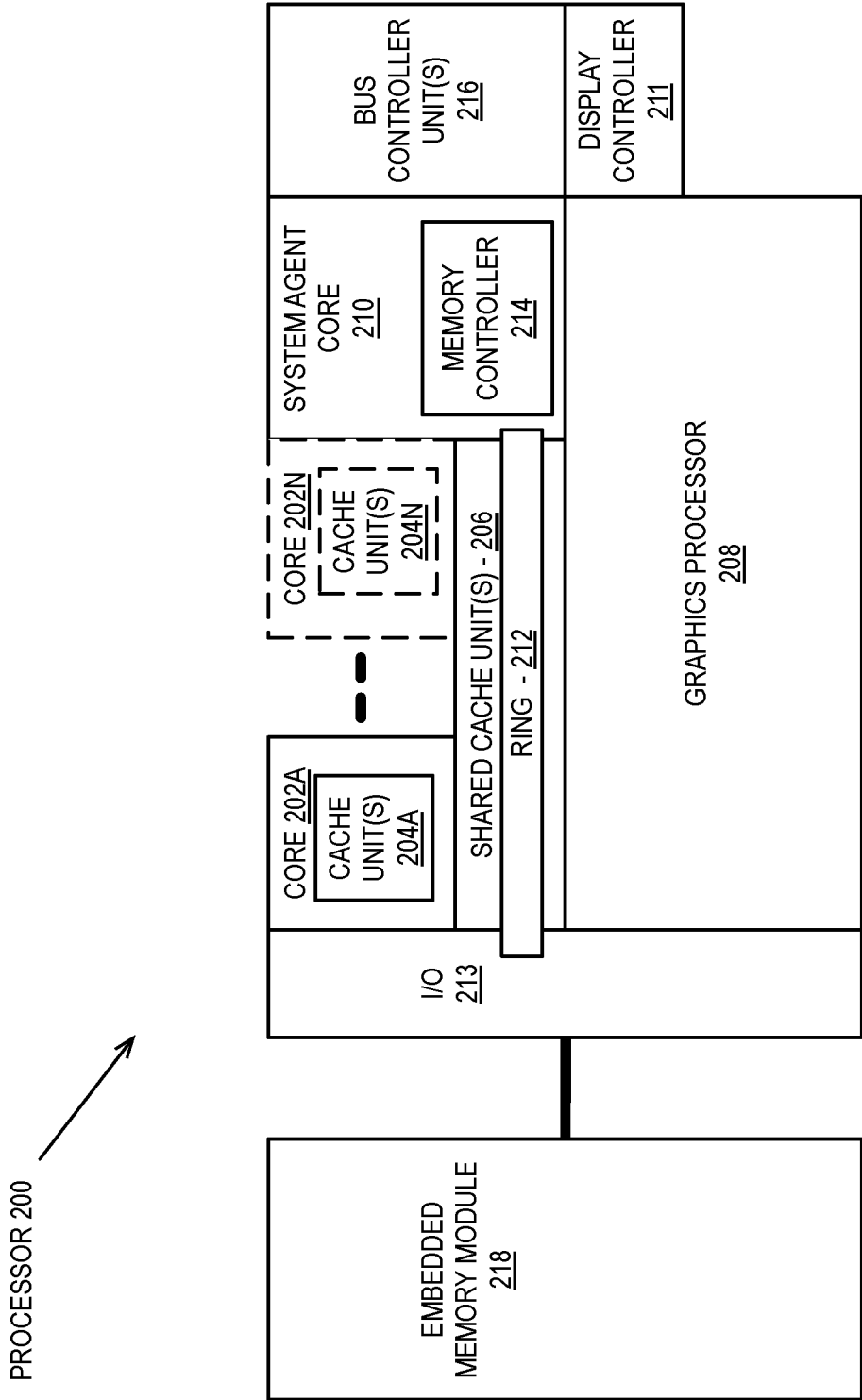


FIG. 2

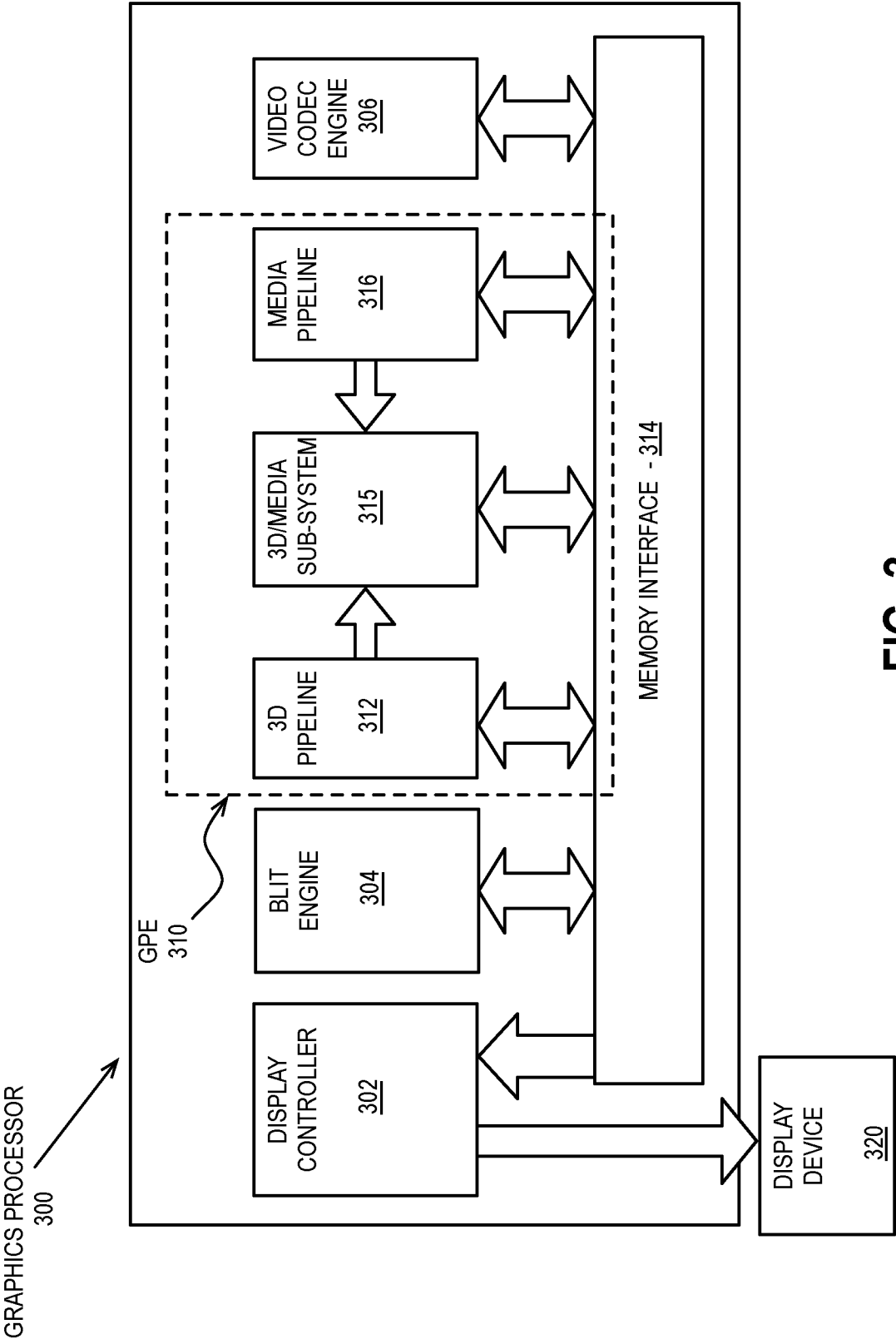


FIG. 3

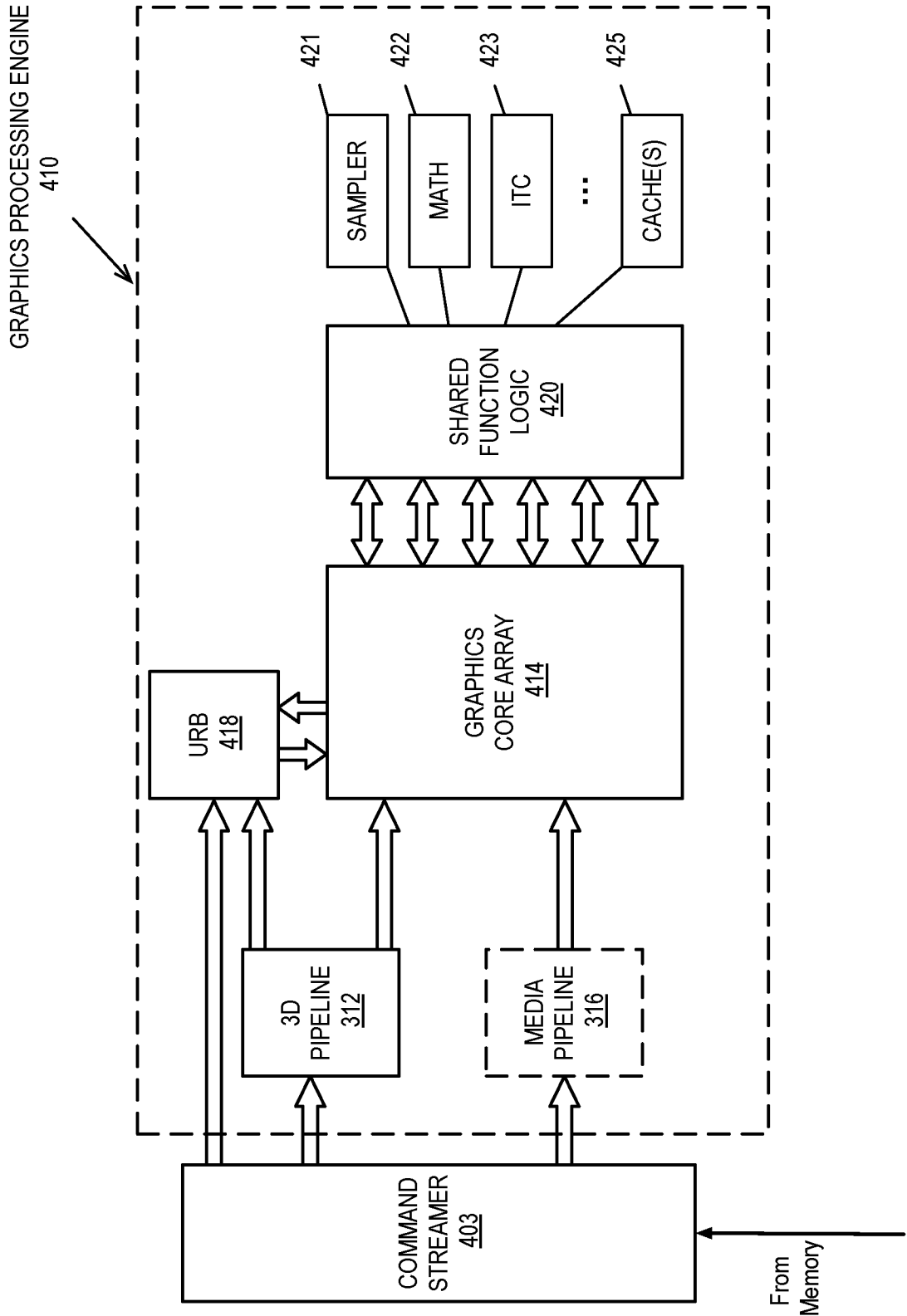


FIG. 4

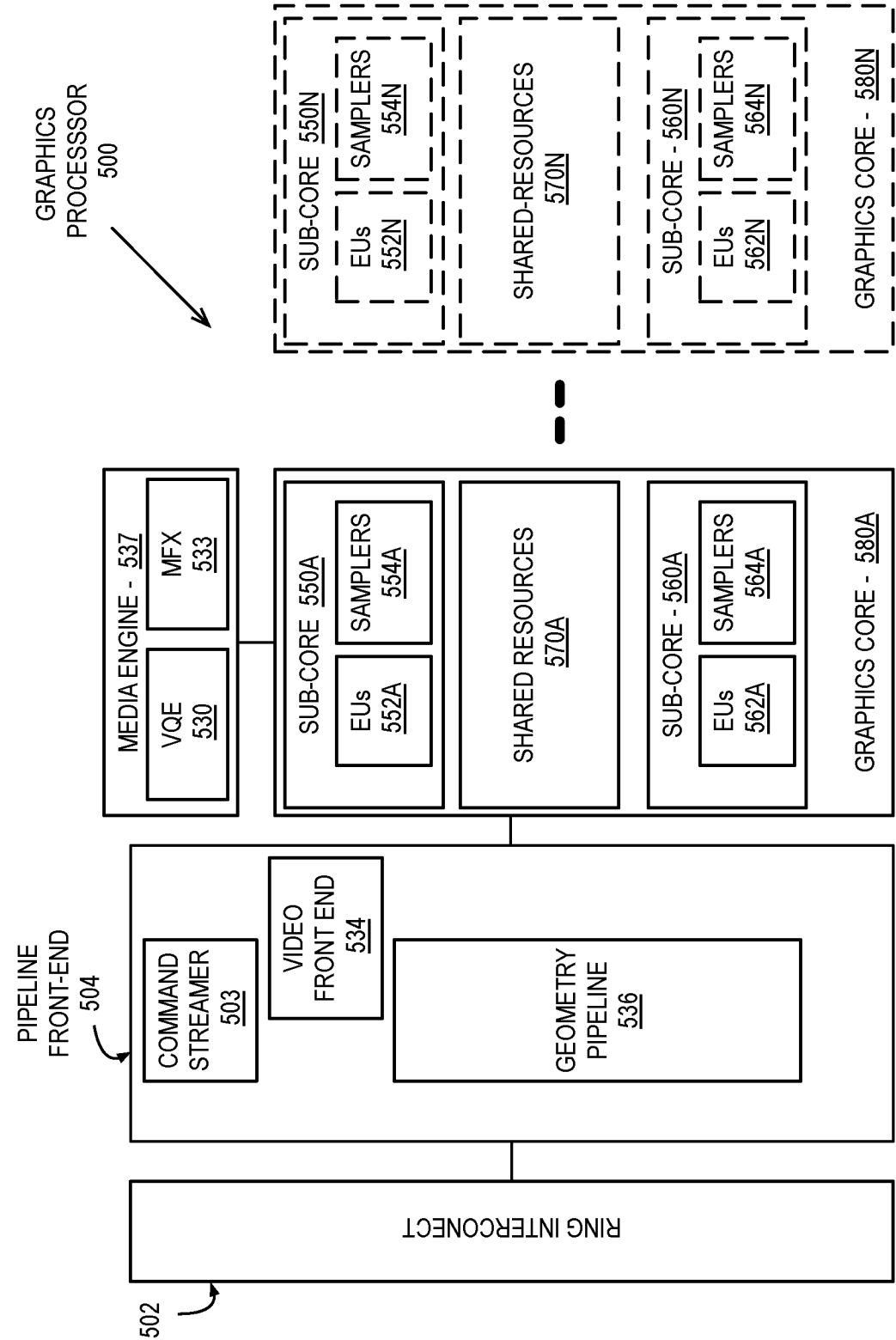


FIG. 5

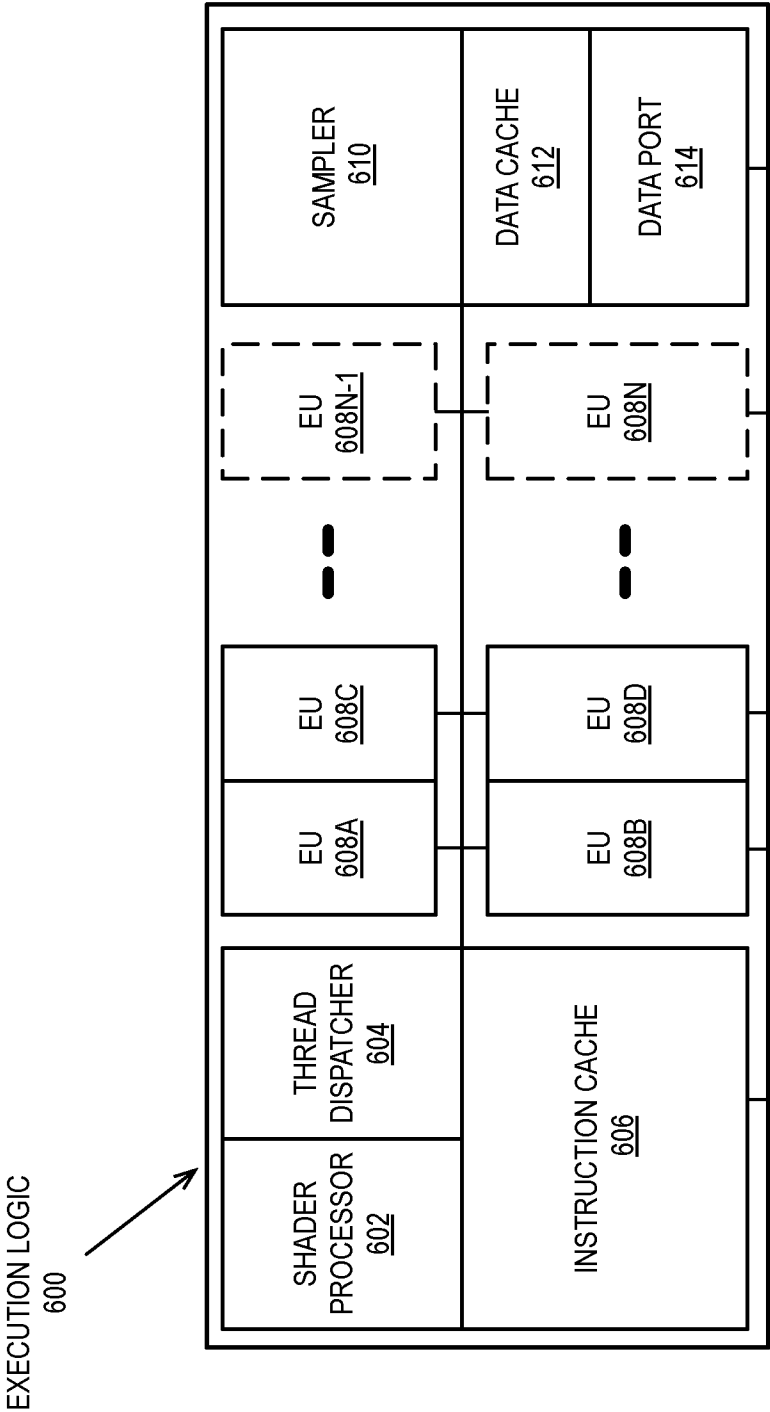


FIG. 6

GRAPHICS PROCESSOR INSTRUCTION FORMATS

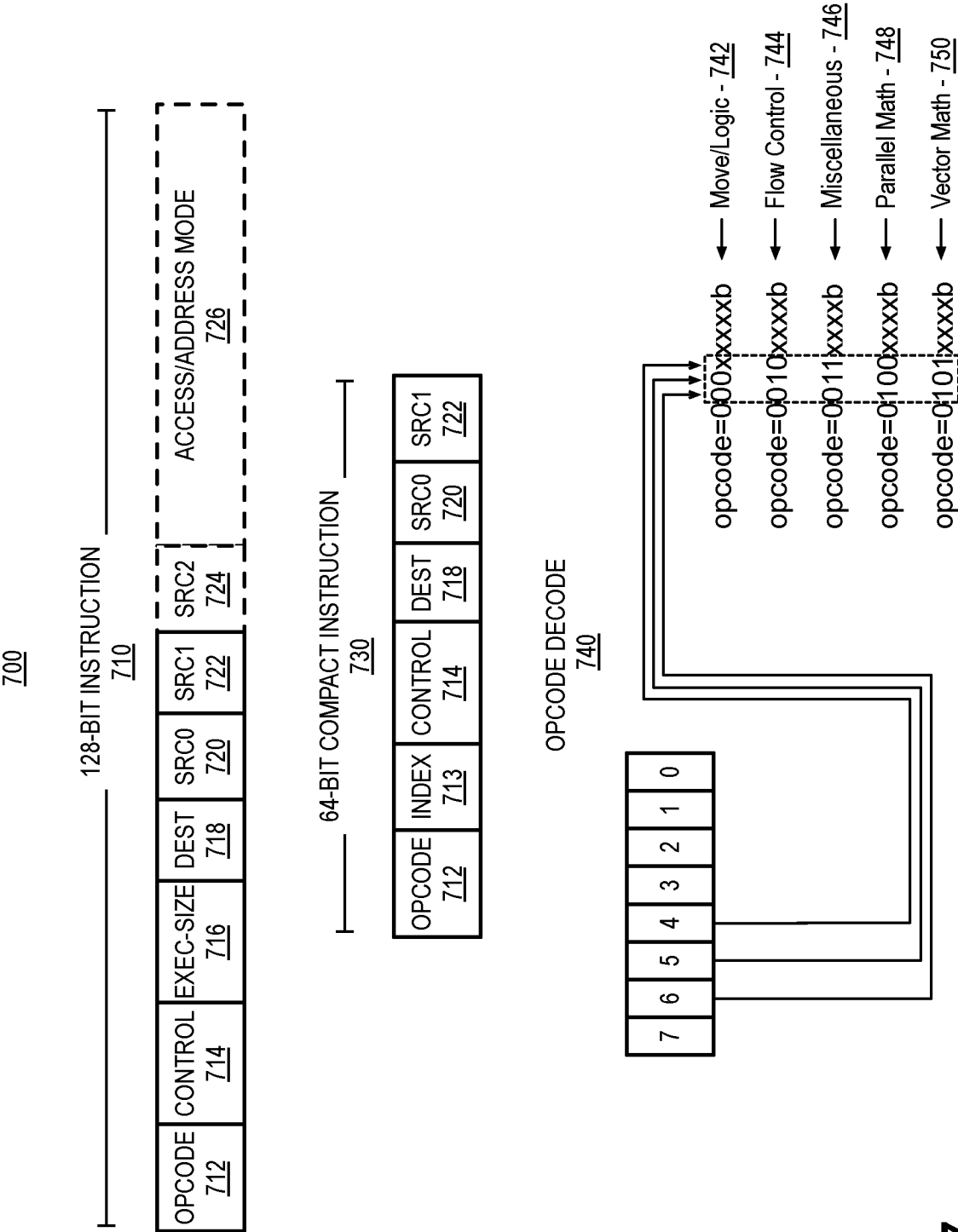


FIG. 7

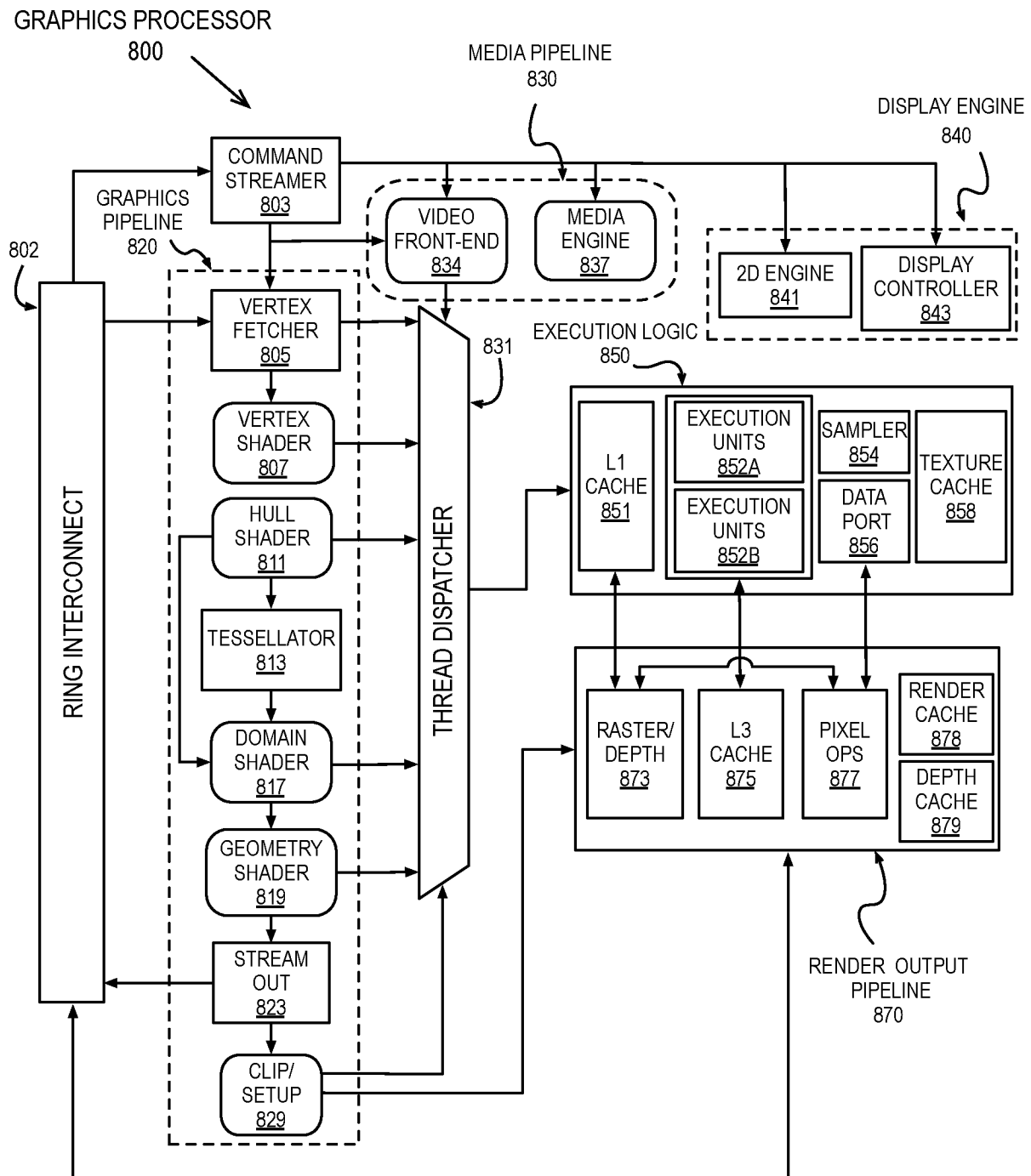


FIG. 8

FIG. 9A **GRAPHICS PROCESSOR COMMAND FORMAT**
900

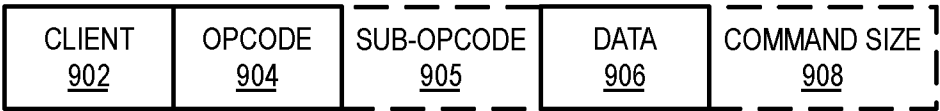
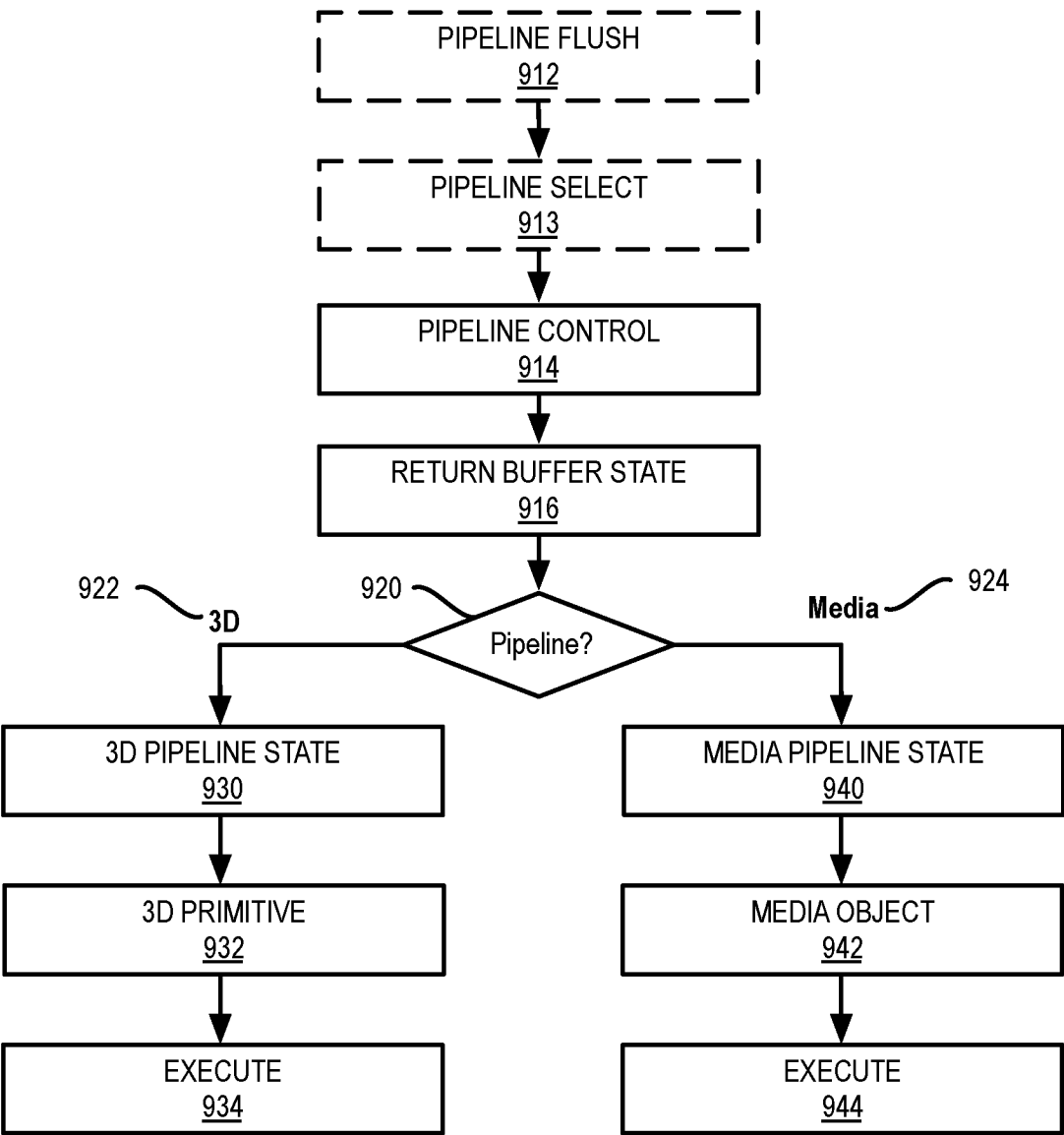


FIG. 9B **GRAPHICS PROCESSOR COMMAND SEQUENCE**
910



DATA PROCESSING SYSTEM -1000

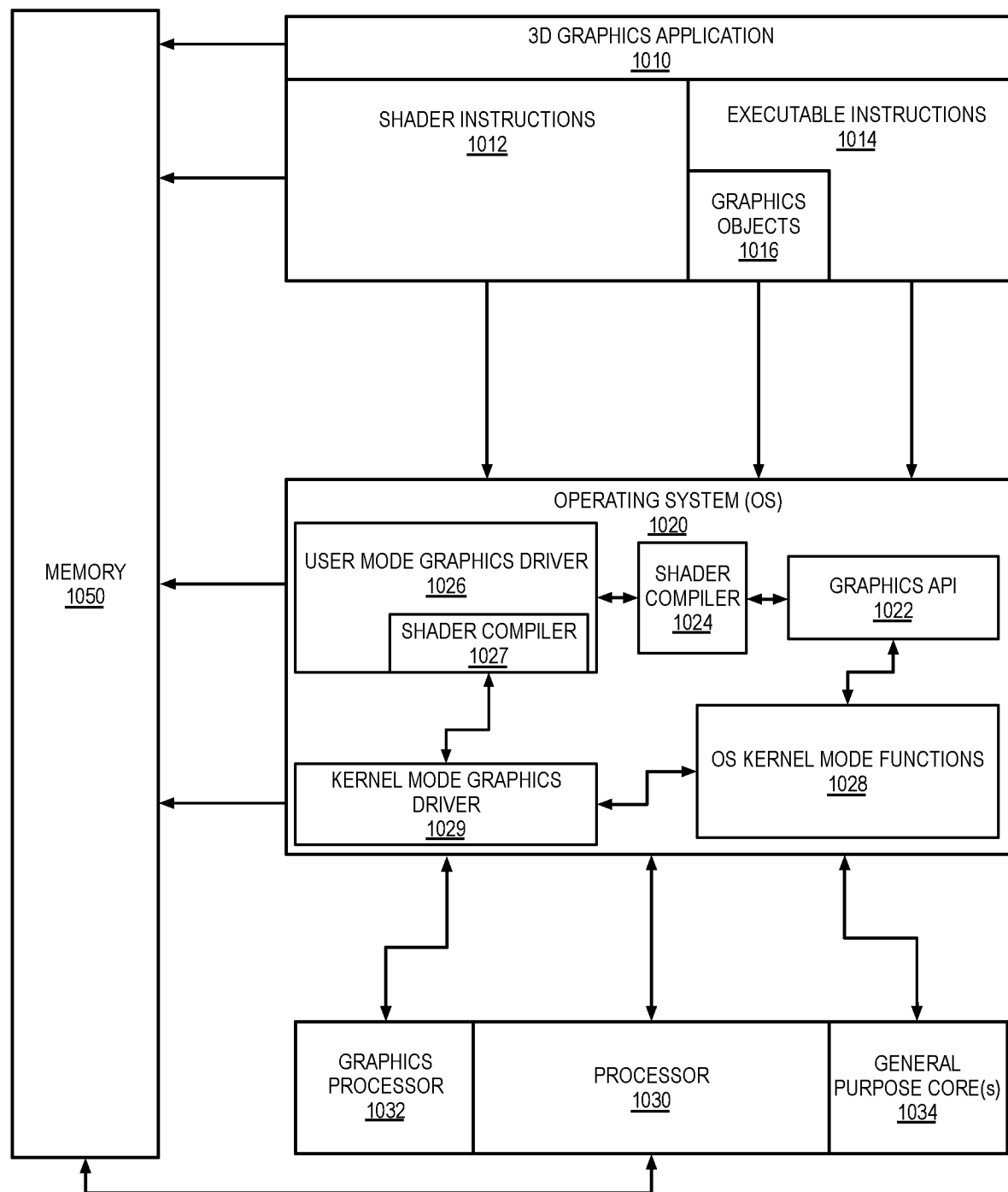


FIG. 10

IP CORE DEVELOPMENT - 1100

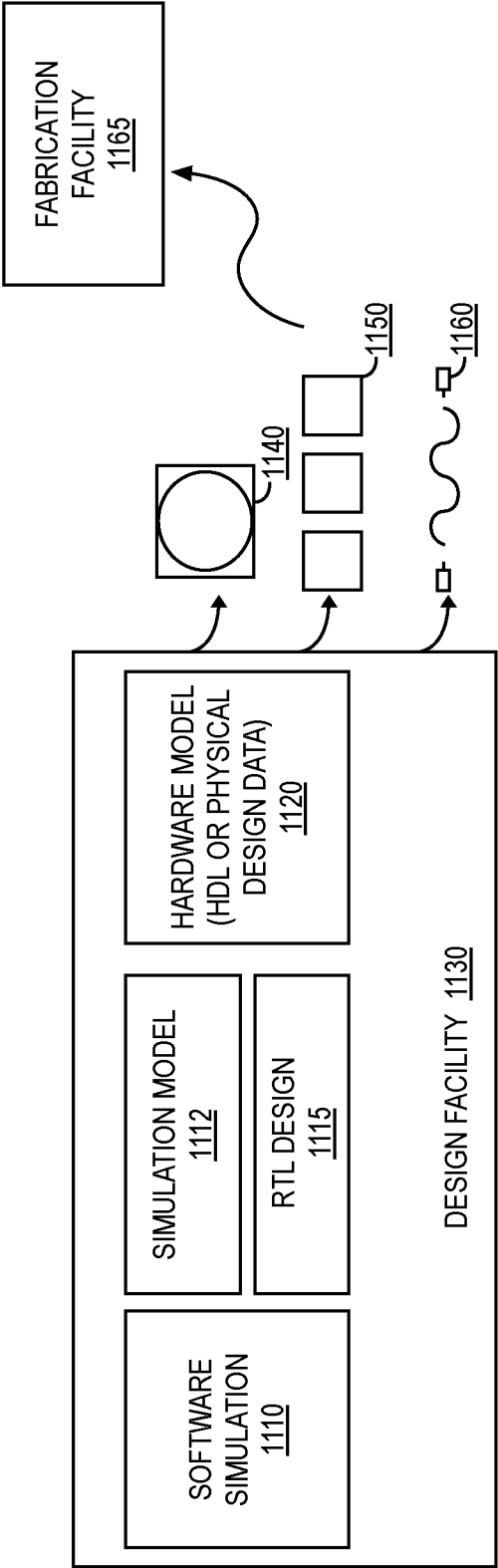
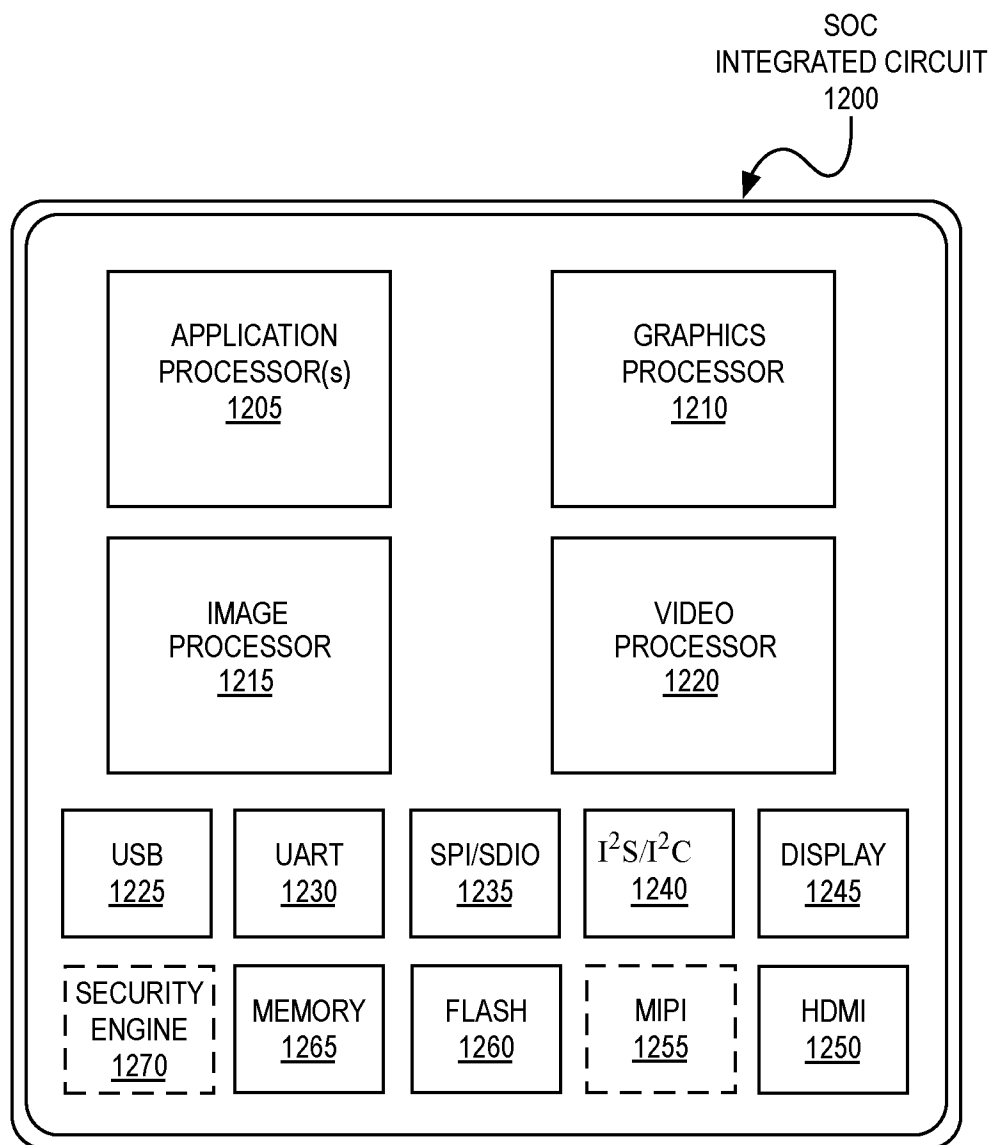
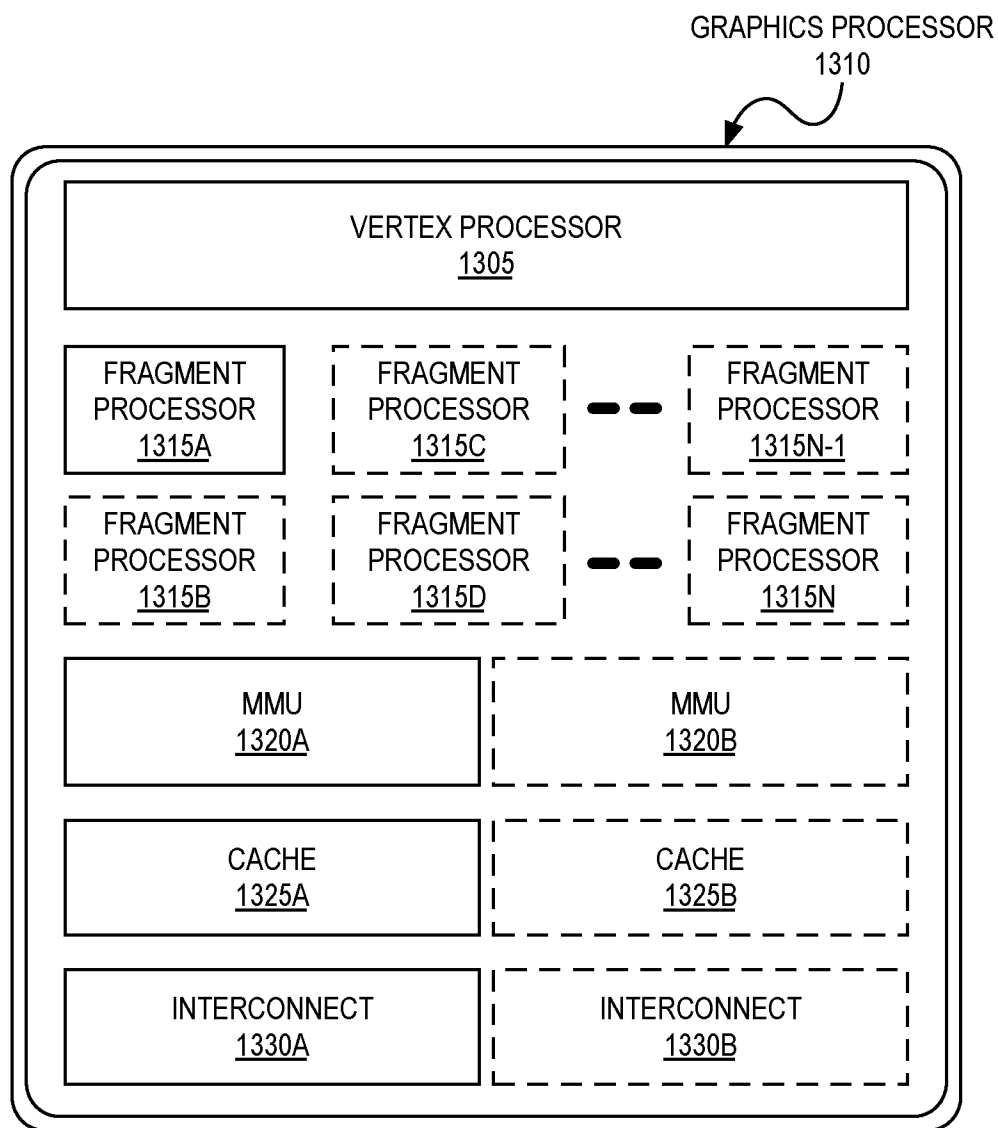


FIG. 11

**FIG. 12**

**FIG. 13**

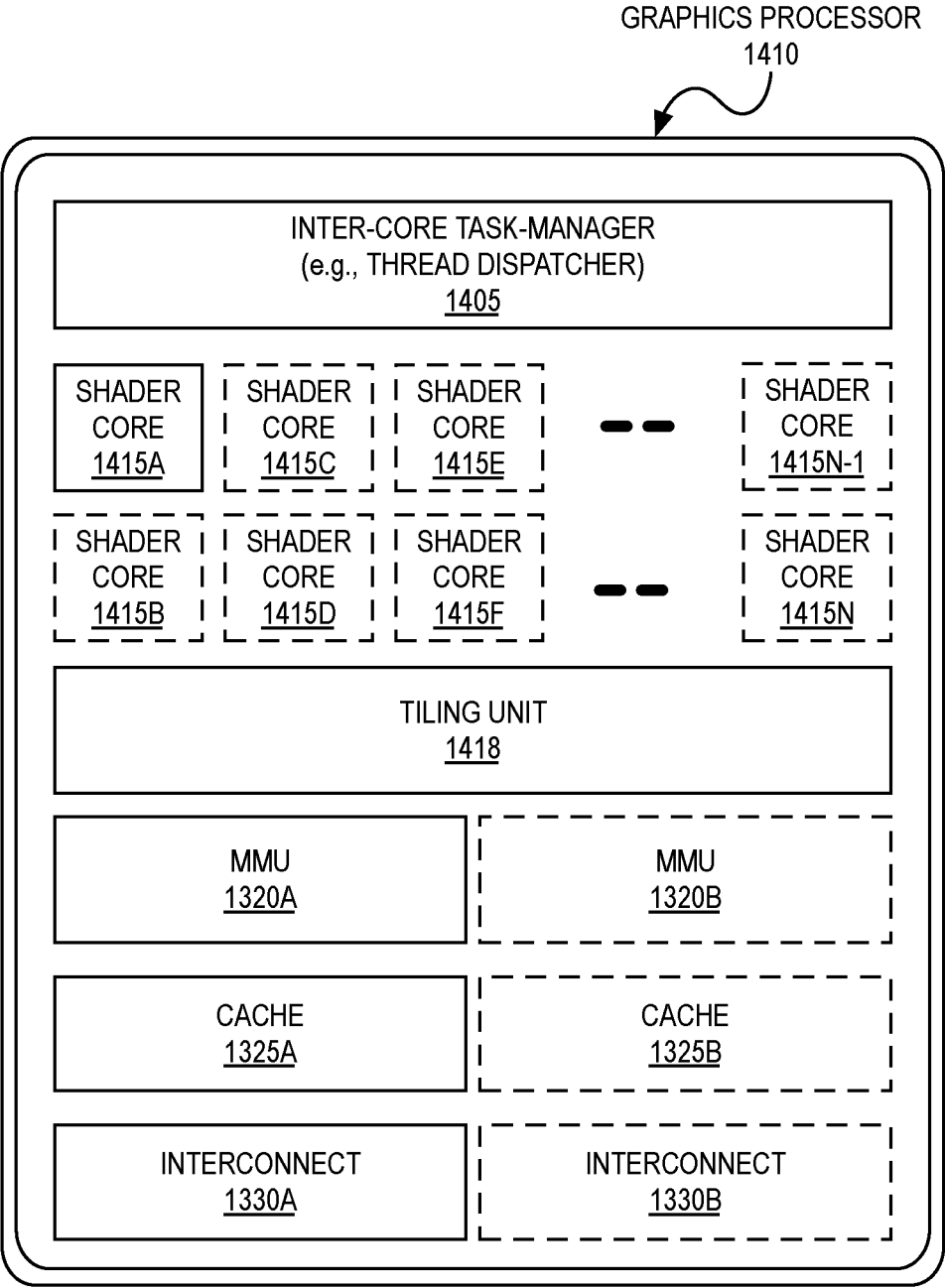
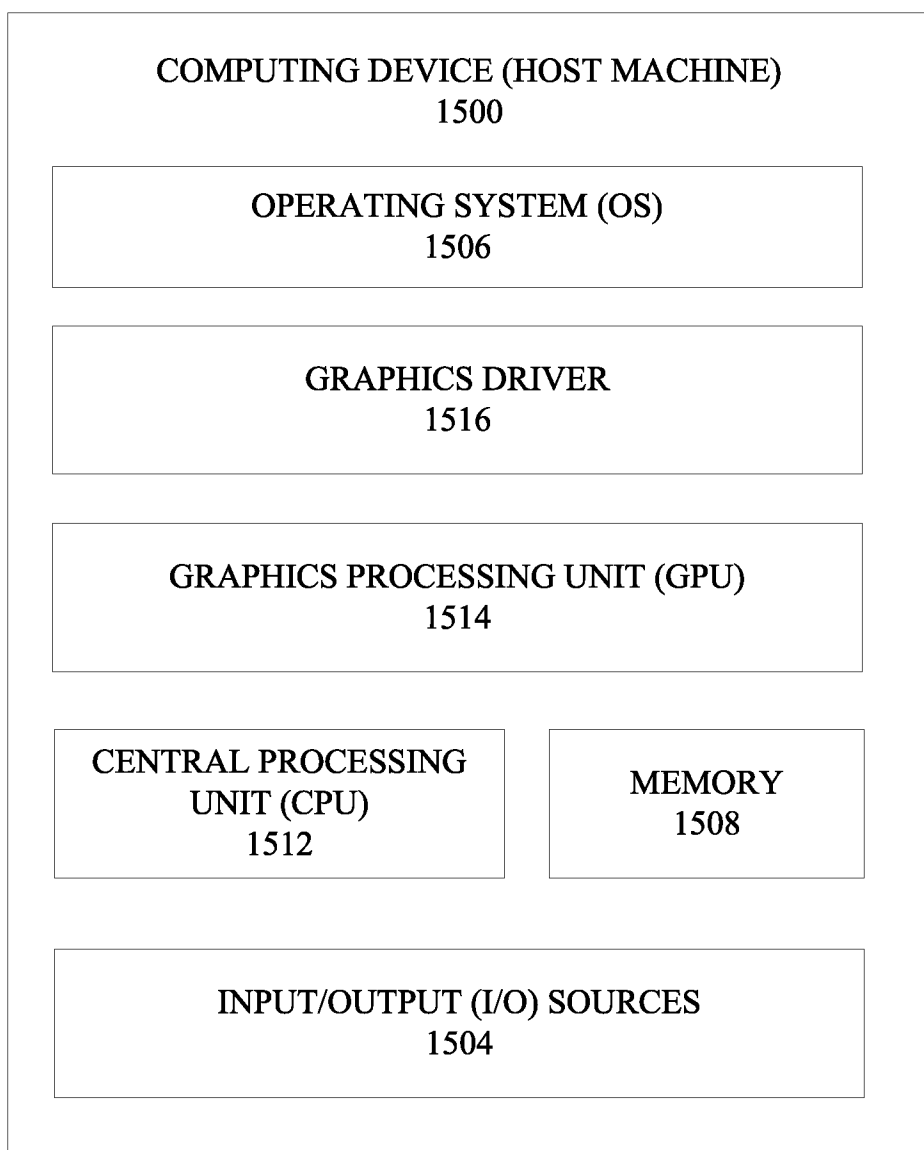
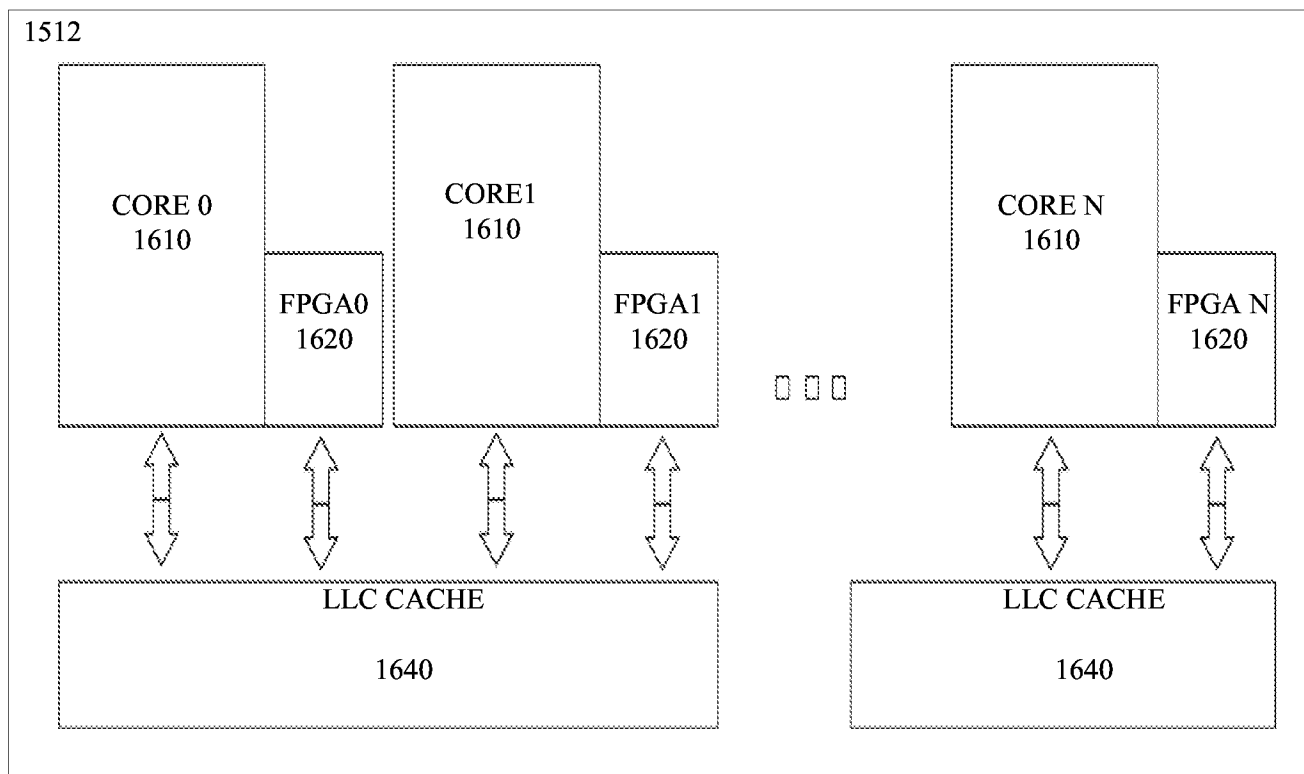
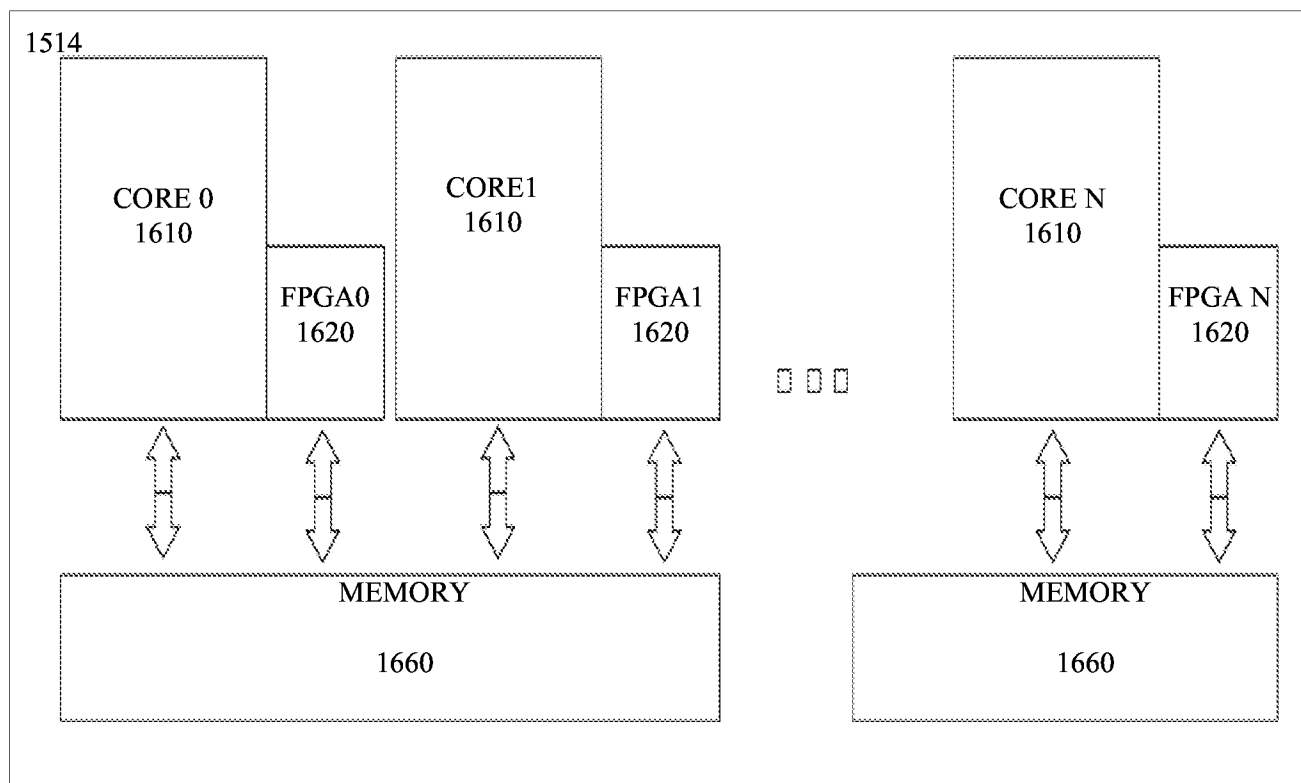
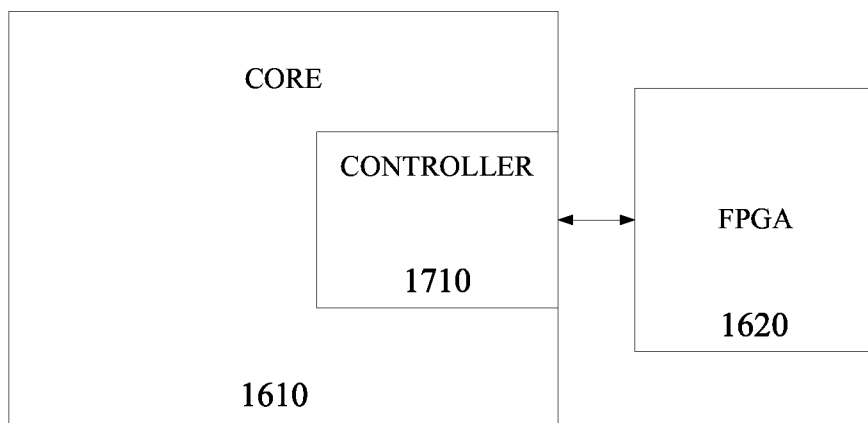
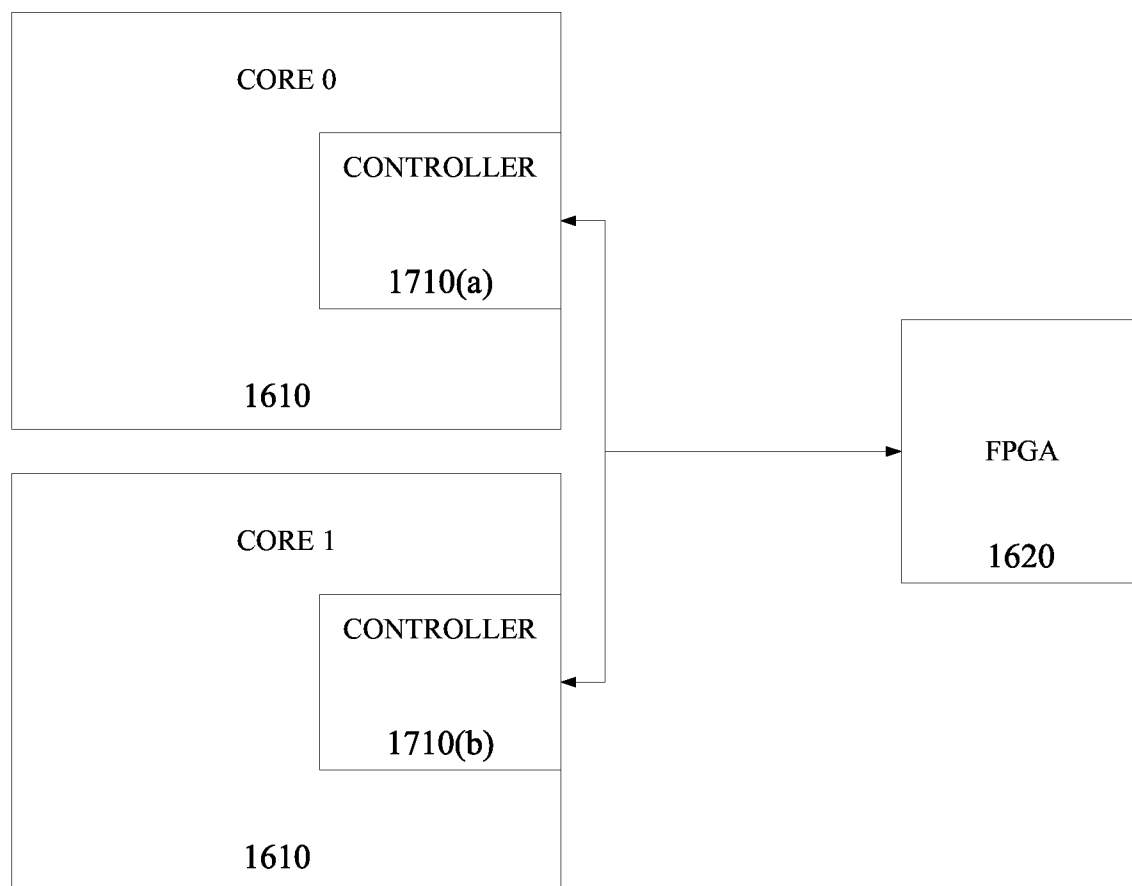


FIG. 14

**FIG. 15**

**FIG. 16A****FIG. 16B**

**FIG. 17A****FIG. 17B**