

CLAIMS:

1. A system for controlling CD uniformity of a wafer in a plasma processing system, comprising:

a wafer support assembly, including a plurality of independently controllable temperature control zones arranged in proximity to device die locations above the temperature control zones; and

a controller configured to:

receive critical device parameters of an incoming wafer and process recipe parameters over a network;

calculate a target trim time and a target temperature profile of the incoming wafer based on the process control and temperature data of the at least one previously processed wafer and the critical device parameters of the incoming wafer; and

adjust the temperature of each device die location for a duration of the target trim time based on the calculated target temperature profile.

2. The system of claim 1, wherein the controller is configured to calculate the target trim time using

$$TrimTimeNew = \frac{AEINewWaferAverage - ADINewWaferAverage - CDBiasWithoutTrimWaferAverage}{AverageTrimRate \left(a + \frac{b}{2} \text{ } ^\circ \text{C.} \right)}$$

where AEINewWaferAverage is the average of the after-etch inspection parameters of the current wafer, ADINewWaferAverage is an average of wafer parameters after development inspection of the incoming wafer, CDBiasWithoutTrimWaferAverage is an average CDBias of a previously processed wafer without a trim step performed, AverageTrimRate is an average of the trim rate of previously processed wafers, a is an ESC temperature of a first previously processed wafer, and b is a difference in ESC temperature of the first previously processed wafer and a second previously processed wafer.

3. The system of claim 1, wherein the controller is configured to calculate the target temperature profile of the current wafer using

$$NewTempMap(x,y)=CurrentBestFile(x,y)+DeltaTemp(x,y),$$

where CurrentBestFile is the temperature profile of a best previously processed wafer, and DeltaTemp is a temperature offset of the incoming wafer to be processed.

4. The system of claim 3, wherein the controller is configured to calculate the DeltaTemp(x,y) based on a difference between temperature values of the best previously processed wafer (TempCurrentBest(x,y)) and temperature values of the incoming wafer (TempNew(x,y)).

5. A non-transitory computer readable medium having program code encoded thereon for performing a method of controlling CD uniformity of a wafer in a plasma processing system having a wafer support assembly including a plurality of independently controllable temperature control zones arranged in proximity to device die locations above the temperature control zones on the wafer, and a controller that controls each temperature control zone, the method comprising:

receiving process control and temperature data associated with at least one wafer previously processed in a plasma chamber of the plasma processing system;

receiving critical device parameters of a current wafer to be processed in the plasma chamber;

calculating a target trim time and a target temperature profile of the current wafer based on the process control and temperature data of the at least one previously processed wafers and the critical device parameters of the current wafer; and

processing the current wafer for a duration of the target trim time where the temperature of each device die location is adjusted based on the target temperature profile.

6. The system of claim 1, wherein the previously processed wafer is a test wafer that was processed using at least one trim time and at least one temperature profile.

7. The system of claim 1, wherein the target trim time is calculated for an entire surface of the wafer.
8. The system of claim 1, wherein the controller calculates the target temperature profile of the current wafer by calculating an operating temperature for each temperature control zone.
9. The system of claim 1, including memory which supplies the process control and temperature data associated with the previously processed wafers.
10. The system of claim 1, including memory which supplies the feature dimensions of the current wafer.
11. The system of claim 1, including a user interface which supplies the feature dimensions of the current wafer.
12. The system of claim 1, wherein the process control data associated with previously processed wafers comprises pre-etch critical device parameters and post-etch parameters.
13. The system of claim 1, wherein the controller recalculates a target etch timing and a target temperature profile for each successive wafer to be processed after the wafer using the process control and temperature data of the previously processed wafers and respective feature dimensions of each successive wafer, respectively received in the plasma processing system.
14. The system of claim 1, wherein the target temperature profile is a spatial temperature profile or a temporal temperature profile.

15. The system of claim 1, wherein the controller maps a sensitivity profile of the received critical device parameters and calculates the target trim time and the target temperature profile based on the mapped sensitivity profile, the process control and temperature data of the previously processed wafers and the critical device parameters of the current wafer.

WHAT IS CLAIMED IS:

1. A method of controlling CD uniformity of the features of a wafer in a plasma processing system, the system having a wafer support assembly including a plurality of independently controllable temperature control zones arranged in proximity to device die locations above the temperature control zones on the wafer, and a controller that controls each temperature control zone, the method comprising:

receiving process control and temperature data associated with at least one wafer previously processed in a plasma chamber of the plasma processing system;

receiving critical device parameters of a wafer currently inserted in the plasma chamber;

calculating a target trim time and a target temperature profile of the current wafer to be processed based on the process control and temperature data of the at least one previously processed wafer and the critical device parameters of the current wafer; and

processing the current wafer for a duration of the target trim time where the temperature of each device die location is adjusted based on the target temperature profile.

2. The method of claim 1, wherein the previously processed wafers are test wafers that are processed using at least one trim time and at least one temperature profile.

3. The method of claim 1, wherein the target trim time is calculated for an entire surface of the wafer.

4. The method of claim 1, wherein calculating the target temperature profile of the current wafer comprises calculating an operating temperature for each temperature control zone.
5. The method of claim 1, wherein the process control and temperature data associated with the previously processed wafers received from memory.
6. The method of claim 1, wherein the feature dimensions of the current wafer are received from memory.
7. The method of claim 1, wherein the feature dimensions of the current wafer are received from a user interface.
8. The method of claim 1, wherein the process control data associated with previously processed wafers comprises pre-etch critical device parameters and post-etch parameters.
9. The method of claim 1, further comprising:
recalculating a target etch timing and a target temperature profile for each successive wafer to be processed after the wafer using the process control and temperature data of the previously processed wafers and respective feature dimensions of each successive wafer, respectively received in the plasma processing system.
10. The method of claim 1, wherein the target temperature profile is a spatial temperature profile or a temporal temperature profile.
11. The method of claim 1, comprising:
mapping a sensitivity profile of the received critical device parameters; and
calculating the target trim time and the target temperature profile based on the mapped sensitivity profile, the process control and temperature data of the

previously processed wafers and the critical device parameters of the current wafer.

12. The method of claim 1, wherein the at least one previously processed wafer is processed at a time that is temporally adjacent to the current wafer.

13. The method of claim 1, wherein the at least one previously processed wafer is processed at any time prior to receiving the current wafer in the plasma processing chamber.

14. The method of claim 1, wherein the at least one previously processed wafer comprises a batch of wafers.

15. The method of claim 14, wherein the process temperature data of the at least one wafer is an average of the process temperature data of the batch of wafers.

16. The method of claim 1, wherein the target trim time is calculated based using

TrimTimeNew

$$= \frac{AEINewWaferAverage - ADINewWaferAverage - CDBiasWithoutTrimWaferAverage}{AverageTrimRate \left(a + \frac{b}{2}^{\circ}\text{C} \right)}$$

where *AEINewWaferAverage* is the average of the after-etch inspection parameters of the current wafer, *ADINewWaferAverage* is the average of wafer parameters after development inspection of the current wafer, *CDBiasWithoutTrimWaferAverage* is an average CDBias of a previously processed wafer without a trim step performed, *AverageTrimRate* is an average of the trim rate of previously processed wafers, *a* is an ESC temperature of a first previously processed wafer, and *b* is a difference in ESC temperature of the first previously processed wafer and a second previously processed wafer.

17. The method of claim 1, wherein the target temperature profile of the current wafer is calculated using

$$NewTempMap(x,y)=CurrentBestFile(x,y)+DeltaTemp(x,y),$$

where *CurrentBestFile* is the temperature profile of the best previously processed wafer, and *DeltaTemp* is a temperature offset of the current wafer to be processed.

18. A system for controlling CD uniformity of a wafer in a plasma processing system, comprising:

a wafer support assembly, including a plurality of independently controllable temperature control zones arranged in proximity to device die locations above the temperature control zones; and

a controller configured to:

receive critical device parameters of an incoming wafer and process recipe parameters over a network;

calculate a target trim time and a target temperature profile of the incoming wafer based on the process control and temperature data of the at least one previously processed wafer and the critical device parameters of the incoming wafer; and

adjust the temperature of each device die location for a duration of the target trim time based on the calculated target temperature profile.

19. The system of claim 18, wherein the controller is configured to calculate the target trim time using

$$\text{TrimTimeNew} = \frac{\text{AEINewWaferAverage} - \text{ADINewWaferAverage} - \text{CDBiasWithoutTrimWaferAverage}}{\text{AverageTrimRate} \left(a + \frac{b}{2}^{\circ}\text{C} \right)}$$

where *AEINewWaferAverage* is the average of the after-etch inspection parameters of the current wafer, *ADINewWaferAverage* is an average of wafer parameters after development inspection of the incoming wafer, *CDBiasWithoutTrimWaferAverage* is an average CDBias of a previously processed wafer without a trim step performed, *AverageTrimRate* is an average of the trim rate of previously processed wafers, *a* is an ESC temperature of a first previously processed wafer, and *b* is a difference in ESC temperature of the first previously processed wafer and a second previously processed wafer.

20. The system of claim 19, wherein the controller is configured to calculate the target temperature profile of the current wafer using

$$\text{NewTempMap}(x,y) = \text{CurrentBestFile}(x,y) + \text{DeltaTemp}(x,y),$$

where *CurrentBestFile* is the temperature profile of a best previously processed wafer, and *DeltaTemp* is a temperature offset of the incoming wafer to be processed.

21. The system of claim 20, wherein the controller is configured to calculate the *DeltaTemp(x,y)* based on a difference between temperature values of the best previously processed wafer (*TempCurrentBest(x,y)*) and temperature values of the incoming wafer (*TempNew(x,y)*).

22. A non-transitory computer readable medium having program code encoded thereon for performing a method of controlling CD uniformity of a wafer in a plasma processing system having a wafer support assembly including a plurality of independently controllable temperature control zones arranged in proximity to device die locations above the temperature control zones on the wafer, and a controller that controls each temperature control zone, the method comprising:

receiving process control and temperature data associated with at least one wafer previously processed in a plasma chamber of the plasma processing system;

receiving critical device parameters of a current wafer to be processed in the plasma chamber;

calculating a target trim time and a target temperature profile of the current wafer based on the process control and temperature data of the at least one previously processed wafers and the critical device parameters of the current wafer; and

processing the current wafer for a duration of the target trim time where the temperature of each device die location is adjusted based on the target temperature profile.