

FIG. 1

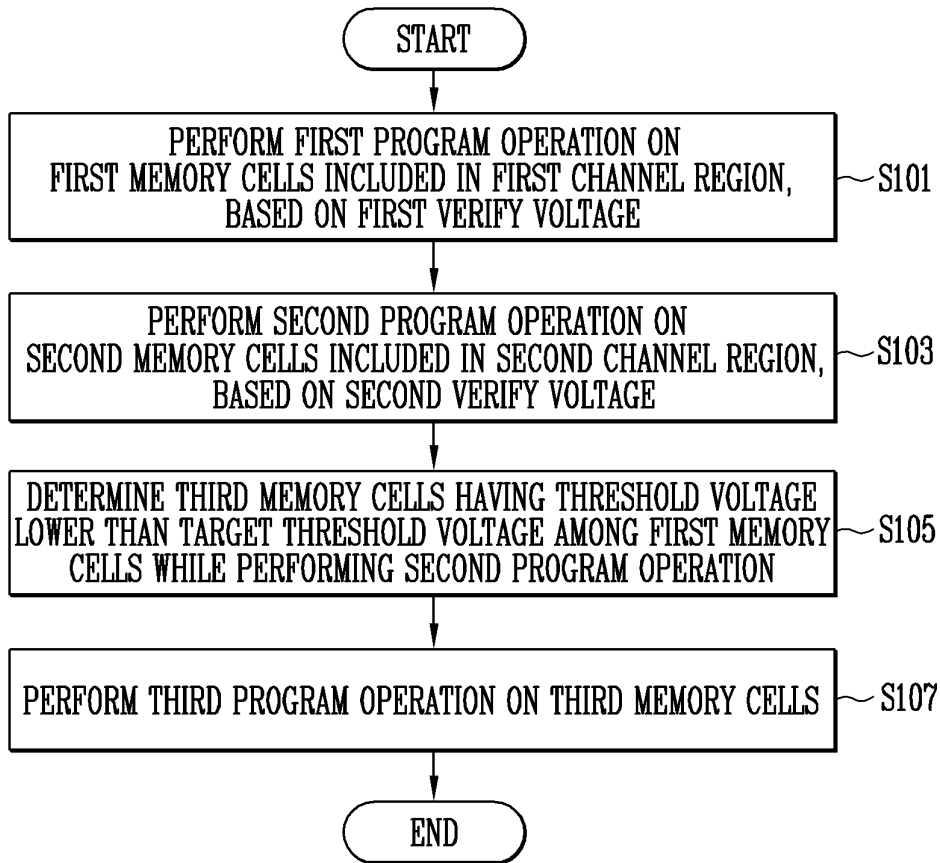


FIG. 2

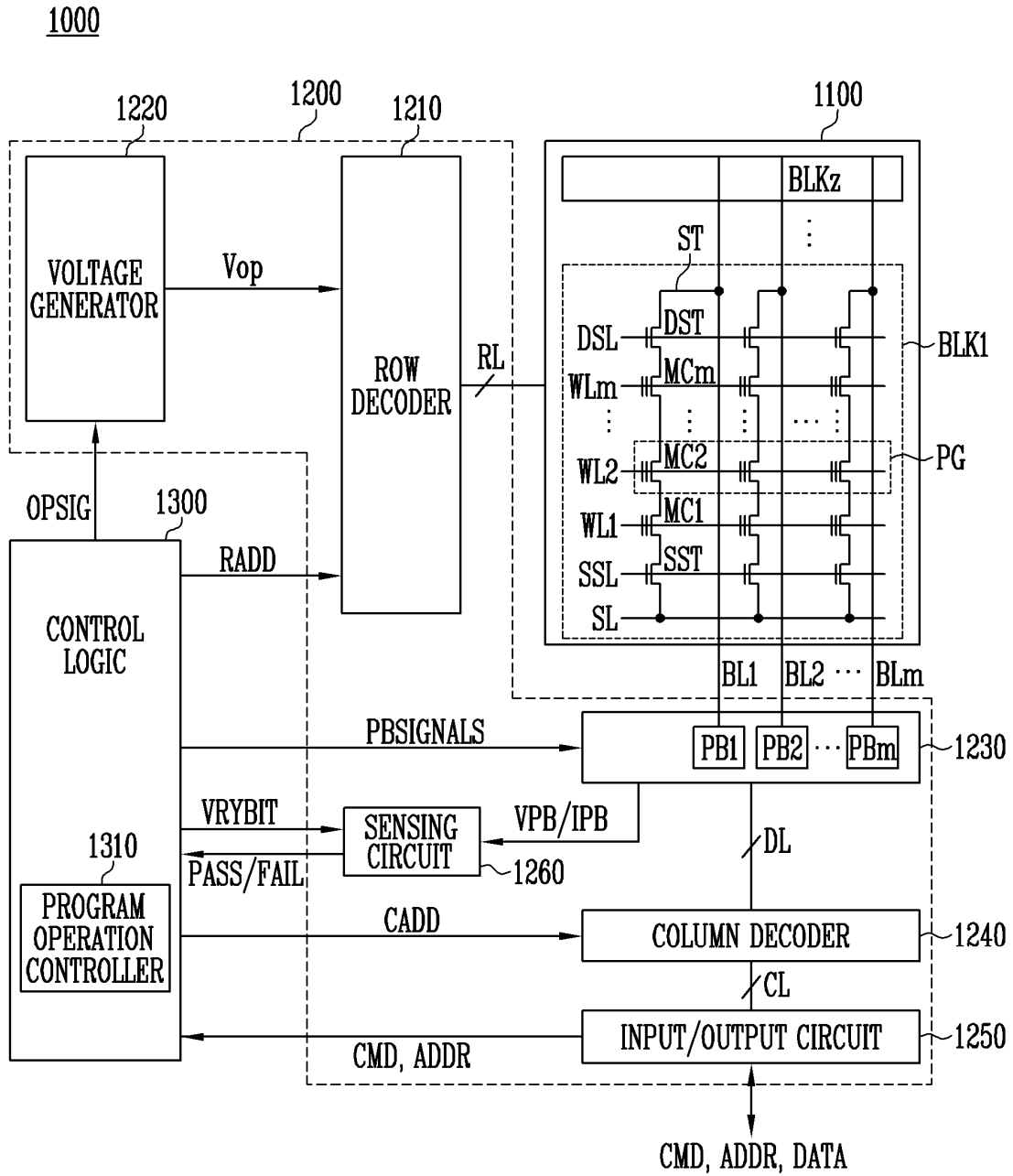


FIG. 3A

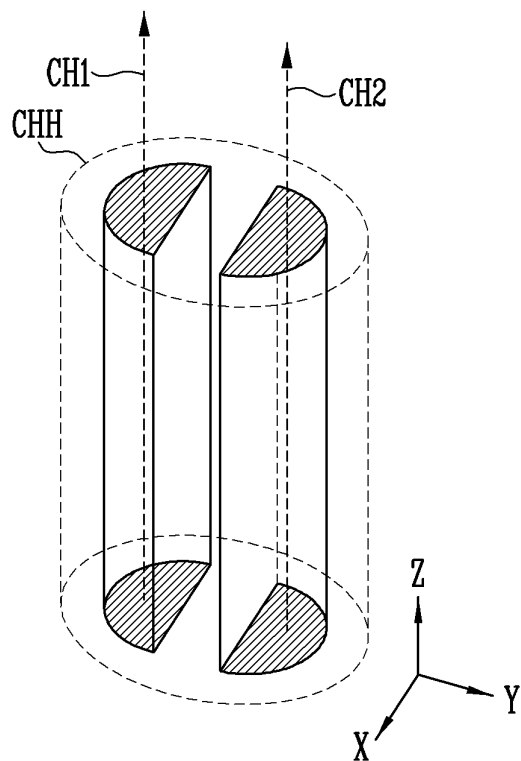


FIG. 3B

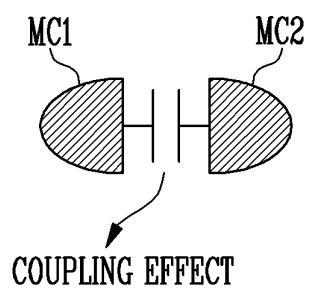


FIG. 4

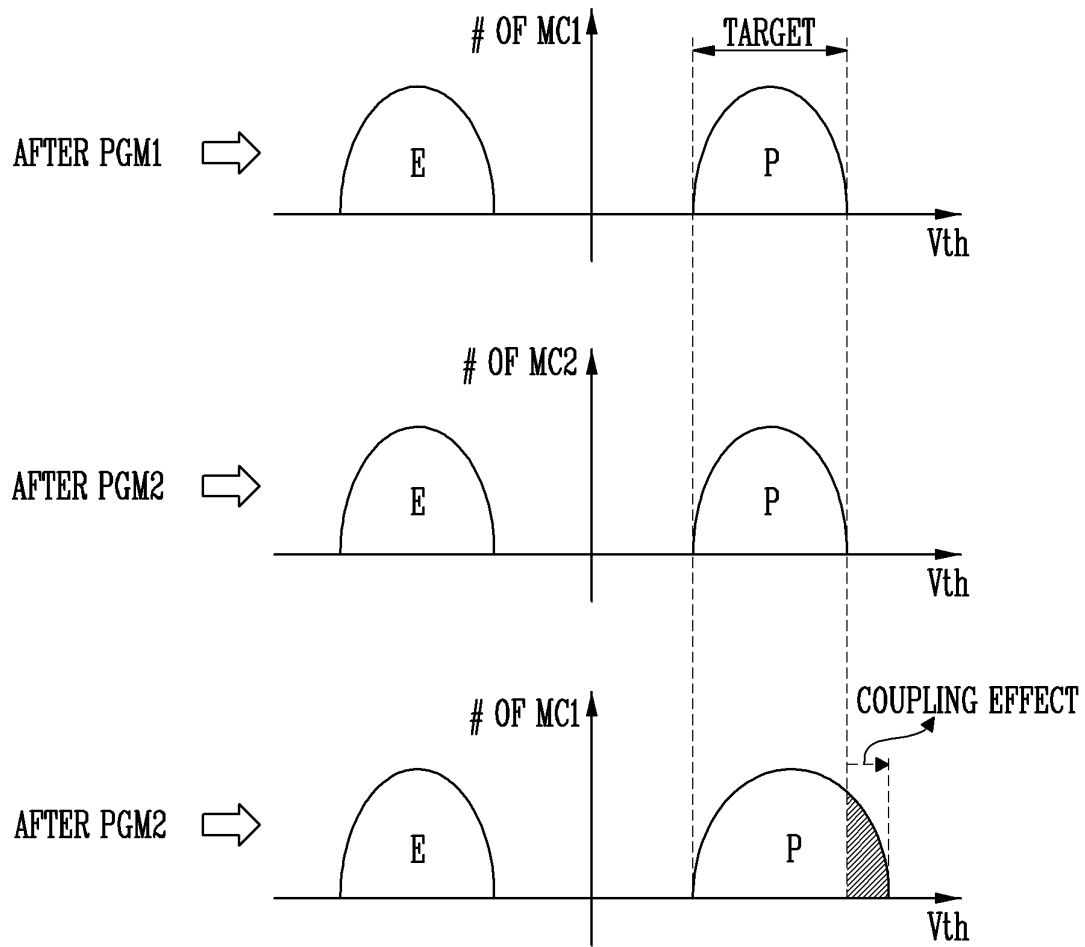


FIG. 5

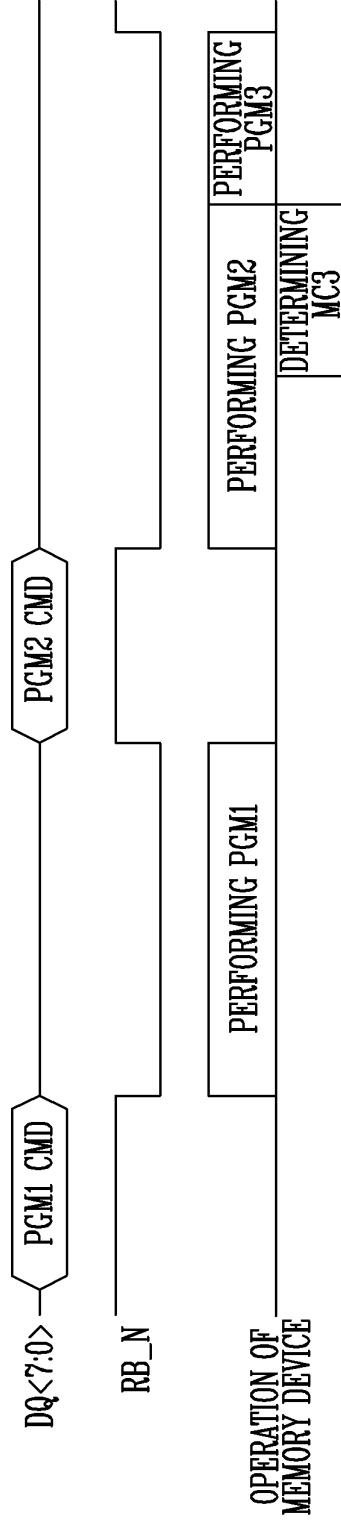


FIG. 6

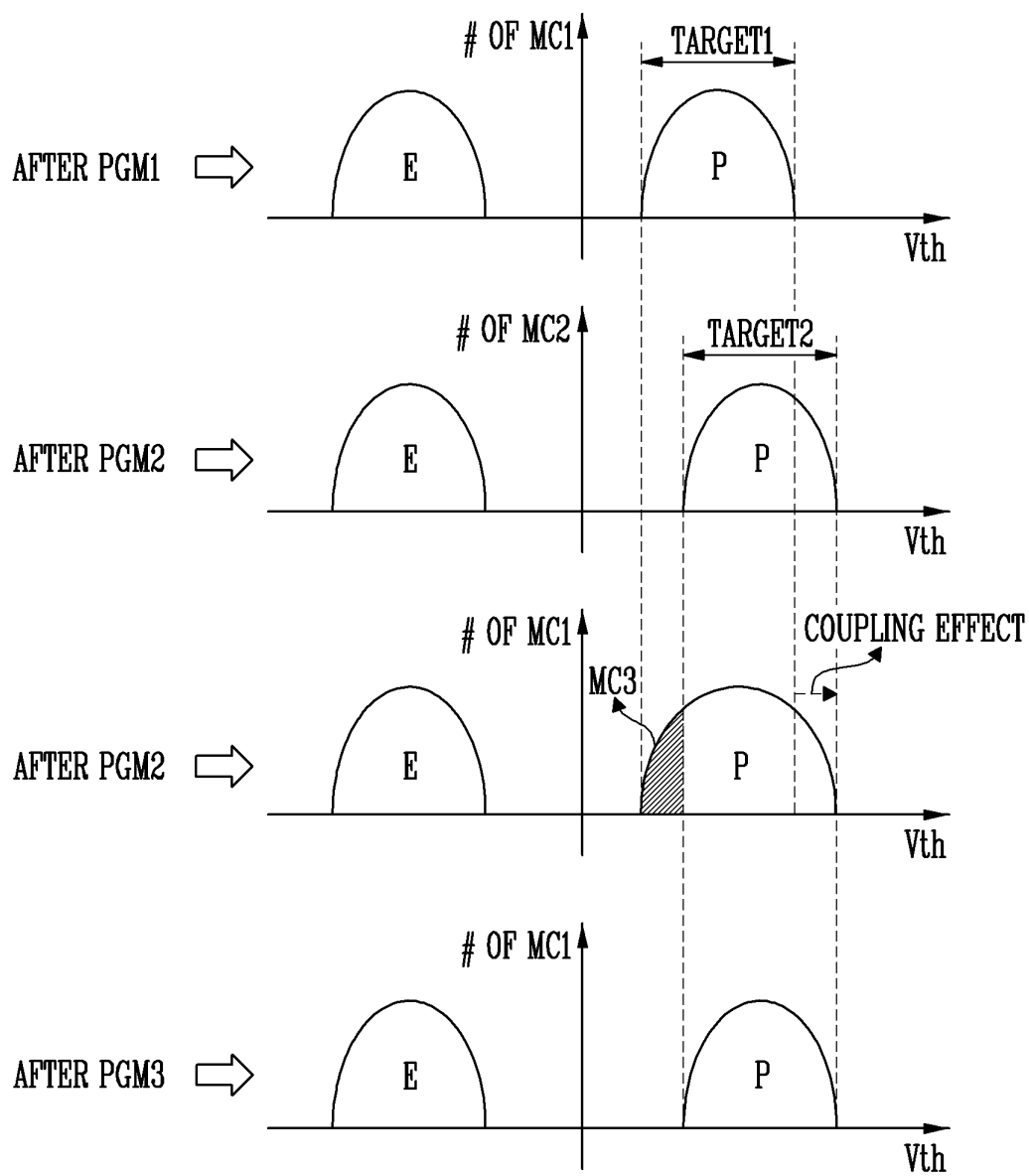


FIG. 7

DIVISION	PGM1	PGM2	SIZE COMPARISON
START PROGRAM VOLTAGE	V_{pgm1}	V_{pgm2}	$V_{pgm1} < V_{pgm2}$
UNIT VOLTAGE	$\Delta V1$	$\Delta V2$	$\Delta V1 > \Delta V2$
VERIFY VOLTAGE	V_{vfy1}	V_{vfy2}	$V_{vfy1} < V_{vfy2}$
PROGRAM PASS VOLTAGE	V_{passP1}	V_{passP2}	$V_{passP1} < V_{passP2}$
VERIFY PASS VOLTAGE	V_{passV1}	V_{passV2}	$V_{passV1} < V_{passV2}$

FIG. 8A

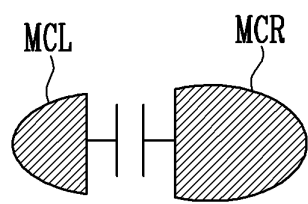


FIG. 8B

DIVISION	MCL	MCR
NUMBER OF BITS STORED IN MEMORY CELL	m	n (AT THIS TIME, $n > m$)
PROGRAM ORDER	1st	2nd

FIG. 9

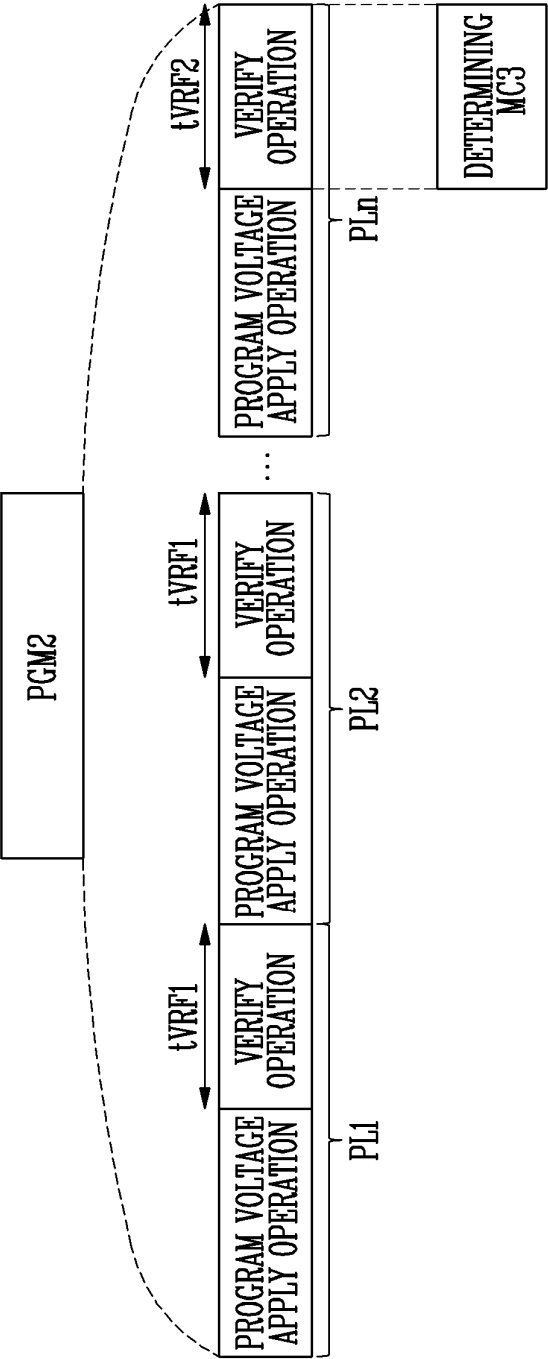


FIG. 10

