CLAIMS

1. A semiconductor storage device comprising:

a substrate;

a plurality of first conductive layers provided above the substrate, the plurality of first conductive layers being mutually separated in a first direction;

a pillar penetrating the plurality of the first conductive layers, the pillar including a first semiconductor layer extending in the first direction, a part of the pillar that intersects with the first conductive layers functioning as memory cells; and

a second conductive layer provided above the plurality of first conductive layers and being in direct contact with the first semiconductor layer, the second conductive layer being made of a metal or a silicide.

2. The semiconductor storage device of claim 1, further comprising:

a first insulating layer provided between the plurality of first conductive layers and the second conductive layer and being in contact with the second conductive layer, wherein

an interval in the first direction between the substrate and a boundary portion between the first semiconductor layer and the second conductive layer is shorter than an interval in the first direction between the first insulating layer and the substrate.

3. The semiconductor storage device of claim 2, further

comprising:

a third conductive layer provided between the plurality of first conductive layers and the first insulating layer and being penetrated by the pillar, wherein

a location of the boundary portion is included at a height at which the third conductive layer is provided.

4. The semiconductor storage device of claim 1, further comprising:

a third conductive layer provided between the plurality of first conductive layers and the second conductive layer and being penetrated by the pillar, wherein

no conductive layer is included between the third conductive layer and the second conductive layer, and

an interval in the first direction between the third conductive layer and the second conductive layer is equal to or shorter than 50 nm.

5. The semiconductor storage device of any one of claims 1 to 4, further comprising:

a fourth conductive layer provided between the substrate and the plurality of first conductive layers and electrically coupled to the first semiconductor layer, wherein

the second conductive layer is used as a source line, and

the fourth conductive layer is used as a bit line.

6. The semiconductor storage device of claim 5, further comprising:

a control circuit configured to perform a read operation, wherein

in a read operation the control circuit applies, when determining a threshold voltage of a memory cell, a first voltage to the source line and a second voltage higher than the first voltage to the bit line.

7. The semiconductor storage device of claim 5, further comprising:

a control circuit configured to perform a read operation, wherein

in a read operation the control circuit applies, when determining a threshold voltage of a memory cell, a third voltage to the source line and a fourth voltage lower than the third voltage to the bit line.

8. The semiconductor storage device of any one of claims 1 to 7, wherein

the second conductive layer includes any one selected from the group consisting of titanium, titanium silicide, titanium nitride, nickel silicide, and tungsten.

9. The semiconductor storage device of any one of claims 1 to 8, wherein

a concentration of impurity in the first semiconductor layer is 10^{19} (atoms/cm^3) or lower.

10. The semiconductor storage device of any one of claims 1 to 9, further comprising:

a first chip that includes the substrate and a first junction metal coupled to a circuit formed in the substrate;

and

a second chip that includes the plurality of first conductive layers, the second conductive layer, the pillar, and a second junction metal coupled to the pillar, wherein

the first junction metal and the second junction metal are coupled to each other.