

## SPECIFICATION

### Electronic timer

This invention relates to electronic timers. In conventional electronic timers which measure

- 5 time preset in a counter which successively subtract time units from the preset time to report the time when the preset time has elapsed, it is accepted practice to display the remaining time so that the passage of time may be known.
- 10 Therefore, in the case where time has passed the preset time, it is difficult quickly to know at a glance what amount of time has elapsed.

- According to one aspect of the present invention there is provided an electric timer
- 15 comprising: a liquid crystal display device consisting of a plurality of circularly arranged spaced apart common electrodes, a plurality of radially arranged segment electrodes, and liquid crystal material disposed between the common
- 20 electrodes and the segment electrodes to constitute a plurality of liquid crystal display elements arranged so as to simulate the hands of a mechanical timepiece when energised; a storage circuit for storing preset time data; a down-
- 25 counter for receiving time-keeping data and, in operation, carrying out a down-count operation upon receipt of pulses of a predetermined period; and selection circuit means for selectively passing the output of the storage circuit and the output of
- 30 the down-counter to a drive circuit which drives the display device.

The common electrodes may consist of a plurality of radially arranged inner electrodes and a plurality of radially arranged outer electrodes.

- 35 In one embodiment the electronic timer includes a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a
- 40 common voltage supplying circuit for driving the common electrodes; the selection circuit means being arranged to be controlled by the pulsiform signals for selectively passing the output of the storage circuit and the output of the down-counter
- 45 to the segment voltage supplying circuit and the common voltage supplying circuit.

- The electronic timer may include means for applying to said drive circuit a signal for causing a display element to indicate when time counting is
- 50 complete.

- According to a further aspect of the present invention there is provided an electronic timer comprising: a liquid crystal display device consisting of a plurality of circularly arranged
- 55 spaced apart common electrodes, a plurality of radially arranged segment electrodes, and a liquid crystal material disposed between the common electrodes and the segment electrodes to constitute a plurality of liquid crystal display
- 60 elements arranged so as to simulate the hands of a mechanical timepiece when energised; a storage circuit for storing preset time data; a down-counter for receiving time-keeping data; and, in operation, carrying out the down-count operation

- 65 upon receipt of pulses of a predetermined period; a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a common
- 70 voltage supplying circuit for driving the common electrodes; and selection circuit means arranged to be controlled by said pulsiform signals for selectively passing the output of the storage circuit and the output of the down-counter to the
- 75 segment voltage supplying circuit and the common voltage supplying circuit.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

- 80 Figure 1 is a cross-section of a display device of an electronic timer according to the present invention;

Figures 2 and 3 illustrate the arrangement of electrodes of the display device of Figure 1;

- 85 Figure 4 is a front view of an electronic timer according to the present invention;

Figure 5 is a block diagram of one embodiment of an electronic timer according to the present invention;

- 90 Figure 6 is a circuit diagram of an output conversion circuit of a segment supply circuit of the electronic timer of Figure 5;

Figure 7 is a diagram showing voltage waveforms which are applied to common electrodes and to segment electrodes shown in Figures 2 and 3;

- 95 Figure 8 illustrates the display produced by a second embodiment of an electronic timer according to the present invention;

- 100 Figure 9 is a block diagram of the second embodiment of the electronic timer of Figure 8;

Figure 10 is a circuit diagram of a common voltage supply circuit of the electronic timer of Figure 9;

- 105 Figure 11 is a diagram of voltage waveforms applied to common electrodes and to segment electrodes of the electronic timer of Figure 9;

Figure 12 illustrates the display produced by a third embodiment of an electronic timer according to the present invention;

- 110 Figures 13 and 14 are diagrams of parts of the circuit of the electronic timer of Figure 12;

Figure 15 illustrates the display produced by a fourth embodiment of an electronic timer according to the present invention;

- 115 Figures 16 and 17 illustrate the arrangement of electrodes of a liquid crystal display device of another embodiment of an electronic timer according to the present invention;

- 120 Figure 18 is a front view of an electronic timer having the liquid crystal display device of Figures 16 and 17;

Figures 19 to 23 illustrate various displays produced by further embodiments of electronic timers according to the present invention; and

- 125 Figures 24A and 24B are block diagrams of an electronic timer for producing the display of Figure 23.

Referring first to Figure 1, there is illustrated a

liquid crystal display device of an electronic timer according to the present invention. The display device comprises two opposed glass plates 1, 2 which are maintained a predetermined distance apart with a liquid crystal material 3 therebetween. On the inner surface of the glass plate 1 are formed six fan shaped or radially arranged common electrodes 4 as shown in Figure 2. Terminals  $C_0$  to  $C_5$  are lead out from the common electrodes. On the inner surface of the glass plate 2 are formed 60 radially arranged segment electrodes 5 as shown in Figure 3. The segment electrodes 5 at predetermined positions are successively connected by lead electrodes 6 and are connected to ten terminals  $e_0$  to  $e_9$ .

Figure 4 is a front view of a 60 minute electronic timer according to the present invention having a dial with time graduations 7 which divide the circumference into 60 equal segments, time graduations 8 for indicating minutes, and a graduation 9 which indicates when time counting is complete.

The circuit of one embodiment of an electronic timer according to present invention is shown in Figure 5. The output of quartz crystal oscillator 10 is converted into pulse signals of a period of one minute through frequency dividers 11, 12. The pulse signals are applied to a down-counter 13 of the presetting type which is capable of setting time data of units of minutes, and a carry output of the down-counter 13 is applied to a down-counter 14 of the presetting type which is capable of setting the time data of tens of minutes. With reference to the preset time the units of minutes are set in a storage circuit 15 and tens of minutes are set in a storage circuit 16. One output of the frequency divider 11 is applied to a pulse generator 17 whereby timing pulses are formed depending upon the pulse being applied, and pulses appear at the terminals  $P_1$ ,  $P_2$  thereof. Pulses which are successively generated at the terminals  $P_1$ ,  $P_2$  are applied to selection circuits 18, 19 composed of gate circuits.

The selection circuit 18 alternately selects the respective outputs of the down-counter 13 and the storage circuit 15 on receipt of the pulses  $P_1$ ,  $P_2$ . The selection circuit 19 alternately selects the respective outputs of the down counter 14 and the storage circuit 16 on receipt of the pulses  $P_1$ ,  $P_2$ . A discriminator circuit 22 produces a signal for changing the order of the input and output data of an output conversion circuit 23, depending upon whether the output data of the selection circuit 19 fed to a decoder 21 is of even number or odd number. The output of the output conversion circuit 23 causes a segment voltage supply circuit 24 to produce predetermined outputs at the terminals  $e_0$  to  $e_9$ . The output of the decoder 21, on the other hand, causes a common voltage supply circuit 25 to produce predetermined output voltages at the terminals  $C_0$  to  $C_5$ . Switching circuits 26, 27 composed of analog switches receive an output from an AND gate circuit 28 whereby one of them is closed and the other opened so that voltage applied to terminals 26a,

27a is produced at terminal 24a. The AND gate circuit 28 produces an output when it has received a pulse from the frequency divider 11 and a pulse generated at the terminal  $P_1$  of the pulse generator 17. The output level of the AND gate circuit 28 is inverted by an inverter 29 and is then fed to the switching circuit 26.

Figure 6 illustrates in greater detail the output conversion circuit 23 and the segment voltage supply circuit 24. The outputs of the decoder 20 are fed to switching circuits 45 to 47 which are analog switches *via* AND gate circuits 30 to 39 and OR gate circuits 40 to 44 and to switching circuits 46, 48 *via* inverters 49, 50.

The pulse generator 17 of Figure 5 alternately produces through its terminals  $P_1$ ,  $P_2$  pulses of a frequency of 128 Hz to display the preset time and the remaining time in a time-divisional manner. When a pulse at the terminal  $P_1$  is fed to the selection circuits 18, 19, which select the contents in the down counters 13, 14, respectively, the selected respective contents are supplied to the decoders 20, 21 respectively. On the other hand, when a pulse at the terminal  $P_2$  is fed to the selection circuits 18, 19, which select the preset time data in the storage circuits 15, 16, the selected respective time data is fed to the decoders 20, 21, respectively. Provided that the respective data of 0 to 9 minutes is successively fed to the decoder 20, a logic 1 appears at a corresponding 1 of terminals  $d_0$  to  $d_9$ , a logic 0 appearing at the remaining terminals. For examples, when the input data to the decoder 20 is 3 minutes, logic 1 is produced at the terminal  $d_3$  and logic 0 is produced at the remaining terminals  $d_0$  to  $d_2$  and  $d_4$  to  $d_9$ .

The decoder 21 works in the same manner as the decoder 20, namely when the data is less than 10 minutes and in the range 10 minutes to 50 minutes, logic 1 is produced at one of the terminals  $d_0$  to  $d_5$ .

On the other hand, when data of the order of 10 minutes is an even number, a logic 1 appears at a terminal  $w_1$  of the discriminator circuit 22 and when data of 10 minutes is an odd number, a logic 1 is produced at a terminal  $w_2$  of the discriminator circuit 22. Therefore, when data of 10 minutes is 0, 2, 4, 6, or 8, the respective AND gate circuits 30, 32, 34, 36 or 38 is opened, whereby the output of the switching circuit is produced at the terminals  $e_0$  to  $e_9$  being selected by the output from the terminals  $d_0$  to  $d_9$  of the decoder 20. When data of tens of minutes is an odd number, the respective AND gate circuits 31, 33, 35, 37 or 39 is opened, and the output of the switching circuit is produced at the terminals  $e_0$  to  $e_9$  being selected by the output from the terminals  $d_0$  to  $d_9$  of the decoder 20.

Responsive to the outputs of the output conversion circuit 23 and the decoder 21, the segment voltage supply circuit 24 and the common voltage supply circuit 25 produce the following outputs. First, assuming that pulses shown in Figure 7 are fed to input terminals 26a, 27a of the switching circuits 26, 27 and to input

terminals 25a, 25b of the common voltages supply circuit 25, which are illustrated in Figure 5.

The liquid crystal material turns ON when a voltage | 3V | is periodically applied, and turns OFF when a voltage | 1V | is periodically applied. Therefore, the liquid crystal material is turned ON when the common electrode is applied with a pulse from the terminal 25a and the segment electrode is applied with a pulse from the terminal 26a, and is turned OFF in other cases. When any one output from the output conversion circuit 23 is logic 0, a pulse appearing on the terminal 27a is fed to the segment electrode via a selected one of the switching circuits 46 to 48 of Figure 6. When any one output from the output conversion circuit 23 is logic 1, a pulse appearing on the terminal 24a is fed to the segment electrode via a selected one of the switching circuits 45 to 47.

Pulses appearing at the terminal 24a will now be described with reference to Figure 5. The output of the AND gate circuit 28 remains logic 0 while pulses are being generated at the terminal P<sub>2</sub> of the pulse generator 17, whereby at the terminal 24a appears pulses that are applied to the terminal 26a via the switching circuit 26. When any one pulse is generated at the terminal P<sub>1</sub>, pulses appearing at the terminal 27a and pulses appearing at the terminal 26a are alternately produced at an interval of one second at the terminal 24a because pulses of 1Hz are fed to the AND gate circuit 28 from the frequency divider 11.

On the other hand, when any one output of the decoder 21 is logic 1, the common voltage supply circuit 25 produces a pulse applied to the terminal 25a at any selected output terminal thereof, and when any one output of the decoder 21 is logic 0, the common voltage supply circuit 25 produces a pulse applied to the terminal 25b at any selected output terminal thereof.

For example, assuming that a preset time of 25 minutes is indicated by a display element 5a and a remaining time of 13 minutes is indicated by a display element 5b as shown in Figure 4, in this condition when pulses are periodically produced at the terminal P<sub>1</sub> of Figure 5, pulses applied to the terminals 26a and 27a respectively alternately appear at the terminal e<sub>s</sub> of the segment voltage supply circuit 24 and pulses applied to the terminal 27a appear at all other terminals except the terminal e<sub>s</sub>.

On the other hand, pulses applied to the terminal 25a appear at the terminal C<sub>1</sub> of the common voltage supply circuit 25 and pulses applied to the terminal 25b appear at all other terminals except the terminal C<sub>1</sub>. Accordingly, the display element 5b flash to display a remaining time of 13 minutes.

Then, when any one pulse is generated at the terminal P<sub>2</sub>, pulses applied to the terminal 26a appear at the terminal e<sub>s</sub> of the segment voltage supply circuit 24, and pulses applied to the terminal 27a appear at all other terminals except the terminal e<sub>s</sub>. On the other hand, the terminal C<sub>2</sub> of the common voltage supply circuit 25 produces

pulses applied to the terminal 25a, and other terminals produce pulses applied to the terminal 25b. Therefore, the display element 5a is turned ON to display the set time of 25 minutes.

Figure 8 shows the display produced by a second embodiment of an electronic timer according to the present invention in which a display element 5c to display a preset time is turned ON and display elements from a display element 5d to the graduation 9 flash. Figure 8 indicates that the time has been set to 40 minutes and the remaining time is 23 minutes.

Figure 9 is a circuit diagram of the second embodiment of an electronic timer according to the present invention in which decoders 51, 52 and a common voltage supply circuit 53 are different from those shown in Figure 5. The decoders 51, 52 produce outputs for displaying the remaining time in a cumulative manner. When the contents of the counter 13 are 0 to 9, the decoder 51 produces outputs of logic 1 at the terminals d<sub>10</sub>, (d<sub>10</sub>, d<sub>11</sub>), ... (d<sub>10</sub>...d<sub>18</sub>), (d<sub>10</sub>...d<sub>19</sub>), respectively. The decoder 52 also works in the same manner.

Figure 10 illustrates in detail a portion of the common voltage supply circuit 53 in which reference numerals 54 to 60, 62, 64, 65, 67, 68 denote AND gate circuits, reference numerals 61, 63, 66 denote OR gate circuits, reference numerals 69 to 77 denote switching circuits, and reference numerals 78 to 81 denote inverters. Reference numerals which are the same as those of Figure 5 denote circuits having the same functions as those of Figure 5. Only a part of the common voltage supply circuit 53 in Figure 10 is shown for the reason that the same circuits as provided for the terminal t<sub>1</sub> or t<sub>2</sub> are also provided for the terminals t<sub>3</sub> and t<sub>4</sub> except for the final terminal t<sub>5</sub>. In other words there is provided for the terminals t<sub>3</sub> or t<sub>4</sub> the same circuit consisting of the AND gate circuits 58, 59, 67, 68, OR gate circuit 66, switching circuits 75, 76, 77 as provided for the terminal t<sub>2</sub>. The circuit for the terminal t<sub>5</sub> is different from the circuit provided for the terminals t<sub>1</sub> to t<sub>4</sub>. The circuit for the terminal t<sub>5</sub> consists of two switching circuits one of which receives pulses appearing at terminal 53b and is switched ON and OFF by directly receiving an output from the terminal t<sub>5</sub>, the other receives pulses appearing at terminal 53a and is switched ON and OFF by an output from the terminal t<sub>5</sub> inverted by an inverter. The respective output terminals of the two switching circuits are connected in common and the common terminal is connected to the terminal C<sub>5</sub>. With respect to the above circuits, in explaining the basis of the circuit provided for the terminal t<sub>2</sub>, assuming that the terminal t<sub>5</sub> is substituted for the terminal t<sub>2</sub>, the AND gate circuits 58, 59, 67, 68, OR gate circuit 66 and switching circuit 77 are removed, an output from the terminal t<sub>5</sub> is directly fed to the switching circuit 76 and is fed via the inverter 80 to the switching circuit 75.

First, the operation for displaying the remaining time in a flashing manner will be described with

reference to the case when a time of 23 minutes is to be displayed as shown in Figure 8. In this case, the contents of the counters 14, 13 of Figure 9 are 2 and 3, respectively, whereby a logic 1 is produced at the terminals  $d_{30}$  to  $d_{32}$  of the decoder 52 and at the terminals  $d_{10}$  to  $d_{13}$  of the decoder 51.

When pulses are periodically generated at the terminal  $P_1$ , the outputs of the decoders 51 and 52 are selected, so that a logic 1 is produced at the terminals  $t_0$  to  $t_2$  of the selection circuit 19. Here, the output of the discriminator circuit 22 causes the output of the decoder 51 to be directly produced by the output conversion circuit 23, so that the output terminals  $s_0$  to  $s_3$  produce a logic 1. Since the terminals  $t_0$  to  $t_2$  assume a logic 1, the AND gate circuits 55, 57 of Figure 10 produce a logic 1. Further, since the terminal  $t_3$  assumes a logic 0, the AND gate circuit 58 produces a logic 1 as will be recognised from the periodic nature of the circuit. Moreover since a terminal  $n$  is fed with pulses of 1 Hz from the frequency divider 11 of Figure 9, the AND gate circuits 60, 64 and the AND gate circuits 62, 65 open alternately maintaining a period of 1 second.

Therefore, the switching circuits 69, 71 are alternately turned ON and the switching circuits 72, 74 are alternately turned ON such that pulses from the terminals 53a, 53c are alternately generated at the terminals  $C_0$ ,  $C_1$ .

The terminals 53b, 53a, 53c are fed with pulses which are shown in Figure 11, as the pulses is fed from the terminals 53a to the common electrode, the corresponding display elements are all turned OFF. The display elements are all turned ON upon receipt of pulses from the terminal 53c. Therefore, all of the display elements from 0 to 19 minutes corresponding to common electrodes which are connected to the terminals  $C_0$ ,  $C_1$  of Figure 9 flash.

On the other hand, the AND gate circuit 58 of Figure 10 produces a logic 1, so that the switching circuit 76 is turned ON, pulses are fed from the terminal 53b to the terminal  $C_2$ , and pulses are fed from the terminal 53a to the terminals  $C_3$  to  $C_6$ . Therefore, the display elements from 30 to 58 corresponding to common electrodes which are connected to the terminals  $C_3$  to  $C_6$ , are all turned OFF. The display state of the display elements of the order of 20 minutes is controlled by pulses which are fed to the segment electrodes. Since the terminals  $s_0$  to  $s_3$  of the output conversion circuit 23 of Figure 9 assume a logic 1, the terminals  $e_0$  to  $e_3$  of the segment voltage supply circuit 24 are served with pulses from the terminal 24a i.e. alternately fed with pulses from the terminals 26a, 27a maintaining a period of one second, and the terminals  $e_4$  to  $e_9$  are fed with pulses from the terminal 27a. Therefore, the display elements of 20 to 23 minutes flash, and the display elements of 24 to 29 minutes are turned OFF.

As mentioned above, the remaining time is displayed in a flashing manner as shown in Figure 8.

With reference to the preset time, the display elements corresponding to the preset time only are turned ON by pulses which are periodically produced from the terminal  $P_2$  of Figure 9 in the same manner as the aforementioned embodiment of the present invention.

Figure 12 illustrates a third embodiment of an electronic timer according to the present invention in which a preset time is displayed in the same manner as in the above-mentioned two embodiments of the present invention. However, the remaining time is displayed by causing a boundary display element 5e to flash and the display elements from the graduation line 9 to a display element just before the display element 5e are turned ON.

With reference to the circuit for effecting this display, the segment voltage supply circuit 24 of Figure 9 must be modified as shown in Figure 13 and the common voltage supply circuit 53 must be modified as shown in Figure 14. The circuits of Figures 13 and 14 are similarly constructed and reference numerals 82 to 87 and 100 to 105 denote AND gate circuits, reference numerals 88 to 96 and 106 to 114 denote switching circuits, and reference numerals 97 to 99 and 115 to 117 denote inverters. Figure 13 shows only part of the whole circuit of the segment voltage supply circuit 24 for the reason that the segment voltage supply circuit 24 is constructed by a repetition of the same circuit configuration as provided for the terminals  $s_1$  or  $s_2$  except for a circuit provided for the final terminal  $s_9$ . The circuit provided for the terminal  $s_9$  consists of two switching circuits one of which receives pulses appearing at the terminal 24a and is switched ON and OFF by directly receiving an output from the terminal  $s_9$ , the other receives pulses appearing at the terminal 27a and is switched ON and OFF by an output from the terminal  $s_9$  inverted by an inverter. The respective output terminals of two switching circuits are connected in common and the common terminal is connected to the terminal  $e_9$ . In Figure 14, the circuit has a similar configuration as mentioned with reference to Figure 13.

Operation of this embodiment will be described with reference to a remaining time of 22 minutes as shown in Figure 12. When pulses are periodically produced from the terminal  $P_1$  of Figure 9 in the same manner as in the preceding embodiments, terminals  $t_0$ ,  $t_1$ ,  $t_2$  of Figure 14 assume a logic 1. Therefore, the outputs of the AND gate circuits 101, 103, 104 assume a logic 1 and the switching circuits 108, 111, 113 are turned ON. Therefore, the terminals  $C_0$ ,  $C_1$  produce pulses which are fed from the terminal 53c so that the display elements from 0 to 19 minutes are all turned ON. Furthermore, pulses applied to the terminal 53a are produced at the terminals  $C_3$  to  $C_6$  so that the display elements from 30 to 59 minutes are all turned OFF.

Furthermore, pulses applied to the terminal 53b are produced at the terminal  $C_2$ . Here, since the terminals  $s_0$  to  $s_2$  of Figure 13 assume a logic 1, and the terminals  $s_3$  to  $s_9$  assume a logic 0, the

AND gate circuits 83, 85, 86 produce a logic 1 such that the switching circuits 90, 93, 95 are turned ON. Consequently, the terminals  $e_0$ ,  $e_1$  produce pulses which are fed from the terminal 26a, the terminal  $e_2$  is alternately fed with pulses from the terminals 26a, 27a via the terminal 24a of Figure 9, and the terminals  $e_3$  to  $e_8$  produce pulses which are fed from the terminal 27a. Accordingly, the display elements of 20 and 21 minutes are turned ON and the display element of 22 minutes flashes.

Display of a preset time of 40 minutes will now be described. When pulses are generated from the terminal  $P_2$  of Figure 9, only the terminal  $s_0$  of Figure 13 and the terminal  $t_4$  of Figure 14 assume a logic 1. Therefore, the output of the AND gate circuit 82 of Figure 13 causes the switching circuit 89 to be turned ON whereby the terminal  $e_0$  produces the pulses applied to the terminal 24a and the terminal  $e_1$  to  $e_8$  produce pulses applied to the terminal 27a. Here, since pulses are generated from the terminal  $P_2$  of Figure 9, the terminal 24a produces pulses applied to the terminal 26a, the terminal  $C_4$  produces pulses applied to the terminal 53b and the other terminals produce pulses applied to the terminal 53a. Therefore, the display element of 40 minutes only is turned ON.

Referring to Figure 15 there is illustrated the display by a further embodiment of an electronic timer according to the present invention in which the display element 5c for displaying a preset time is turned ON, a display elements 5i between the display element corresponding to a remaining time to the graduation 9 are all turned ON, and a display element 9a flashes with a period of one second. This display can be produced relying upon the same circuit as in the preceding embodiments but so constructing the segment voltage supply circuit of Figure 13 that the terminals  $e_0$  to  $e_8$  produce the pulses applied to the terminals 26a, 27a of Figure 11 when the terminals  $s_0$  to  $s_8$  assume a logic 1 or logic 0.

Figures 16 and 17 illustrate a liquid crystal display device of a further embodiment of an electronic timer according to the present invention in which common electrodes and segment electrodes are further provided on the periphery of the electrodes shown in Figures 2 and 3. Namely, like Figure 2, Figure 16 has six fan-shaped or radially arranged inner common electrodes 115 and six outer common electrodes 116 with outwardly extending terminals  $x_0$  to  $x_5$ . With reference to Figure 17, sixty radially arranged inner segment electrodes 117 are formed in the same manner as those of Figure 3 to correspond to the common electrodes 115. On the radially outer ends of the segment electrodes 117 are located sixty respective outer segment electrodes 118 which face the outer common electrodes 116. The inner segment electrodes 117 and the outer segment electrodes 118 at predetermined positions are successively connected by lead electrodes 119 and are connected to ten terminals  $e_0$  to  $e_9$ .

As shown in Figure 18, a preset time is

displayed by turning ON an outer display element located at a position of 40 minutes, and remaining time is displayed by causing an inner display element located at a position of 23 minutes to flash.

The circuit for effecting this display can be constructed by simply adding a circuit for driving the outer common electrodes 116 to the circuit of Figure 5. The circuit for driving the outer common electrodes 116 may be constructed in the same manner as the circuit 25 of the Figure 5 for feeding a common voltage to the inner common electrodes 115. Namely, the remaining time is displayed by feeding the output of the decoder 21 to the common voltage supply circuit 25 responsive to pulses that are periodically generated at the terminal  $P_1$ , and the preset time is displayed by feeding the output of the decoder 21 to the outer common electrodes 116 responsive to pulses that are periodically generated at the terminal  $P_2$ .

In Figure 19, a preset time and a remaining time are displayed in a cumulative manner by the outer and inner display elements, and a display element 9a for displaying seconds flashes. In this case a decoder for the preset time and the remaining time should be such that each output produced in turn from the first output terminal of the decoder to an intermediate terminal before the last is held ON until the output of the last terminal is produced. The same circuit is used in the preceding embodiment where the display elements are turned ON in a cumulative manner may be used for the segment electrodes, inner common electrodes and outer common electrodes.

In Figure 20 the outer display elements are turned ON in a cumulative manner to display the preset time, and an inner display element corresponding to the remaining time flashes to display the remaining time.

In Figure 21, an inner display element corresponding to the preset time is turned ON to display the preset time, the outer display elements are turned ON in a cumulative manner to display the remaining time, and the display element 9a for displaying seconds is caused to flash.

In Figure 22, the outer and inner display elements corresponding to the preset time are turned ON to display the preset time, the inner display elements are turned ON in a cumulative manner to display a remaining time, and the display element 9a for displaying seconds is caused to flash.

The circuitry of the embodiments of the electronic timers according to the present invention for producing the displays of Figures 20 to 22 can be driven by suitably employing the circuitry of the preceding embodiments and are not illustrated here.

In Figure 23, an inner display element corresponding to a preset time is turned ON to display the preset time, the inner display elements are turned ON in a cumulative manner to display a remaining time, and the outer display elements

are cumulatively turned ON to display the remaining seconds. Figure 23 displays a preset time of 40 minutes and the remaining time of 23 minutes and 48 seconds.

5 Figures 24A and 24B illustrate circuits for effecting the display of Figure 23 in which reference numeral 120 denotes a pulse generator which successively produces pulses at the terminals  $P_1$ ,  $P_2$ ,  $P_3$  to display, in a time-divisional  
10 manner, remaining minutes and seconds and a preset time. Reference numerals 121, 122 denote respective counters for seconds and tens of seconds of the remaining time. Responsive to the pulses generated at the terminal  $P_1$ , the outputs of  
15 the counters 121, 122 pass through selection circuits 123, 124 and are fed to decoders 125, 126 for cumulative display.

Reference numerals 127, 128 denote OR gate circuits. The output of the selection circuit 123 is fed to a segment voltage supply circuit 130 via an  
20 output conversion circuit 129. The output of the decoder 126, on the other hand, passes through the OR gate circuit 128 and an AND gate circuit 131, and is fed to a common voltage supply circuit  
25 132 which is constructed in the same manner as that of Figure 14. Owing to the output of a common voltage supply circuit 132 and the output of the segment voltage supply circuit 130, the remaining seconds are displayed in a  
30 cumulative manner by the outer display elements as shown in Figure 23. Here, the same reference numerals as those used in the description of the preceding embodiments denote the same parts.

As the pulses are periodically generated from  
35 the terminal  $P_2$ , the outputs of the counters 133, 134 for remaining minutes are selected and fed to the decoders 125, 126 for cumulative display. The output of the decoder 126 is fed to the common voltage supply circuit 136 via the OR gate circuit  
40 128 and the AND gate circuit 135. Responsive to the output of the common voltage supply circuit 136 and the output of the segment voltage supply circuit 130, the inner display elements display the remaining minutes in a cumulative manner.

45 As pulses are produced from the terminal  $P_3$  of the pulse generator 120, the outputs of storage circuits 137, 138 pass through AND gate circuits 139, 140 and are fed to decoders 141, 142 which are constructed in the same manner as the  
50 decoders 20, 21 of Figure 5. The output of the decoder 142 is fed to the common voltage supply circuit 136 via the OR gate circuit 128, and the AND gate circuit 135. Therefore, responsive to the outputs of the segment voltage supply circuit 130,  
55 and the common voltage supply circuit 136, the inner display element corresponding to the preset time is turned ON.

The remaining seconds may be displayed by cumulatively turning ON the outer display  
60 elements while causing them to flash at a period of one second.

The embodiments of the present invention described above are such that preset time and remaining time are simultaneously displayed in an  
65 analog manner so it is easy to recognise at a

glance the preset time, the remaining time and the elapse of time. Furthermore, relations among these times can be discriminated at a glance without needing to produce a series of displays.  
70 Consequently, an electronic timer can be constructed relatively simply.

#### CLAIMS

1. An electronic timer comprising: a liquid crystal display device consisting of a plurality of circularly arranged spaced apart common electrodes, a plurality of radially arranged segment electrodes, and liquid crystal material disposed between the common electrodes and the segment electrodes to constitute a plurality of liquid crystal display elements arranged so as to simulate the hands of a mechanical timepiece when energised;  
75 a storage circuit for storing preset time data; a down-counter for receiving time-keeping data and, in operation, carrying out a down-count operation upon receipt of pulses of a predetermined period; and selection circuit means for selectively passing the output of the storage circuit and the output of the down-counter to a drive circuit which drives the display device.  
80

2. An electronic timer as claimed in claim 1 in which the common electrodes consist of a plurality of radially arranged inner electrodes and a plurality of radially arranged outer electrodes.  
85

3. An electronic timer as claimed in claims 1 or 2 including: a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a common voltage supplying circuit for driving the common electrodes; the selection circuit means being arranged to be controlled by the pulsiform signals for selectively passing the output of the storage circuit and the output of the down-counter to the segment voltage supplying circuit and the common voltage supplying circuit.  
90  
95  
100  
105

4. An electronic timer as claimed in any preceding claim including means for applying to said drive circuit a signal for causing a display element to indicate when time counting is complete.  
110

5. An electronic timer comprising: a liquid crystal display device consisting of a plurality of circularly arranged spaced apart common electrodes, a plurality of radially arranged segment electrodes, and liquid crystal material disposed between the common electrodes and the segment electrodes to constitute a plurality of liquid crystal display elements arranged so as to simulate the hands of a mechanical timepiece when energised;  
115 a storage circuit for storing preset time data; a down-counter for receiving timekeeping data and, in operation, carrying out the down-count operation upon receipt of pulses of a predetermined period; a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a common voltage supplying  
120  
125



are cumulatively turned ON to display the remaining seconds. Figure 23 displays a preset time of 40 minutes and the remaining time of 23 minutes and 48 seconds.

- 5 Figures 24A and 24B illustrate circuits for effecting the display of Figure 23 in which reference numeral 120 denotes a pulse generator which successively produces pulses at the terminals  $P_1$ ,  $P_2$ ,  $P_3$  to display, in a time-divisional manner, remaining minutes and seconds and a preset time. Reference numerals 121, 122 denote respective counters for seconds and tens of seconds of the remaining time. Responsive to the pulses generated at the terminal  $P_1$ , the outputs of the counters 121, 122 pass through selection circuits 123, 124 and are fed to decoders 125, 126 for cumulative display.

- Reference numerals 127, 128 denote OR gate circuits. The output of the selection circuit 123 is fed to a segment voltage supply circuit 130 via an output conversion circuit 129. The output of the decoder 126, on the other hand, passes through the OR gate circuit 128 and an AND gate circuit 131, and is fed to a common voltage supply circuit 132 which is constructed in the same manner as that of Figure 14. Owing to the output of a common voltage supply circuit 132 and the output of the segment voltage supply circuit 130, the remaining seconds are displayed in a cumulative manner by the outer display elements as shown in Figure 23. Here, the same reference numerals as those used in the description of the preceding embodiments denote the same parts.

- As the pulses are periodically generated from the terminal  $P_2$ , the outputs of the counters 133, 134 for remaining minutes are selected and fed to the decoders 125, 126 for cumulative display. The output of the decoder 126 is fed to the common voltage supply circuit 136 via the OR gate circuit 128 and the AND gate circuit 135. Responsive to the output of the common voltage supply circuit 136 and the output of the segment voltage supply circuit 130, the inner display elements display the remaining minutes in a cumulative manner.

- As pulses are produced from the terminal  $P_3$  of the pulse generator 120, the outputs of storage circuits 137, 138 pass through AND gate circuits 139, 140 and are fed to decoders 141, 142 which are constructed in the same manner as the decoders 20, 21 of Figure 5. The output of the decoder 142 is fed to the common voltage supply circuit 136 via the OR gate circuit 128, and the AND gate circuit 135. Therefore, responsive to the outputs of the segment voltage supply circuit 130, and the common voltage supply circuit 136, the inner display element corresponding to the preset time is turned ON.

- The remaining seconds may be displayed by cumulatively turning ON the outer display elements while causing them to flash at a period of one second.

- The embodiments of the present invention described above are such that preset time and remaining time are simultaneously displayed in an analog manner so it is easy to recognise at a

glance the preset time, the remaining time and the elapse of time. Furthermore, relations among these times can be discriminated at a glance without needing to produce a series of displays.

- 70 Consequently, an electronic timer can be constructed relatively simply.

#### CLAIMS

1. An electronic timer comprising: a liquid crystal display device consisting of a plurality of circularly arranged spaced apart common electrodes, a plurality of radially arranged segment electrodes, and liquid crystal material disposed between the common electrodes and the segment electrodes to constitute a plurality of liquid crystal display elements arranged so as to simulate the hands of a mechanical timepiece when energised; a storage circuit for storing preset time data; a down-counter for receiving time-keeping data and, in operation, carrying out a down-count operation upon receipt of pulses of a predetermined period; and selection circuit means for selectively passing the output of the storage circuit and the output of the down-counter to a drive circuit which drives the display device.

2. An electronic timer as claimed in claim 1 in which the common electrodes consist of a plurality of radially arranged inner electrodes and a plurality of radially arranged outer electrodes.

3. An electronic timer as claimed in claims 1 or 2 including: a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a common voltage supplying circuit for driving the common electrodes; the selection circuit means being arranged to be controlled by the pulsiform signals for selectively passing the output of the storage circuit and the output of the down-counter to the segment voltage supplying circuit and the common voltage supplying circuit.

4. An electronic timer as claimed in any preceding claim including means for applying to said drive circuit a signal for causing a display element to indicate when time counting is complete.

5. An electronic timer comprising: a liquid crystal display device consisting of a plurality of circularly arranged spaced apart common electrodes, a plurality of radially arranged segment electrodes, and liquid crystal material disposed between the common electrodes and the segment electrodes to constitute a plurality of liquid crystal display elements arranged so as to simulate the hands of a mechanical timepiece when energised; a storage circuit for storing preset time data; a down-counter for receiving timekeeping data and, in operation, carrying out the down-count operation upon receipt of pulses of a predetermined period; a pulse generator for producing at least two pulsiform signals having different waveforms from one another; a segment voltage supplying circuit for driving the segment electrodes; and a common voltage supplying



36

circuit for driving the common electrodes; and  
selection circuit means arranged to be controlled  
by said pulsiform signals for selectively passing  
the output of the storage circuit and the output of  
5 the down-counter to the segment voltage

supplying circuit and the common voltage  
supplying circuit.

6. An electronic timer substantially as herein  
described with reference to and as shown in the  
10 accompanying drawings.