

Claims

1. An event-driven spiking convolutional neural network (1), comprising a plurality of layers, wherein each layer comprises
 - a kernel module (110) configured to store and to process in an event-driven fashion kernel values of at least one convolution kernel (410);
 - a neuron module (120) configured to store and to update in an event-driven fashion neuron states of neurons of the spiking convolutional neural network (1), and to output spike events (150) generated from updated neurons (420);
 - a memory mapper (130) configured to determine neurons (420) to which an incoming spike event (140) from a source layer projects - by means of a convolution with at least one convolution kernel (410) and wherein neuron states of said determined neurons (420) are to be updated with applicable kernel values of the at least one convolution kernel (410), wherein the memory mapper (130) is configured to process incoming spike events in an event-driven fashion.

2. The event-driven spiking convolutional neural network according to claim 1, wherein the kernel module (110) comprises a kernel interface (111) connected to an associated kernel memory (112), wherein the associated kernel memory (112) is configured to store the kernel values of the at least one convolution kernel (110) in kernel addresses, wherein the kernel module (110) is electronically connected to the neuron module (120).

3. The event-driven spiking convolutional neural network according to claims 1 and 2, wherein the memory mapper (130) is electronically connected to the kernel module (110), wherein the memory mapper (110) is configured and arranged

a) to receive the incoming spike event (140) from a source layer of the spiking convolutional neural network (1), the incoming spike event (140) comprising information on a neuron coordinate (421) in the source layer;

and in response to the received spike event (140),

b) to determine neuron coordinates (422) and corresponding neuron addresses of the neurons (420) to which a convolution of the received spike event (140) with the at least one convolution kernel (110) projects,

c) to determine kernel coordinates (411) with corresponding kernel addresses of the kernel values applicable to the neuron states of the determined neuron addresses, wherein the neuron states of the determined neuron addresses are to be updated with the applicable kernel values,

d) to provide the determined neuron addresses to the kernel module.

4. The event-driven spiking convolutional neural network according to claim 3, wherein the kernel module (110) is configured and arranged to receive the determined kernel addresses and to provide the applicable kernel values stored at the determined kernel addresses, to the neuron module (120).

5. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein the neuron module (120) is configured and arranged

a) to receive the determined neuron addresses (142n) and the applicable kernel values (142k),

b) to determine for each received neuron address (142n) an updated neuron state for the neuron (420) based on the applicable kernel value (142k),

c) to output an outgoing spike event (150) for updated neurons (420) reaching at least one predefined threshold value (502).

6. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein the memory mapper (130) is configured to determine for each received spike event (140) at least one output feature map (430) consisting of neurons assigned to the output feature map (430), wherein the number of output feature maps (430) is equal to the number of convolution kernels (410) of the current layer (10).
7. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein each layer (10, 10') further comprises a bias module (160) comprising an associated bias memory (162) and a bias interface (161) connected to the associated bias memory (162), wherein the associated bias memory (162) is configured to store bias values in bias addresses, wherein the bias module (160) is connected to the neuron module (120) and wherein the bias module (160) is configured to provide predefined time-intervals bias values to the neuron module (120), wherein the neuron module (120) is configured to update the neuron states of all neurons (431) in at least one output feature map (430) based on the received bias values.
8. The event-driven spiking convolutional neural network according to one of the preceding claims, wherein the neuron module (120) comprises a plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process received neuron addresses (142n) and kernel values (142k), and received bias values (142b) and to generate (501, 502) updated neuron states and spike events (150), wherein each neuron sub-interface (121s) has an associated neuron memory (506) for reading the neuron state for the received neuron address and to write the updated neuron state to the received neuron address in the associated neuron memory (506), such that a parallel processing of neuron

state is achieved by the neuron sub-interfaces and their associated neuron memories (506).

9. The event-driven spiking convolutional neural network according to claim 8, wherein the neuron module (120) comprises a router module (601) configured and adapted to receive determined neuron addresses (142n) and kernel values (142k), and bias values (142b) from the kernel module (110) and/or the bias module (160), and to transmit the received neuron addresses (142n) and the kernel values (142k), and the bias values (142b) to the plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process the received neuron addresses (142n) and kernel value (142k), and the bias values (142b) in parallel.
10. The event-driven spiking convolutional neural network according to claim 8, wherein the neuron module further comprises a merger module (602) configured and adapted to receive generated spike events (150) from the plurality of neuron sub-interfaces (121s) and funnel the spike events for serial processing in a bus having less channels than neuron sub-interfaces, wherein the bus has a single transmission channel only.
11. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein the neuron module (120) is configured
 - to receive a neuron address (142n) and a kernel value (142k), and a bias value (142b) from the kernel module (110) and/or the bias module (160) at the router module,
 - to read (500) a neuron state of the received neuron address (142n) from the associated neuron memory (506) on one of the neuron sub-interfaces (121s)

- to update (501) the read neuron state with the received kernel value (142k) and/or with the received bias value (142b) on the neuron sub-interface (121s),
 - to compare the updated neuron state with at least one threshold value (502) stored in and accessible from a threshold register (504) on the neuron sub-interface (121s),
 - upon reaching the at least one threshold value (502), to generate a spike event (503) that is provided to a destination mapper (170), and to reset the updated neuron state to a reset neuron state,
 - to write (505) the updated neuron state to the received neuron address (142n) of the associated neuron memory (506).
12. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein the memory mapper (130) is configured to execute the following sequence of operations in order to determine the kernel addresses of the applicable kernel values (142k) and the neuron coordinates (421) with the corresponding neuron addresses (142n) to be updated, when a spike event (140) is received by the memory mapper (130), the spike event (140) comprising or consisting of an information about a coordinate (x,y) of a neuron (421) having generated the spike event (140) in a source feature map (440), and a channel identifier (c), the coordinate (x,y) comprising an x-identifier and y-identifier:
- zero padding ($x+p_x$, $y+p_y$) the coordinate (x,y) of the spike event (140) with a predefined offset (p_x , p_y) provided by and stored in a register,
 - from the coordinate (x,y), from the zero-padded coordinate ($x+p_x$, $y+p_y$), computing a neuron anchor coordinate (x_0 , y_0) to which the spike event projects, and a corresponding kernel anchor coordinate (x_0^k , y_0^k) of the at least one kernel (f), wherein the kernel anchor coordinate (x_0^k , y_0^k) is indicative of a kernel coordinate (f, x_0^k , y_0^k) for each of the at least one kernel (f), wherein the neuron anchor coordinate (x_0 , y_0) is associated to an output feature map (430),

- starting from the neuron anchor coordinate and the kernel anchor coordinate, determining all neuron coordinates (f, x, y) that are to be updated and all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values (142k) by processing information on an output feature map (430) size, a stride size and/or a kernel size that are provided by a register,
 - determining from the determined all neuron coordinates (f, x, y) and the all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values (142k) compressed neuron addresses and compressed kernel addresses,
 - providing the determined compressed neuron addresses and compressed kernel addresses to the kernel module (110) and/or the neuron module (120).
13. The event-driven spiking convolutional neural network according to claim 8, wherein the associated neuron memory (506) is organized such that all neuron states are stored in consecutive neuron addresses, wherein the memory mapper (130) is configured to generate for all neuron coordinates (f, x, y) in the consecutive neuron addresses such as to generate compressed neuron addresses and wherein the memory mapper (130) is configured to provide the compressed neuron addresses to the neuron module (120).
14. The event-driven spiking convolutional neural network according to any one of the preceding claims, wherein the event-driven spiking convolutional network (1) comprises a plurality of layers (10, 10', 10'') that are connected with a spike event router (200) that is configured to route an outgoing spike event received from a source layer to at least one destination layer, wherein the router (200) accesses the destination information associated to the outgoing spike event (150), wherein the destination layer (10'') can be the source layer (10').

15. A memory mapper (130) equipment for an event-driven spiking convolutional neural network configured to determine kernel addresses and neuron addresses (142n) to be updated in an event-driven fashion when a spike event (140) is received by the memory mapper (130), wherein the spike event (140) comprising or consisting of an information about a coordinate (x,y) and a channel identifier (c) of the spike event (140), the coordinate comprising an x-identifier and y-identifier, wherein when a spike event (140) is received by the memory mapper (130), the memory mapper (130) executes the following sequence of operations:
- zero padding (300) $(x+p_x, y+p_y)$ the coordinate (x,y) of the spike event (140) with a predefined offset (p_x, p_y) provided by and stored in a register (300r),
 - from the coordinate (x,y) , computing (301) a neuron anchor coordinate (x_o, y_o) to which the spike event projects, and a corresponding kernel anchor coordinate (x_o^k, y_o^k) of the at least one kernel $(410, f)$, wherein the kernel anchor coordinate (x_o^k, y_o^k) is indicative of a kernel coordinate (f, x_o^k, y_o^k) for each of the at least one kernel $(410, f)$, wherein the neuron anchor coordinate is associated to an output feature map (430),
 - starting (302) from the neuron anchor coordinate and the kernel anchor coordinate, determining all neuron coordinates (f, x, y) that are to be updated and all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values by processing information on an output feature map size, a stride size and/or a kernel size that are provided by a register,
 - determining (303) from the determined all neuron coordinates (f, x, y) and the all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values compressed neuron addresses and compressed kernel addresses,
 - providing the determined compressed neuron addresses and compressed kernel addresses to a kernel module (110) and/or a neuron module (120) for processing the compressed neuron addresses and compressed kernel addresses.

16. An electronic circuit, comprising a plurality of layers (10,10',10''), wherein at least one (10) of the layers comprises:
 - a memory mapper (130) which is configured to receive an incoming spike event (140) and to determine the neurons (420) to which the incoming spike event projects;
 - a kernel module (110) which is configured to provide applicable kernel values of at least one convolution kernel (410);
 - a neuron module (120) which is configured to update the neuron states of the determined neurons (420) with the applicable kernel values.
17. The electronic circuit according to claim 16, wherein the memory mapper (130) is also configured to execute a formula that computes the neuron addresses to be updated and the kernel addresses for the applicable kernel values;
 - the neuron addresses and the kernel addresses determined by the memory mapper (130) are provided to the kernel module (110).
18. The electronic circuit according to claims 16-17, wherein the applicable kernel values are sent to the neuron module (120) where the neuron states of the determined neurons (420) are updated with the applicable kernel values.
19. The electronic circuit according to claims 16-17, wherein the neuron addresses (142n) for the determined neurons (420) are provided by kernel interface (111) of the kernel module (110) in an output data set comprising said neuron addresses (142n) associated to the applicable kernel values (142k).

20. The electronic circuit according to claims 16-17, wherein the neuron module (120) receives bias values (142b) from bias module (160).
21. The electronic circuit according to claim 20, wherein the neuron states of the determined neurons (420) are to be updated with the applicable kernel values (142k) and/or the bias values (142b).
22. The electronic circuit according to claims 16-17 or 21, wherein the memory mapper (130) is configured to provide compressed neuron addresses to the neuron module (120);
the memory mapper (130) is configured to provide compressed kernel addresses to the kernel module (110).
23. The electronic circuit according to claims 16-17 or 21, wherein the spike event (140) received by the memory mapper (130) comprises or consists of an information about a coordinate (x, y) and a channel identifier (c) .
24. The electronic circuit according to claim 23, wherein the memory mapper (130) is configured to zero pad $(x+p_x, y+p_y)$ the coordinate (x, y) of the spike event with a predefined offset (p_x, p_y) provided by and stored in a register (300r).
25. The electronic circuit according to claims 16-17 or 21 or 24, wherein the memory mapper (130) is configured to compute the neuron anchor coordinate (x_o, y_o) to which the spike event (140) projects from the coordinate (x, y) or from the zero-padded coordinate $(x+p_x, y+p_y)$ and to compute the corresponding kernel anchor coordinate (x_o^k, y_o^k) of at least one kernel (410, f), wherein the kernel anchor coordinate (x_o^k, y_o^k) is indicative of a kernel coordinate (f, x_o^k, y_o^k) for each of the

at least one kernel (410, f) and to determine all neuron coordinates that are to be updated and all kernel coordinates of the applicable kernel values starting from the neuron anchor coordinate and the kernel anchor coordinate.

26. The electronic circuit according to claims 25, wherein the neuron anchor coordinate is the coordinate of the neuron located at a corner of a projection window to which the spike event (140) projects in output feature map; the neuron anchor coordinate serves the purpose of defining a starting point in the output feature map for convolution;

the kernel anchor coordinate is the coordinate of the kernel value that is located in a corner or close to a corner of the kernel (410);

the kernel anchor coordinate serves the purpose of defining a starting point for determining all the applicable kernel values.

27. The electronic circuit according to claims 16 or 17 or 21 or 24 or 26, wherein the neuron module (120) comprises a router module (601) configured and adapted to receive the neuron addresses (142n) for the determined neurons (420) and the applicable kernel values (142k) from the kernel module (110), and

to transmit the received the neuron addresses (142n) for the determined neurons (420) and the applicable kernel values (142k) to the plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process the received the neuron addresses (142n) for the determined neurons (420) and the applicable kernel values (142k) in parallel, and

to receive the bias values (142b) from the bias module (160), and to transmit the received the bias values (142b) to the plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process the bias values (142b) in parallel.

28. The electronic circuit according to claim 27, when a neuron sub-interface receives a neuron address from the neuron addresses (142n) for the determined neurons (420) and an applicable kernel value from the applicable kernel values (142k), the neuron sub-interface (121s) reads the neuron state that is stored under the received neuron address from associated neuron memory (506); and then,
- the applicable kernel value is added to the neuron state to get resulting neuron state.
29. The electronic circuit according to claims 28, wherein the resulting neuron state is then compared to at least one threshold value (502) to generate an outgoing spike event (150) when the resulting neuron state exceeds one of the thresholds; and then,
- the neuron state is reset to a reset neuron state.
30. The electronic circuit according to claim 29, the at least one (10) of the layers also comprises:
- a destination mapper (170) which is configured and arranged to append the information of the outgoing spike event (150) such that it can be routed to the destination layer.