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(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(71) We, TOKYO SHIBAURA ELECTRIC COMPANY LIMITED, a Japanese company of 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawaken, Japan do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

This invention relates to semiconductor integrated circuits ("I. C. circuits"), and in particular to a Complementary Metal Oxide Semiconductor (hereinafter referred to as CMOS).

Various CMOS circuits have been known in the past, a typical example being a CMOS inverter circuit. That inverter circuit is made up of a P channel-type MOS field effect transistor Q_1 (see Figure 1 of the accompanying drawings) and an N channel-type MOS field effect transistor Q_2; the source electrodes of the transistors Q_1 and Q_2 are connected respectively to a high bias voltage supply source V_{DD}, and to a low bias voltage supply source V_{SS}; the drain electrodes of the transistors Q_1 and Q_2 are connected together to an output terminal OUT, while the gate electrodes are both connected to an input terminal IN.

In a CMOS circuit as described, the threshold voltages V_{th} of the N and P channel MOS transistors have opposite polarities, and therefore their responses to input voltages are entirely opposite; consequently, as is well known, the operating power is extremely small. For example, where the source V_{DD} is made +5V and the source V_{SS} is made earth (GND), and if +5V is supplied to the input IN, then transistor Q_2 conducts and transistor Q_1 is not conductive and no direct current at all flows between the two power sources. Conversely, if zero voltage is applied to the input IN, transistor Q_2 becomes non-conductive and transistor Q_1 becomes conductive, so that, again, no direct current flows between the power sources. Therefore, in a CMOS circuit there is ideally no operating power consumption; during the input information pulse transition time period, transistors Q_1 and Q_2 both conduct resulting in an instantaneous flow of transition current, when there is flow of leakage current at the P N junctions and current due to the charge and discharge of the load capacity at the output. In general, therefore, the power consumption of a CMOS circuit is extremely small.

However, when noise in impulse form appears at the output or at the input of a CMOS circuit, a large direct current (several tens mA to several hundred mA) flows between the power sources V_{DD} and V_{SS} due to the triggering of parasitic transistors in the CMOS I.C.; even when the applied noise disappears, the large current between the sources continues. That phenomenon (hereinafter referred to as "Latch-up") substantially increases the power consumption and may result in the CMOS circuit having low reliability. Latch-up may occur whether the polarity of the noise impulse is positive or negative; in order to eliminate the phenomenon, it has been necessary to lower the voltage of the power source V_{DD} to below a given value, or to isolate the power sources.

A first aspect of the invention resides in a semiconductor integrated circuit comprising a CMOS circuit having an input part, an output part, means for connecting an external, relatively positive, bias voltage source, and means for connecting an external, relatively

negative, bias voltage source, the structure of the CMOS circuit being such that parasitic transistors are formed therein; first bypass circuit means connected between the relatively positive bias voltage connecting means and the output part of the CMOS circuit for bypassing noise supplied to the output at a first level more positive than the relatively positive bias voltage; and second bypass circuit means connected between the relatively negative bias voltage source connecting means and the output part for bypassing noise supplied to the output part at a second level more negative than the relatively negative bias voltage; the first and second bypass circuit means satisfying the following conditions:

(1) when positive noise is supplied to the output part, $Z_1 < Z_3$; and

(2) when negative noise is supplied to the output part, $Z_2 < Z_4$,

Z_1 is the internal impedance of the first bypass circuit means when positive noise is supplied to the output part,

Z_2 is the internal impedance of the second bypass circuit means when negative noise is supplied to the output part, and

Z_3 and Z_4 are the output impedances of the CMOS circuit when positive noise and negative noise are supplied to the output part respectively in the absence of the first and second bypass circuit means, whereby impulse noise capable of triggering the parasitic transistors is absorbed. By having the noise absorbing bypassing circuits, the danger of latch-up occurring is largely eliminated.

A second aspect of the invention provides a semiconductor integrated circuit comprising a CMOS circuit having an input part, an output part, means for connecting an external, relatively positive, bias voltage source, and means for connecting an external, relatively negative, bias voltage source, the structure of the CMOS circuit being such that parasitic transistors are formed therein; a plurality of protective diodes connected to the input part for preventing gate breakdown at the input part; first bypass circuit means connected between the relatively positive bias voltage connecting means and the input part of the CMOS circuit for bypassing noise supplied to the input part at a first level more positive than the relatively positive bias voltage; and second bypass circuit means connected between the relatively negative bias voltage source connecting means and the input part for bypassing noise supplied to the input part at a second level more negative than the relatively low bias voltage; the first and second bypass circuit means satisfying the following conditions:

(1) when positive noise is supplied to the input part, $Z_1 < Z_3$; and

(2) when negative noise is supplied to the input part, $Z_2 < Z_4$.

where

Z_1 is the internal impedance of the first bypass circuit means when positive noise is supplied to the input part,

Z_2 is the internal impedance of the second bypass circuit means when negative noise is supplied to the input part, and

Z_3 and Z_4 are the input impedances of the CMOS circuit when positive noise and negative noise are supplied to the input part respectively in the absence of the first and second bypass circuit means, whereby impulse noise capable of triggering the parasitic transistors is absorbed.

The invention will be more readily understood by way of example from the following description of CMOS circuits in accordance therewith, reference being made to the accompanying drawings, in which:-

Figure 1 is a circuit diagram of a known CMOS inverter;-

Figure 2 shows in section a CMOS inverter and illustrates the parasitic bipolar transistors that are formed;

Figure 3 is an equivalent circuit diagram of the parasitic transistor circuit of the CMOS inverter of Figure 2;

Figure 4 is a circuit illustrating the use of noise absorption circuits on the output of a CMOS inverter, while *Figure 5* is a similar circuit with the noise absorption circuit connected to the input;

Figure 6 is a sectional view showing the protective diodes of Figure 5 formed in the CMOS inverter I.C.;

Figure 7 shows an alternative form of noise absorption circuit, while *Figure 8* illustrates the operation of the circuit of Figure 7;

Figure 9 is a section through a CMOS inverter I.C.; and

Figures 10 to *16* illustrate other forms of noise protection circuits.

Figure 1 shows a CMOS inverter circuit, while Figure 2 shows in section a semiconductor wafer forming that circuit. In the example illustrated, a P-well 2 having a P-type impurity in a concentration of about 2×10^{16} atoms/cm^3 is formed in an N-type substrate 1 having a concentration of about 1×10^{15} atoms/cm^3. In the N-type substrate, but outside the P-well 2, P-type regions 3 and 4 are formed by diffusion with a concentration of for instance about

10^{19} atoms/cm^3; the P-type regions 3 and 4 with the N-type substrate 1 form a P channel MOS transistor (Q_1 in Figure 1). Similarly, with the P-well 2, there are N-type regions 5 and 6, which form an N channel MOS transistor (Q_2 in Figure 1), and which are created by diffusion of about 10^{20} atoms/cm^3 of an N-type impurity.

A P-type guard band 7 is formed in the P-well 2 about the regions 5 and 6. A silicon oxide film about 1500 Å thick is deposited to form the gates 8 and 9 of the MOS transistors. Apertures are made where required, and conducting films, such as aluminium, are applied to form the conductors. For the CMOS inverter circuit illustrated, source region 4 and source region 5 are connected respectively to high bias voltage supply source V_{DD} and low bias voltage supply source V_{SS} (GND), gates 8, 9 are connected together to imput terminal N (Figure 1), and drain regions 3 and 6 are commoned and connected to the output terminal OUT of the resulting CMOS inverter circuit. 10 and 11 are respectively a N+ ohmic region connected to V_{DD} to fix the N-type substrate 1 at V_{DD} potential and a P+ ohmic region connected to V_{SS} to fix the P-well 2 at V_{SS} potential.

The known CMOS I.C. shown in Figures 1 and 2 has parasitic bipolar transistors which are indicated in Figure 2 at Tr_1 - Tr_4, and which have thyristor characteristics. The circuits of the parasitic transistors can be triggered by externally applied impulses, resulting in an avalanche action causing substantial current flow between the power sources and the danger of thermal breakdown of the I.C. Thus, parasitic bipolar transistors Tr_2 and Tr_4 are formed in P-well 2 in the direction of the thickness of substrate 1, while parasitic transistors Tr_1 and Tr_3 are formed in substrate 1 outside P-well 2 in the direction at right angles to the thickness. In addition, resistances $R_{P\text{-well}}$, $R_{N\text{-sub }1}$ and $R_{N\text{-sub }2}$ are present in the P-well 2 and substrate 1.

Figure 3 shows the equivalent circuit of the parasitic transistors circuits. When positive impulse noise I_{in} is applied to output terminal OUT, a current $\alpha_3 \times I_{in}$ flows in the chain-dotted path 12 of Figure 3, bypassing the $R_{P\text{-well}}$ region; when the voltage drop becomes V_{BE2}, a current I_{b2} flows in the base of transistor Tr_2:

$$I_{b2} \simeq \alpha_3 I_{in} \qquad (R_{P\text{-well}} >> r_{be2}) \qquad \ldots(1)$$

The collector current I_{c2} of transistor Trd22 is then

$$I_{c2} = \beta_2 I_{b2} = \beta_2 \alpha_3 I_{in} \qquad \ldots(2)$$

Here α_1, α_2, α_3 and α_4 are the common base current gains of transistors Tr_1, Tr_2, Tr_3 and Tr_4;

$$\beta_1 = \frac{\alpha_1}{1-\alpha_1} \quad \text{and} \quad \beta_2 = \frac{\alpha_2}{1-\alpha_2}$$

are the common emitter current gains of transistors Tr_1 and Tr_2; and r_{be1} and r_{be2} are the effective dynamic resistance between base and emitter of transistors Tr_1 and Tr_2.

Similarly, when I_{c2} has become the drive current and the voltage drop across resistance $R_{N\text{-sub }2}$ has become V_{BE1}, the base current I_{b1} of transistor Tr_1 flows and that transistor conducts:

$$I_{b1} = I_{c2} \qquad \ldots(3)$$

($R_{N\text{-sub }2}$ is greater than or approximately equal to $+_{be1}$)

$$I_{c1} = \beta_1 I_{b1} = \beta_1 \beta_2 \alpha_3 I_{in} \qquad \ldots(4)$$

Current thus flows from V_{DD} through transistors Tr_1 and Tr_2 to ground. Even if the externally applied noise is cut off, that current will continue to flow, provided that the condition

$$I_{b2} \leqslant I_{c1} \qquad \ldots(5)$$

is satisfied. In other words, if

$$\alpha_3 I_{in} \leqslant \beta_1 \beta_2 \alpha_3 I_{in} \text{ or}$$
$$1 < \beta_1 \beta_2 \qquad \ldots(6)$$

occur, the base current I_{b2} of transistor Tr_2 increases in each cycle. The current increase does not continue indefinitely; because of the dependency of β on the current, as the current increases a limit β max will be reached at which β will begin to decrease, and in the steady state it appears that the abnormal current will settle down where the following two conditions are satisfied simultaneously:

$$I_{b2(n-1)} = I_{b2}(n); \qquad \beta_{1(n)} \cdot \beta_{2(n)} \geqslant 1.$$

Here $I_{b2(n)}$, the base current is the nth cycle, is the current at which stability is maintained, stability occurring in the nth cycle.

The dimensional size of the transistors is not the main factor controlling the occurrence of the latch-up phenomenon. However, when current gain is measured against the dimensional size, or more precisely the drain surface area, of the transistors, there is a correlation between the value at which the abnormal current converges and the dimensional size; when the transistors have large drain surface areas, the abnormal current is greater than when those areas are small.

Where negative noise is applied to the output terminal OUT, the current flow 13 is along the path indicated by the chain line 13 in Figure 3. As in the case of positive noise,

$$I_{b1} \simeq \alpha_4 I_{in} \quad ...(7)$$

($R_{N\text{-sub }2}$ is greater than or approximately equal to 042_{bc1})

$$I_{c1} = \beta_1 I_{b1} = \beta_1 \alpha_4 I_{in}$$

$$I_{b2} = I_{c1} \ (R_{P\text{-well}} >> r_{bc2})$$

$$I_{c2} = \beta_2 I_{b2} = \beta_1 \beta_2 \alpha_4 I_{in}$$

and the condition for the maintenance of the current of the system becomes

$$I_{b1} \leqslant I_{c2} \text{ or } 1 \leqslant \beta_1 \beta_2 \quad ...(8)$$

Thus, the same conditions for latch-up apply for negative noise as for positive noise.

Figure 4 shows a CMOS circuit with noise absorption circuits for eliminating the latch-up phenomenon, the CMOS circuit being shown in the same form as Figure 1. Here, to prevent noise liable to trigger the parasitic transistor circuit from passing from the OUT terminal to the I.C., a protective or bypass circuit is connected between the OUT terminal and the power sources. Thus, Figure 4 shows a bypass circuit 21, consisting of a transistor or its equivalent, connected between the OUT terminal and power source V_{DD}, and a similar bypass circuit 22 connected between the OUT terminal and power source V_{SS} (in this case earth). Z_1 is the internal impedance of circuit 21 when positive noise is applied to the OUT terminal, while Z_2 is the corresponding impedance of circuit 22 when negative noise is applied. Z_3 is the output impedance of the CMOS circuit when a positive noise is applied to the same OUT terminal when circuits 21 and 22 are not present and is approximately equal to the "on" resistance of the equivalent parasitic diode D_3. Z_4 is the similar output impedance of the CMOS circuit when negative noise is applied to the OUT terminal in the same circumstances and is approximately equal to the "on" resistance of parasitic diode D_4. Diodes D_3 and D_4 are parasitically formed, respectively by the P+ region 3 and the substrate 1, and by the P-well $_2$ and N+ region 6.

The necessary conditions for the bypass circuits 21, 22, for them to be effective in protecting the CMOS device from applied noise are:

when positive noise is applied to the output part OUT : $Z_1 < Z_3$

when negative noise is applied to the output part OUT : $Z_2 < Z_4$.

If noise having a level higher than the voltage of V_{DD} is applied to the output terminal OUT, that noise is bypassed to the source V_{DD} through the impedance Z_1 of circuit 21, while if negative noise having a level lower than the voltage of source V_{SS} (in this case earth) is applied to terminal OUT, that noise is similarly bypassed to earth through impedance Z_2 of circuit 22. In other words, the circuits 21, 22 perform the function of keeping noise applied to the CMOS below the voltage V_{La} necessary to trigger the conduction of the abnormal current by the parasitic transistors. Accordingly, latch-up is prevented.

At the input of the CMOS circuit, it is possible to have diodes D_5 and D_6 (Figure 5) connected respectively to the supply sources V_{DD} and V_{SS}, in order to eliminate the danger of gate break-down. Those diodes D_5 and D_6 are shown in Figure 6 as formed by the N region 10 and a P type diffusion region 14 in substrate 1 and by the region 11 and an N type diffusion region 17 in the P-well 2. The diodes D_5, D_6 form parasitic bipolar transistors Tr'_3 and Tr'_4 as shown in Figure 6 and those transistors correspond in function to the parasitic bipolar transistors Tr_3 and Tr_4 of Figure 3 and therefore give rise to latch-up. To prevent latch-up, bypass circuits 23 and 24, which are similar to the circuits 21, 22 of Figure 4, are connected to the terminal IN, as shown in Figure 5, in order to prevent noise on the input IN causing abnormal current to flow between the voltage sources.

Reverting to the noise absorption circuits connected to the OUT terminal (Figure 4), the circuits 21, 22 can take the form of low break-down voltage diodes D_1, D_2 (Figure 7). The reverse direction characteristics of the parasitic diodes D_3 and D_4 are about 40V, as shown in Figure 8, but the breakdown voltage of diodes D_1 and D_2 is substantially less, as shown in the same figure. Consequently, diodes D_1 and D_2 conduct noise applied to terminal OUT to the voltage sources and the noise passing to the I.C. is prevented from reaching a level liable to cause parasitic transistor conduction and latch-up.

The break-down voltage of parasitic diodes D_3 and D_4 can be lowered to eliminate the need for diodes D_1 and D_2. As shown in Figure 9, a P region 25 is formed in P-well 2 adjacent N region 6, and a N region 26 is formed adjacent the P region 3 in the substrate 1 outside the P-well 2. Regions 3 and 26 thus form the diode D_3 while regions 6 and 25 form the diode D_4, the regions 25 and 26 being connected respectively to the supply terminals V_{SS} and V_{DD}. There are various methods of forming the regions 25, 26, such as ion injection, simultaneous diffusion and self-matching type diffusion; the important thing is that the P N junctions of the diffusion regions 6 and 25 and the P N junctions of the diffusion regions 3 and 26 are each regions of high concentration, the break-down voltages of those junctions being determined by the regions in question. For example, if as described previously boron in a concentration of about 10^{19} atoms/cm^3 is diffused into the diffusion regions 3 and 25, and phosphorus in a concentration of about 10^{20} atoms/cm^3 is diffused into

the diffusion regions 6 and 26, the break-down voltages of the diodes D_3, D_4 will be about 4V.

Alternatively, as shown in Figure 10, the diodes D_1, D_2 may be retained and formed in the CMOS I.C. separately from the MOS transistor regions 3, 4 and 5, 6. In Figure 10, diode D_1 is formed by P and N regions 27, 28 respectively connected to the terminals OUT and V_{DD}, and diode D_2 is formed by the P region 11 and an N region 31 within the P-well 2, and connected respectively to the terminals V_{SS} and OUT. P and N regions 33 and 34 then form guards for the two MOS transistors. In order to vary the break-down voltages of the diodes D_1 and D_2, the P N junctions 27, 28 and 11, 31 may be coupled by P- (N-) layers 35 and 36 respectively, as shown in Figure 13. It is then possible to vary the break-down voltages by control of the ion concentration of the layers 35, 36, and thereby improve the effectiveness of the diodes D_1, D_2. The same technique of using P- (N-) layers can be applied to the I.C. arrangement of Figure 9.

Reverting to Figures 7 and 8, if noise above the break-down voltage of diode D_1, e.g. noise of -6V, is applied to the output terminal OUT, the diode D_1 conducts on, because a reverse bias of 9V is applied, the voltage of terminal V_{DD} being 3V. Current then flows along the path V_{DD} - D_1 - OUT to the noise source, and a voltage above the break-down voltage of the diode D_1 is prevented from being supplied to the emitters of the parasitic transistors Tr_3 and Tr_4. As a consequence, the emitter of transistors Tr_3 is at -1V, the break-down voltage of diode D_1 being about 4V, and if the values of the resistance $R_{P\text{-well}}$ is made large so that Tr_3 does not conduct and the current gain of the vertical parasitic transistor is made small, as by making the depth of the P-well 2 large, or the like, then Tr_3 is maintained off and latch-up does not occur. The resistance of P-well 2 is often formed with a concentration of about 2×10^{16} atoms/cm^3 so that the sheet resistance of the I.C. is large, i.e. several kΩ/aperture, and the depth of the P-well is large, about 8μ to 12μ; consequently, the current amplification rates of the vertical transistors Tr_2 and Tr_4 are not very great, e.g. several dozen, and the transistors do not conduct when a voltage of several volts is applied.

Similarly, if noise above the break down voltage of diode D_2, e.g. noise of above +6V, is applied, diode D_2 conducts because the reverse bias is 6V and current flows from the noise source along the path OUT - D_2 - V_{SS}. The voltage applied to the emitters of transistors Tr_3 and Tr_4 cannot therefore exceed the yield voltage of diode D_2 and the emitter of transistor Tr_4 is at +4V and, if the values of the resistances of N -Sub are made sufficiently large so that the Tr_4 is not conductive, and if the current amplification rate of the lateral transistor Tr_4 is made small (for instance by making the distance between the regions 3 and the P-well 2 large), then when transistor Tr_4 is off, latch-up does not occur. The current amplification of the lateral transistors is naturally small, often for instance about 0.01 and therefore those transistors are not put on by noise of several volts.

In the above analysis, consideration has been given to noise above the break-down voltages of the diodes D_1, D_2 with reference to their break-down characteristics. Noise is also absorbed by the forward direction characteristics of diodes D_1 and D_2. In that respect, the parasitic diodes D_3 and D_4 of the MOS transistors do not absorb that noise, due to the fact that the sheet resistance of the I.C. is great. Even if the noise were absorbed by diodes D_3, D_4 the current through those diodes would become the base emitter current of the transistors Tr_3 and Tr_4 and latch-up would not be prevented. For that reason, diodes D_1 and D_2 are selected to absorb noise of relatively small level in the forward direction to ensure prevention of latch-up. As a result, the action of the parasitic transistors is completely prevented, without increasing substantially the production process stages of the CMOS.

It is necessary to select the break-down voltages of the diodes D_1 and D_2 according to the power source V_{DD} and V_{SS} that are employed. For example if the voltage of those sources are respectively +15V and OV, diodes having a break-down voltage of not less than 15V are necessary. If noise also appears at other terminals of the CMOS device, they may be similarly provided with absorption circuits. Thus, low breakage voltage diodes may be connected between the power source terminals V_{DD} and V_{SS}, between the input terminal IN and either or both of the power source terminals, or connected to any other terminal where noise is likely to arise.

As shown in Figure 12, a resistance R_0 may be interposed in the noise supply path between the output terminal OUT and the MOS transistors of the CMOS I.C. If noise above the break-down voltage of the low voltage break-down diodes D_1, D_2 is applied to terminal OUT, the resistance R_0 causes the voltage of the noise reaching the parasitic transistor circuit to be reduced, or the noise current to be limited, so that the occurrence of latch-up is kept to a minimum and the effectiveness of diodes D_1, D_2 is increased. Figure 11 is a section through the I.C. corresponding to the circuit of Figure 12. It is similar to Figure 13, except that each of the regions 27, 31 has two spaced conductor connections and incorporate resistances indicated at R_{01} and R_{02}. It will thus be seen that the output

terminal OUT is connected to the MOS transistors 3, 4, 9 and 5, 6, 8 through the resistances R_{01} and R_{02}. In similar manner, resistances R_0 can be introduced into the input circuit of the CMOS, as illustrated in Figure 14.

It will be appreciated that the low break-down voltage diodes D_1 and D_2 may be formed by P N P or N P N transistors, rather than the P N transistors previously illustrated, provided that they do not contribute to the parasitic transistor circuits and have satisfactory forward direction characteristics. Also, the CMOS I.C. may have a P-type substrate, rather than the N-type substrate 1.

In the embodiment illustrated in Figures 15 and 16, the noise absorption circuits are constituted by transistors, rather than low break-down voltage diodes. Figure 15 is a section through the I.C., and it will be seen that, in addition to the P-well 2, there is a second P-well 40 formed in the N-type semiconductor substrate 1. An N+ -type semiconductor region 41 is formed in the P-well 40 and a P+ -type semiconductor region 42 is formed outside P-well 40; the output terminal OUT is connected to the regions 41, 42. The regions 41, 42 form with the P-well 40 and the substrate 1 a vertical transistor indicated at Tr_V and a lateral transistor indicated at Tr_L respectively. Supply terminals V_{SS} and V_{DD} are connected respectively to a P+ -type region 43 formed in P-well 40 and a N+ -type region 44 formed in the substrate 1 outside P-well 40. Consequently, the transistors Tr_V and Tr_L are connected between the output terminal OUT and the power source terminals V_{DD} and V_{SS}, as illustrated in the equivalent circuit of Figure 16, to form noise absorption circuits preventing the thyristor phenomenon in the parasitic transistor circuits produced by the previously described parasitic transistors Tr_1 to Tr_4.

The circuit of Figures 15 and 16 causes both external noise and noise produced by internal operation to be absorbed. Thus, for positive impulse noise, the base electrode of transistor Tr_L is equal to V_{DD} and the condition for transistor TR_L to be on is $V_B = V_{DD} + V_{BE}$, and therefore if $V_{DD} \geq +3V$ and $V_{BE} = 0.7V$, the above-mentioned lateral transistor Tr_L will be put on by noise of +3.7 volts or more. Accordingly, noise of 3.7 volts or more is not transmitted into the interior of the CMOS structure but instead is absorbed in the power source V_{SS} (earth) by way of the transistor Tr_L, the parasitic transistor Tr_3 remains in the off state and therefore latch-up does not occur. Similarly for negative impulse noise, the base electrode of transistor Tr_V is equal to V_{SS}, and the condition for that transistor to be on is $V_B \geq V_{BE}$ so that if $V_{DD} = +3V$ and $V_{BE} = 0.7V$, the above-mentioned vertical transistor Tr_V will be put on by noise of -0.7 volts or more. Accordingly, large negative noise of -0.7 volts or more is not transmitted into the interior of the CMOS structure but is absorbed by power source V_{DD} by way of transistor Tr_V, the parasitic transistor Tr_2 remains in the off state, and therefore latch-up does not occur.

It will be seen that in the I.C. of Figures 15 and 16, latch-up is prevented by the use of bipolar transistors (Tr_V and Tr_L) which are similar to the parasitic transistors. Forming noise absorption circuits by means of supplementary transistors is extremely simple, and it is possible to increase the noise absorption effect by using at the same time diodes or resistances as previously described.

It will be appreciated that the noise absorption circuits described herein can be employed, not only with CMOS inverter circuits such as that shown in Figure 1, but also to other kinds of CMOS circuits in which parasitic transistors are formed. Also, as regards the CMOS I.C. structure, the noise absorption circuits can be used where an N-well is or are formed in a P-type semiconductor substrate, and also with a CMOS I.C. having silicon gates.

WHAT WE CLAIMS IS:-

1. A semiconductor integrated circuit comprising a CMOS circuit having an input part, an output part, means for connecting an external, relatively positive, bias voltage source, and means for connecting an external, relatively negative, bias voltage source, the structure of the CMOS circuit being such that parasitic transistors are formed therein; first bypass circuit means connected between the relatively positive bias voltage connecting means and the output part of the CMOS circuit for bypassing noise supplied to the output part at a first level more positive than the relatively positive bias voltage; and second bypass circuit means connected between the relatively negative bias voltage source connecting means and the output part for bypassing noise supplied to the output part at a second level more negative than the relatively negative bias voltage; the first and second bypass circuit means satisfying the following conditions:

(1) when positive noise is supplied to the output part, $Z_1 < Z_3$; and

(2) when negative noise is supplied to the output part, $Z_2 < Z_4$.

where

Z_1 is the internal impedance of the first bypass circuit means when positive noise is supplied to the output part,

Z_2 is the internal impedance of the second bypass circuit means when negative noise is

terminal OUT is connected to the MOS transistors 3, 4, 9 and 5, 6, 8 through the resistances R_{01} and R_{02}. In similar manner, resistances R_{01} can be introduced into the input circuit of the CMOS, as illustrated in Figure 14.

It will be appreciated that the low break-down voltage diodes D_1 and D_2 may be formed by P N P or N P N transistors, rather than the P N transistors previously illustrated, provided that they do not contribute to the parasitic transistor circuits and have satisfactory forward direction characteristics. Also, the CMOS I.C. may have a P-type substrate, rather than the N-type substrate 1.

In the embodiment illustrated in Figures 15 and 16, the noise absorption circuits are constituted by transistors, rather than low break-down voltage diodes. Figure 15 is a section through the I.C., and it will be seen that, in addition to the P-well 2, there is a second P-well 40 formed in the N-type semiconductor substrate 1. An N+ -type semiconductor region 41 is formed in the P-well 40 and a P+ -type semiconductor region 42 is formed outside P-well 40; the output terminal OUT is connected to the regions 41, 42. The regions 41, 42 form with the P-well 40 and the substrate 1 a vertical transistor indicated at Tr_V and a lateral transistor indicated at Tr_L respectively. Supply terminals V_{SS} and V_{DD} are connected respectively to a P+ -type region 43 formed in P-well 40 and a N+ -type region 44 formed in the substrate 1 outside P-well 40. Consequently, the transistors Tr_V and Tr_L are connected between the output terminal OUT and the power source terminals V_{DD} and V_{SS}, as illustrated in the equivalent circuit of Figure 16, to form noise absorption circuits preventing the thyristor phenomenon in the parasitic transistor circuits produced by the previously described parasitic transistors Tr_1 to Tr_4.

The circuit of Figures 15 and 16 causes both external noise and noise produced by internal operation to be absorbed. Thus, for positive impulse noise, the base electrode of transistor Tr_L is equal to V_{DD} and the condition for transistor TR_L to be on is $V_B = V_{DD} + V_{BE}$, and therefore if $V_{DD} \geq +3V$ and $V_{BE} = 0.7V$, the above-mentioned lateral transistor Tr_L will be put on by noise of +3.7 volts or more. Accordingly, noise of 3.7 volts or more is not transmitted into the interior of the CMOS structure but instead is absorbed in the power source V_{SS} (earth) by way of the transistor Tr_L, the parasitic transistor Tr_3 remains in the off state and therefore latch-up does not occur. Similarly for negative impulse noise, the base electrode of transistor Tr_V is equal to V_{SS}, and the condition for that transistor to be on is $V_B \geq V_{BE}$ so that if $V_{DD} = +3V$ and $V_{BE} = 0.7V$, the above-mentioned vertical transistor Tr_V will be put on by noise of -0.7 volts or more. Accordingly, large negative noise of -0.7 volts or more is not transmitted into the interior of the CMOS structure but is absorbed by power source V_{DD} by way of transistor Tr_V, the parasitic transistor Tr_2 remains in the off state, and therefore latch-up does not occur.

It will be seen that in the I.C. of Figures 15 and 16, latch-up is prevented by the use of bipolar transistors (Tr_V and Tr_L) which are similar to the parasitic transistors. Forming noise absorption circuits by means of supplementary transistors is extremely simple, and it is possible to increase the noise absorption effect by using at the same time diodes or resistances as previously described.

It will be appreciated that the noise absorption circuits described herein can be employed, not only with CMOS inverter circuits such as that shown in Figure 1, but also to other kinds of CMOS circuits in which parasitic transistors are formed. Also, as regards the CMOS I.C. structure, the noise absorption circuits can be used where an N-well is or are formed in a P-type semiconductor substrate, and also with a CMOS I.C. having silicon gates.

WHAT WE CLAIMS IS:-

1. A semiconductor integrated circuit comprising a CMOS circuit having an input part, an output part, means for connecting an external, relatively positive, bias voltage source, and means for connecting an external, relatively negative, bias voltage source, the structure of the CMOS circuit being such that parasitic transistors are formed therein; first bypass circuit means connected between the relatively positive bias voltage connecting means and the output part of the CMOS circuit for bypassing noise supplied to the output part at a first level more positive than the relatively positive bias voltage; and second bypass circuit means connected between the relatively negative bias voltage source connecting means and the output part for bypassing noise supplied to the output part at a second level more negative than the relatively negative bias voltage; the first and second bypass circuit means satisfying the following conditions:

(1) when positive noise is supplied to the output part, $Z_1 < Z_3$; and

(2) when negative noise is supplied to the output part, $Z_2 < Z_4$,

where

Z_1 is the internal impedance of the first bypass circuit means when positive noise is supplied to the output part.

Z_2 is the internal impedance of the second bypass circuit means when negative noise is

supplied to the output part, and

Z_3 and Z_4 are the output impedances of the CMOS circuit when positive noise and negative noise are supplied to the output part respectively in the absence of the first and second bypass circuit means, whereby impulse noise capable of triggering the parasitic transistors is absorbed.

2. A semiconductor integrated circuit comprising a CMOS circuit having an input part, an output part, means for connecting an external, relatively positive, bias voltage source, and means for connecting an external, relatively negative, bias voltage source, the structure of the CMOS circuit being such that parasitic transistors are formed therein; a plurality of protective diodes connected to the input part for preventing gate breakdown at the input part; first bypass circuit means connected between the relatively positive bias voltage connecting means and the input part of the CMOS circuit for bypassing noise supplied to the input part at a first level more positive than the relatively positive bias voltage; and second bypass circuit means connected between the relatively negative bias voltage source connecting means and the input part for bypassing noise supplied to the input part at a second level more negative than the relatively negative bias voltage; the first and second bypass circuit means satisfying the following conditions:

(1) when positive noise is supplied to the input part, $Z_1 < Z_3$; and

(2) when negative noise is supplied to the input part, $Z_2 < Z_4$,

where

Z_1 is the internal impedance of the first bypass circuit means when positive noise is supplied to the input part,

Z_2 is the internal impedance of the second bypass circuit means when negative noise is supplied to the input part, and

Z_3 and Z_4 are the input impedances of the CMOS circuit when positive noise and negative noise are supplied to the input part respectively in the absence of the first and second bypass circuit means, whereby impulse noise capable of triggering the parasitic transistors is absorbed.

3. A semiconductor integrated circuit according to any one of the preceding claims, in which each bypass circuit includes a diode.

4. A CMOS circuit according to claim 3, in which each bypass circuit includes a low breakdown voltage diode.

5. A CMOS circuit according to claim 1 or claim 2, in which each bypass circuit includes a bipolar transistor.

6. A CMOS circuit according to any one of claims 3 to 5, in which each diode or bipolar transistor is formed in the substrate of the CMOS circuit.

7. A CMOS circuit substantially as herein described with reference to Figures 4 to 16 of the accompanying drawings.

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