

"DOUBLE-CURRENT DETECTOR"

The present invention relates to a double-current detector, and more particularly to a double-current detector for shaping a double-current signal transmitted through a line of a data transmission system such as telex, for example.

Some conventional double-current detectors for producing a rectangular wave substantially in synchronism with a received double-current signal from a data transmission system include rheostats or variable resistors for adjusting positive and negative slice levels employed by comparators which compare output signals from photocouplers with such slice levels. However, the use of such rheostats has been disadvantageous in that the cost of the double-current detectors is high, and slice level adjustments are necessary. Furthermore, characteristic variations of the photocouplers must be small.

The present invention seeks to provide a double-current detector which requires no rheostats for adjusting slice levels for signal level comparison, which is inexpensive to manufacture, and which is substantially free from limitations caused by variations in the characteristics of the photocouplers used.

According to the present invention there is provided a double-current detector for generating a rectangular waveform signal substantially in phase with a received double-current signal, said detector comprising a full-wave rectifying bridge circuit having a pair of AC terminals for receiving the double-current therebetween, a pair of DC terminals, a first photocoupler including a light-emitting element connected between said DC terminals, and a second photocoupler including a light-emitting element connected in one arm of the bridge circuit; first means responsive to an

output signal from said first photocoupler for generating a first signal indicative of whether the absolute value of said double current signal exceeds a prescribed value or not; second means responsive to an output
5 signal from said second photocoupler for generating a second signal indicative of whether the double current signal exceeds a prescribed value; a flip-flop; and circuit means responsive to said first and second signals for controlling said flip-flop to produce an output
10 signal in the form of said rectangular waveform signal.

The current which flows through the first light-emitting element goes in one direction only irrespective of whether a positive or negative current flows between the AC terminals. Increases in the
15 positive and negative currents are thus detected by the same first photocoupler in combination with the first means. Therefore, positive and negative slice levels used by the first means automatically remain the same without adjustments which would otherwise be carried
20 out by rheostats. The double-current detector is also substantially free from the effects of characteristic variations of the first and second photocouplers.

The polarity of the current is detected by the second photocoupler. The rectangular waveform signal
25 can be generated substantially in synchronism with the received double-current signal based on the result of detection of the current increase using the first photocoupler and the result of detection of the current polarity using the first photocoupler.

30 In order that the invention may be better understood, an embodiment thereof will now be described by way of example only and with reference to the accompanying drawings in which:-

35 Figures 1A and 1B are respectively circuit diagrams of a double-current detector according to the present invention;

Figure 2 is a timing chart showing the operation of the double-current detector shown in Figures 1A and 1B.

As shown in Figures 1A and 1B, a double-current
5 detector according to an embodiment of the present invention has a full-wave rectifying bridge circuit BR having an AC terminal U coupled through a variable resistor or rheostat VR to a line of a data trans-
mission system such as telex, and an AC terminal V
10 connected to ground. The rectifying bridge circuit BR also has a pair of diagonal DC terminals P, N between which a light-emitting element such as a light-emitting diode LED 1 of a photocoupler PC 1 is connected, the light-emitting diode LED 1 being shunted by a resistor
15 rl.

The rectifying bridge circuit BR has three arms or branches having respective diodes D1, D2, D3 and a fourth arm comprising a light-emitting element such as a light-emitting diode LED 2 of a photocoupler PC2 and a resistor r2 connected across the light-emitting diode
20 LED 2. The diode D1 is connected between the terminals U, P, and the diode D2 is connected between the terminals P, V. The diode D3 is connected between the terminals V, N, and the light-emitting diode LED 2
25 is connected between the terminals N, U.

The diodes D1, D2, D3 and the light-emitting diodes LED 1 are oriented such that both a positive current flowing between the AC terminals U, V and a negative current flowing between the AC terminals U, V
30 will flow through the light-emitting diode LED 1 in the forward direction thereof, and only a negative current flowing between terminals U, V will flow through the light-emitting diode LED 2 in its forward direction.

The resistors rl, r2 connected across the
35 respective light-emitting diodes LED 1, LED 2 have resistances selected to meet the following

relationship:-

$$r_1 < r_2$$

The photocouplers PC1, PC2 have respective light detectors such as phototransistors PT1, PT2.

5 The phototransistors PT1, PT2 have collectors connected to a power supply VCC (=5V), and emitters connected to ground through resistors r3, r4 respectively, the emitters being also coupled to the positive input terminals, respectively, of comparators COM1, COM2.

10 The comparators COM1, COM2 have negative input terminals supplied with output reference signals from respective voltage dividers that comprise series-connected resistors r5, r7 and series-connected resistors r6, r8, respectively, which are joined to the
15 power supply Vcc.

The comparators COM1, COM2 produce a signal of logic level "1" at their respective output terminals OUT1, OUT2 when the signals applied to their positive input terminals are greater than the reference signals
20 applied to their negative input terminals.

The resistors r5, r7 are of such resistances that when a current equal to or greater than 3 mA flows through the light-emitting diode LED1, the signal applied to the positive input terminal of the
25 comparator COM1 is higher than the signal applied to the negative input terminal thereof. The resistors r6, r8 are of such resistances that when a current equal to or greater than 2 mA flows through the light-emitting diode LED2, the signal applied to the positive
30 input terminal of the comparator COM2 is higher than the signal applied to the negative input terminal thereof.

The output signals from the comparators COM1, COM2 are applied to an AND gate AND2. The output
35 signal from the AND gate AND2 is applied to the K input terminal of a JK flip-flop F/F. The output signal

from the comparator COM2 is applied via an inverter NOT to an AND gate AND1, to which the output signal from the comparator COM1 is also supplied. The output terminal of the AND gate AND1 is connected to the J
5 input terminal of the JK flip flop F/F.

Figure 2 shows the waveforms of various signals produced in the double-current detector illustrated in Figures 1A and 1B. The double-current detector of the invention serves to shape and convert a double-current
10 signal (a) to a rectangular waveform signal (d) in Figure 2.

A double-current signal transmitted through a line from an exchange is normally of about 20 mA. During a period in which a positive current (indicated
15 by the solid line in Figure 1A) flows between the AC terminals U, V, the current flows from the diode D1 through the light-emitting diode LED 1 or its parallel-connected resistor r1 to the diode D3. While a negative current (indicated by the broken line in
20 Figure 1A) is flowing between the AC terminals U, V, the current flows from the diode D2 through the light-emitting diode LED1 or its parallel-connected resistor r1 to the light-emitting diode LED2 or its parallel-connected resistor r2. Therefore, current flows
25 through the light-emitting diode LED1 in its forward direction irrespective of whether the current is positive or negative. Thus, whenever the magnitude of the received current exceeds a first prescribed slice level SL1 irrespective of whether the received current
30 is positive or negative, the comparator COM1 produces an output signal of "1" (as shown at (b) in Figure 2).

Current flows through the light-emitting diode LED2 only when the current flowing between the AC terminals U, V is negative. Accordingly, whenever the
35 received current is negative and its magnitude exceeds a second prescribed slice level SL2, the comparator

COM2 produces an output signal of "1" (as shown at (c) in Figure 2).

5 The second slice level SL2 is smaller than the first slice level SL1 so that the output signal from the comparator COM2 becomes "1" earlier than the output signal from the comparator COM1. In the illustrated embodiment, the first slice level SL1 is 3 mA whereas the second slice level SL2 is - 2mA. The resistance of the resistor r2 is greater than the resistance of
10 the resistor r1 to ensure that the light-emitting diode LED2 is rendered conductive earlier than the light-emitting diode LED1.

When a positive current increases to a level such that it exceeds the first slice level SL1 (3mA),
15 the output OUT1 from the comparator COM1 goes high ("1"). At this time, the output OUT2 of the comparator COM2 remains low. The output OUT1 and an inverted signal of the output OUT2 from the inverter NOT are ANDed by the AND gate AND1 which produces an
20 output signal of "1". The outputs OUT1, OUT2 are ANDed by the AND gate AND2 which produces an output signal of "0". Therefore, the output OUT from the flip-flop F/F becomes "1" in synchronism with the next clock pulse.

25 When a negative current increases, the output OUT2 becomes "1" and then the output OUT1 becomes "1". The AND gate AND2 by which the outputs OUT2, OUT1 are ANDed produces an output signal of "1", and the AND gate AND1 by which the output OUT1 and an inverted
30 signal of the output OUT2 are ANDed produces an output signal of "0". Consequently, the output OUT from the flip-flop F/F becomes "0" in synchronism with the next clock pulse.

The aforesaid cycle of operation is repeated to
35 enable the flip-flop F/F to generate a rectangular waveform signal which is substantially synchronous or

in phase with the received current signal.

The current which flows through the light-emitting diode LED1 goes in one direction only irrespective of whether a positive or negative current flows between the AC terminals U, V. Increases in the positive and negative currents are thus detected by the same photocoupler PC1 in combination with the comparator COM1. Therefore, the positive and negative slice levels automatically remain the same without adjustments which would otherwise be carried out by rheostats. The double-current detector is also substantially free from limitations arising from characteristic variations of the photocouplers PC1, PC2.

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1. A double-current detector for generating a rectangular waveform signal (d) substantially in phase with a received double-current signal (a), said
5 detector comprising:

a full-wave rectifying bridge circuit (BR) having a pair of AC terminals (U, V) for receiving the double-current signal (a) therebetween, a pair of DC terminals (P, N), a first photocoupler (PC1) including
10 a light-emitting element (LED1) connected between said DC terminals (P, N), and a second photocoupler (PC2) including a light-emitting element (LED2) connected in one arm of the bridge circuit (BR);

first means responsive to an output signal from
15 said first photocoupler (PC1) for generating a first signal (OUT 1) indicative of whether the absolute value of said double current signal (a) exceeds a prescribed value (SL1) or not;

second means responsive to an output signal
20 from said second photocoupler (PC2) for generating a second signal (OUT 2) indicative of whether the double current signal (a) exceeds a prescribed value (SL2);

a flip-flop (F/F); and

circuit means responsive to said first and
25 second signals for controlling said flip-flop (F/F) to produce an output signal in the form of said rectangular waveform signal (d).

2. A double-current detector according to claim 1, wherein said first and second means comprise first and
30 second comparators (COM1, COM2), respectively, said circuit means including an inverter (NOT) having an input terminal connected to an output terminal of said second comparator (COM2), a first AND gate (AND1) having an input terminal connected to an output
35 terminal of said first comparator (COM1) and another input terminal connected to an output terminal of said



inverter (NOT), and a second AND gate (AND2) having an input terminal connected to the output terminal (OUT1) of said first comparator (COM1) and another input terminal connected to the output terminal (OUT2) of said second comparator (COM2), said first and second AND gates having respective output terminals coupled to said flip-flop (F/F).

3. A double-current detector according to either one of claims 1 or 2 wherein said flip-flop (F/F) comprises a J-K flip-flop having a J input terminal connected to the output terminal of said first AND gate (AND1) and a K input terminal connected to the output terminal of said second AND gate (AND2).

4. A double-current detector for generating a rectangular waveform signal substantially in phase with a received double-current signal substantially as hereinbefore described with reference to the accompanying drawings.

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