

CLAIMS

What is claimed is:

1. An NMOS semiconductor device, comprising:
 - a fin on a substrate, the fin comprising a semiconductor material and having channel region and corresponding source/drain regions adjacent thereto, wherein the fin has a first width (W1);
 - a cladding layer of germanium or silicon germanium (SiGe) on one or more surfaces of the channel region of the fin;
 - a gate dielectric layer over the cladding layer;
 - a gate electrode on the gate dielectric layer; and
 - N+ doped source/drain material in each of the source/drain regions.
2. The NMOS semiconductor device of claim 1, wherein the substrate is comprised of a silicon wafer in a (110) orientation, and wherein the fin is configured with a <110> channel orientation.
3. The NMOS semiconductor device of claim 1, wherein the cladding layer is comprised of between 10 atomic% to 90 atomic% germanium.
4. The NMOS semiconductor device of claim 1, wherein the cladding layer covers opposing side portions and a top portion of the fin in the channel region.
5. The NMOS semiconductor device of claim 1, wherein the cladding layer has a thickness of 2 nm or less.
6. The NMOS semiconductor device of claim 1, wherein the base of the fin is equal to W1 and the top of the fin is a second width (W2).

7. The NMOS semiconductor device of claim 1, wherein W1 is less than or equal to 4 nm.
8. The NMOS semiconductor device of claim 1, wherein the fin includes a third width (W3), and wherein W3 is an overall width based on a thickness of the cladding layer and a width of the fin.
9. The NMOS semiconductor device of claim 1, wherein the cladding layer is deposited such that the ratio of cladding thickness to fin width is a ratio of at least 1 nm of cladding layer for every 2 nm of fin width.
10. An integrated circuit comprising the NMOS semiconductor device of any of claims 1-9.
11. A complementary metal oxide semiconductor (CMOS) comprising the NMOS semiconductor device of any of claims 1-9.
12. A method of forming a NMOS semiconductor device, the method comprising:
forming at least one fin in or on a substrate, wherein the at least one fin has a first width (W1);
depositing an insulator material in the trenches;
forming a dummy gate on a channel region of the at least one fin;
depositing an additional insulator material over surfaces of the at least one fin;
removing the dummy gate to expose the channel region of the at least one fin; and
depositing a cladding layer on one or more surfaces of the channel region of the at least one fin.
13. The method of claim 12, wherein the cladding layer is comprised of germanium (Ge) or silicon germanium (SiGe).

14. The method of claim 12, wherein the cladding layer is comprised of between 10% to 90% Ge.

15. The method of claim 12, wherein forming the at least one fin in or on a substrate further includes the substrate being comprised of a (110) oriented Si wafer.

16. The method of claim 12, further comprising thinning the at least one fin in the channel region to have a second width (W2).

17. The method of claim 12, wherein depositing a cladding layer on one or more surfaces of the channel region of the at least one fin includes selectively depositing the cladding layer on the one or more surfaces of the channel region.

18. The method of claim 12, wherein depositing a cladding layer on one or more surfaces of the channel region of the at least one fin includes the fin having a third width (W3).

19. The method of any of claims 12-18, further comprising selecting a thickness of the cladding layer such that for every 1 nm of fin width 2 nm of cladding layer is deposited.

20. A mobile computing system, comprising:
a printed circuit board;
a processor operatively coupled to the printed circuit board;
a memory operatively coupled to the printed circuit board and in communication with the processor; and

a wireless communication chip operatively coupled to the printed circuit board and in communication with the processor;

wherein at least one of the processor, wireless communication chip, and/or the memory comprises a NMOS semiconductor device including:

a fin on a substrate, the fin comprising a semiconductor material and having channel region and corresponding source/drain regions adjacent thereto;

a cladding layer of germanium (Ge) or silicon germanium (SiGe) on one or more surfaces of the channel region of the fin;

a gate dielectric layer over the cladding layer;

a gate electrode on the gate dielectric layer; and

N⁺ doped source/drain material in each of the source/drain regions.

21. The system of claim 20, wherein the fin is silicon, and the cladding layer is SiGe.

22. The system of claim 20, wherein the source/drain regions include embedded epitaxially grown silicon.

23. The system of claim 20, wherein the fin includes a first width (W1) at a base of the substrate and a second width (W2) at a top of the fin.

24. The system of claim 20, wherein the fin includes a third width (W3), wherein W3 is an overall width of the fin based on a thickness of the cladding layer and a width of the fin.

25. The system of claim 24, wherein W3 includes a ratio of at least 1 nm of cladding layer for every 2 nm of fin width.

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What is claimed is:

1. An NMOS semiconductor device, comprising:
 - a fin on a substrate, the fin comprising a semiconductor material and having channel region and corresponding source/drain regions adjacent thereto, wherein the fin has a first width (W1);
 - a cladding layer of germanium or silicon germanium (SiGe) on one or more surfaces of the channel region of the fin;
 - a gate dielectric layer over the cladding layer;
 - a gate electrode on the gate dielectric layer; and
 - N+ doped source/drain material in each of the source/drain regions.
2. The NMOS semiconductor device of claim 1, wherein the substrate is comprised of a silicon wafer in a (110) orientation, and wherein the fin is configured with a <110> channel orientation.
3. The NMOS semiconductor device of claim 1 or 2, wherein the cladding layer is comprised of between 10 atomic% to 90 atomic% germanium.
4. The NMOS semiconductor device of any of the preceding claims, wherein the cladding layer covers opposing side portions and a top portion of the fin in the channel region.
5. The NMOS semiconductor device of any of the preceding claims, wherein the cladding layer has a thickness of 2 nm or less.
6. The NMOS semiconductor device of any of the preceding claims, wherein the base of the fin is equal to W1 and the top of the fin is a second width (W2).

7. The NMOS semiconductor device of any of the preceding claims, wherein W1 is less than or equal to 4 nm.

8. The NMOS semiconductor device of any of the preceding claims, wherein the fin includes a third width (W3), and wherein W3 is an overall width based on a thickness of the cladding layer and a width of the fin.

9. The NMOS semiconductor device of any of the preceding claims, wherein the cladding layer is deposited such that the ratio of cladding thickness to fin width is a ratio of at least 1 nm of cladding layer for every 2 nm of fin width.

10. An integrated circuit comprising the NMOS semiconductor device of any of the preceding claims.

11. A complementary metal oxide semiconductor (CMOS) comprising the NMOS semiconductor device of any of claims 1 through 9.

12. A method of forming a NMOS semiconductor device, the method comprising:
forming at least one fin in or on a substrate, wherein the at least one fin has a first width (W1);
depositing an insulator material in the trenches;
forming a dummy gate on a channel region of the at least one fin;
depositing an additional insulator material over surfaces of the at least one fin;
removing the dummy gate to expose the channel region of the at least one fin; and
depositing a cladding layer on one or more surfaces of the channel region of the at least one fin.

13. The method of claim 12, wherein the cladding layer is comprised of germanium (Ge) or silicon germanium (SiGe).

14. The method of claim 12 or 13, wherein the cladding layer is comprised of between 10% to 90% Ge.

15. The method of any of claims 12 through 14, wherein forming the at least one fin in or on a substrate further includes the substrate being comprised of a (110) oriented Si wafer.

16. The method of any of claims 12 through 15, further comprising thinning the at least one fin in the channel region to have a second width (W2).

17. The method of any of claims 12 through 16, wherein depositing a cladding layer on one or more surfaces of the channel region of the at least one fin includes selectively depositing the cladding layer on the one or more surfaces of the channel region.

18. The method of any of claims 12 through 17, wherein depositing a cladding layer on one or more surfaces of the channel region of the at least one fin includes the fin having a third width (W3).

19. The method of any of claims 12 through 18, further comprising selecting a thickness of the cladding layer such that for every 1 nm of fin width 2 nm of cladding layer is deposited.

20. A mobile computing system, comprising:
a printed circuit board;
a processor operatively coupled to the printed circuit board;
a memory operatively coupled to the printed circuit board and in communication with the processor; and

a wireless communication chip operatively coupled to the printed circuit board and in communication with the processor;

wherein at least one of the processor, wireless communication chip, and/or the memory comprises a NMOS semiconductor device including:

a fin on a substrate, the fin comprising a semiconductor material and having channel region and corresponding source/drain regions adjacent thereto;

a cladding layer of germanium (Ge) or silicon germanium (SiGe) on one or more surfaces of the channel region of the fin;

a gate dielectric layer over the cladding layer;

a gate electrode on the gate dielectric layer; and

N⁺ doped source/drain material in each of the source/drain regions.

21. The system of claim 20, wherein the fin is silicon, and the cladding layer is SiGe.

22. The system of claim 20 or 21, wherein the source/drain regions include embedded epitaxially grown silicon.

23. The system of any of claims 20 through 22, wherein the fin includes a first width (W1) at a base of the substrate and a second width (W2) at a top of the fin.

24. The system of any of claims 20 through 23, wherein the fin includes a third width (W3), wherein W3 is an overall width of the fin based on a thickness of the cladding layer and a width of the fin.

25. The system of claim 24, wherein W3 includes a ratio of at least 1 nm of cladding layer for every 2 nm of fin width.