

VIDEO SIGNAL DELAY AND FILTER NETWORK

This invention concerns a video signal processing network exhibiting signal filtering and delaying functions. In particular, this invention concerns a network, in a
5 color television receiver for processing luminance and chrominance video signal components, for trapping (nulling) the chrominance component at the input of a luminance signal delaying circuit.

In a conventional color television receiver, the
10 luminance and chrominance components of a baseband composite video signal are processed in separate channels before being combined in a matrix circuit to produce plural color image representative signals. The chrominance signal processing channel exhibits a much narrower frequency
15 bandwidth compared to the bandwidth of the luminance signal processing channel. As a result of this difference in bandwidth, the chrominance signal at the output of the chrominance channel is delayed in time relative to the luminance signal at the output of the luminance channel.
20 The delay between the luminance and chrominance signals must be eliminated before the luminance and chrominance signals are combined in the matrix circuit, since it is necessary for the luminance and chrominance signals to exhibit proper timing synchronism when combined to assure
25 that output color image signals from the matrix circuit are properly constituted.

The described delay between the chrominance and luminance signals is customarily eliminated by means of a wide bandwidth, linear phase delay circuit such as a
30 luminance delay line included in the luminance channel. The delay line is resistively terminated in its characteristic impedance at both input and output ends to prevent unwanted reflections of the luminance signal from the ends of the delay line. A band reject filter which
35 acts as a chrominance trap usually precedes the luminance delay line to prevent the chrominance signal from being conveyed to the luminance channel.

In one known, widely used configuration of a luminance delay line and chrominance trap, the trap is a parallel tuned inductor-capacitor network coupled in series between a luminance signal source and the
5 input of the luminance delay line. This configuration undesirably exhibits a widely varying frequency dependent source impedance at the input of the delay line as the frequency of the wideband luminance input signal varies about the frequency to which the trap is tuned. The
10 varying impedance at the input of the delay line leads to an impedance mismatch at the delay line input, with attendant luminance signal reflections from the ends of the delay line. The signal reflections can lead to significant degradation of a displayed video image such
15 as by creating secondary images, or "ghosts", in a displayed image.

The impedance variations (mismatch) at the input of the luminance delay line and the problems created thereby are reduced significantly by a trap and delay
20 circuit configuration in accordance with the principles of the present invention. In a disclosed implementation of a trap and delay circuit pursuant to the present invention, the source impedance at the input of a luminance delay line includes first and second resistive elements with a total
25 value related to the characteristic impedance of the delay line. A chrominance signal trap is coupled between the junction of the first and second resistive elements and a point of reference potential.

In the drawing:

30 FIGURE 1 shows a portion of a color television receiver including a luminance trap and delay line configuration in accordance with the principles of the present invention; and

35 FIGURE 2 illustrates an impedance versus frequency response characteristic helpful in understanding the operation of the trap and delay line configuration of FIGURE 1.

In FIGURE 1, a composite baseband television signal from a source 10, including luminance and

chrominance signal components, is coupled to a chrominance signal processing channel including a chrominance bandpass network 12 which selectively conveys the chrominance component to a chrominance signal processor 14 of conventional design for producing r-y, g-y and b-y color difference signals. The color difference signals are combined in a matrix amplifier 16 with a processed luminance signal Y from a luminance processor 18 for producing low level color image representative video signals r, g and b. These color signals are amplified by a display driver stage 20 which provides output high level color image signals R, G and B suitable for driving an image display device such as a kinescope.

The signal from source 10 is also coupled to a luminance signal processing channel including a chrominance trapping and luminance delaying network 30 and luminance processor 18. The luminance signal in this example exhibits a bandwidth of from zero Hertz to slightly above 3.0 MHz, which is significantly wider than the chrominance signal bandwidth of $3.58 \text{ MHz} \pm 0.5 \text{ MHz}$.

Network 30, which may be constructed as a monolithic encapsulated circuit, includes a wideband luminance delay line 34 which exhibits a substantially linear phase characteristic over the luminance signal bandwidth. Delay line 34 may be of the glass or inductor-capacitor type, for example. The output of delay line 34 is terminated in its characteristic impedance by means of a load resistor RL. Resistors RS1 and RS2 represent the luminance signal source resistance with respect to the input of delay line 34. The value of resistor RS1 includes the value of a coupling resistor as illustrated, plus the value of a driving source resistance at the output of source 10, e.g., the low output resistance of an output emitter follower transistor. The input of delay line 34 is terminated by means of resistors RS1 and RS2, the combined value of which substantially equals the characteristic impedance of delay line 34.

indicated by response B. Over a luminance signal passband from frequency f_0 (zero Hertz) to a frequency of 3.0 MHz, the known arrangement exhibits a source impedance variation $\Delta 1$, which is significantly greater than a source impedance variation $\Delta 2$ exhibited by the illustrated arrangement in accordance with the present invention over the same passband.

Because of the reduced source impedance variation exhibited by the disclosed arrangement, the amplitude of mismatch induced luminance signal reflections through delay line 34 is reduced significantly. Also, any signals reflected from trap 32 toward load resistor R_L are conducted via resistor RS_2 and are attenuated by a factor of $1 + RS_2/R_L$. These properties of the disclosed arrangement greatly reduce the amount of signal reflections produced by impedance mismatch at the input of the delay line, thereby reducing degradation of a displayed image due to secondary images, or "ghosts". In addition, both the amplitude and duration of video image degrading signal "ringing" induced by impedance mismatch at the delay line input are significantly reduced by the more uniform impedance matching at the input of the delay line of the disclosed arrangement.

The choice of the values of resistors RS_1 and RS_2 depends upon the requirements of a particular system. A small value of resistor RS_1 causes trap 32 to exhibit reduced trapping depth. If the value of resistor RS_2 is reduced, reflected luminance signals through delay line 34 will be attenuated less. Thus the choice of values for resistors RS_1 and RS_2 involves a compromise between a desired trapping depth and a permissible amplitude of reflected luminance signals.

Network 30 also includes a band reject filter 32 including series resonant inductor 35 and capacitor 36 coupled between the junction of resistors RS1 and RS2 in the luminance signal path and a point of reference potential (ground). Filter 32 is tuned to the 3.58 MHz chrominance subcarrier frequency and acts as a chrominance trap to prevent the chrominance component from being conveyed to the luminance channel including delay line 34 and processor 18.

FIGURE 2 illustrates the frequency dependent source impedance variations at the input of delay line 34.

In FIGURE 2, response A depicts the source impedance (Z) variation with frequency (f) for the disclosed arrangement of source resistors RS1 and RS2 with trap 32. The source impedance varies from a maximum value R_S , corresponding to the sum of the values of resistors RS1 and RS2, at lower luminance signal frequencies between frequencies f_0 and f_1 , and at higher luminance signal frequencies greater than a frequency f_2 . The source impedance declines over an intermediate frequency range between frequencies f_1 and f_2 , reaching a minimum value corresponding to the value of source resistor RS2 at the 3.58 MHz frequency to which trap 32 is tuned. The range of source impedance variation, between the combined values of resistors RS1 and RS2 and the value of resistor RS2, produces an acceptably small impedance mismatch at the input of delay line 34.

For the purpose of comparison, a response B in FIGURE 2 depicts the frequency dependent source impedance variation of a known chrominance trap and luminance delay line arrangement which employs a source resistor and a parallel tuned trap tuned to 3.58 MHz coupled in series between a video signal source and a luminance delay line. In such known arrangement, as employed in RCA color television receiver chassis CTC-118 for example, the source impedance variations are extreme, ranging from the value of the source resistance (R_S) at lower luminance frequencies to infinity at the 3.58 MHz trapping frequency, as



CLAIMS:

1. In a video signal processing system including a luminance channel for processing a luminance signal and a chrominance channel for processing a chrominance signal including a chrominance subcarrier component, said processing system comprising:

a signal source having an output providing said luminance and chrominance signal;

signal delaying means having an input and an output;

luminance signal processing means for receiving delayed signals from said output of said signal delaying means;

source resistance means including first and second series resistive elements for coupling said luminance signal of said signal source to said input of said signal delaying means;

filter means coupled from the junction of said first and second resistive elements to a point of reference potential (ground) for trapping said chrominance signal; and wherein

said first and second resistors are of different values selected to provide a predetermined value of trapping depth of said chrominance signal by said filter means and a predetermined amplitude of reflected luminance signal in said signal delaying means.

2. A video processing system as recited in Claim 1, wherein said first resistor is of a relatively small value as compared with said second resistor thereby providing reduced trapping depth for said filter means and reduced reflections for said delaying means.



3. A video processing system as recited in Claim 1, wherein said second resistor is of a relatively small value as compared with said first resistor thereby providing increased trapping depth for said filter means and increased reflections for said delaying means.

4. A video processing system as recited in Claim 1, wherein said signal source of a type exhibiting a low output impedance and said first resistor is coupled directly to said source without intervening elements.

5. A video signal processing system substantially as hereinbefore described with reference to the accompanying drawing.
