CLAIMS

1. A method of providing a semiconductor device, the method comprising:

   providing a flexible substrate;

   depositing at least one layer of material over the flexible substrate, wherein depositing the at least one layer of material over the flexible substrate occurs at a temperature of at least 180°C; and

   providing a diffusion barrier between a metal layer and an N+ amorphous silicon layer.

2. The method of claim 1, wherein:

   depositing the at least one layer of material over the flexible substrate comprises depositing an amorphous silicon layer.

3. The method of claim 2, wherein:

   depositing the at least one layer of material over the flexible substrate further comprises depositing a silicon nitride gate dielectric.

4. The method of claim 3, wherein:

   depositing the at least one layer of material over the flexible substrate further comprises depositing a silicon nitride intermetal dielectric layer.

5. The method of claim 1, wherein:

   depositing the at least one layer of material over the flexible substrate occurs at a temperature of at least 188°C.

6. The method of claim 5, wherein:

   depositing the at least one layer of material over the flexible substrate occurs at near vacuum pressure.

7. The method of claim 1, wherein:

   the diffusion barrier comprises tantalum.

8. The method of claim 1, wherein:

the flexible substrate comprises a planarized flexible substrate.

9. The method of claim 1, further comprising:

providing a carrier substrate; and

coupling the carrier substrate to the flexible substrate.

10. The method of claim 1, further comprising:

providing a first dielectric material, wherein the first dielectric material comprises an organic siloxane-based dielectric material.

11. The method of claim 10, further comprising:

providing a second dielectric material, wherein the second dielectric material comprises silicon nitride and is deposited over the first dielectric material; and

baking the first dielectric material, the second dielectric material, the flexible substrate, and the at least one layer of material, wherein the temperature of the baking reaches at least 200°C.

12. The method of claim 10, wherein:

providing a base dielectric material before providing the first dielectric material, wherein the base dielectric material comprises silicon oxide.

13. The method of claim 1, wherein:

the flexible substrate comprises polyethylene naphthalate.

14. A method of providing a semiconductor device, the method comprising:

providing a carrier substrate;

providing a flexible substrate, wherein the flexible substrate is planarized;

coupling the carrier substrate to the flexible substrate;

depositing a gate metal layer over the flexible substrate;

depositing one or more silicon comprising layers over the gate metal layer, wherein the temperature of the depositing the one or more silicon comprising layers reaches at least 180°C;

depositing one or more contact elements over the one or more silicon comprising layers, wherein the one or more contact elements comprises a diffusion barrier;

depositing a first dielectric material over the one or more contact elements, wherein the first dielectric material comprises an organic siloxane-based dielectric material;

depositing a second dielectric material over the first dielectric material, wherein the second dielectric material comprises silicon nitride; and

baking the first dielectric material, the second dielectric material, the flexible substrate, the carrier substrate, the gate metal layer, the one or more silicon comprising layers, and the one or more contact elements, wherein the temperature of the baking reaches at least 200°C.

15. The method of claim 14, wherein:

the one or more silicon comprising layers comprises an amorphous silicon layer.

16. The method of claim 15, wherein:

the one or more silicon comprising layers further comprises a silicon nitride gate dielectric layer and a silicon nitride intermetal dielectric layer.

17. The method of claim 16, further comprising:

etching the silicon nitride intermetal dielectric layer, the amorphous silicon layer, and the silicon nitride gate dielectric layer so that a portion of the amorphous silicon layer is exposed; and

depositing a mesa passivation layer over the silicon nitride intermetal dielectric layer, the amorphous silicon layer, and the silicon nitride gate dielectric layer so that the mesa passivation layer covers the exposed portion of the amorphous silicon layer.

18. The method of claim 14, wherein:

the diffusion barrier comprises tantalum; and

the one or more contact elements further comprises a metal layer and N+ amorphous silicon layer.

19. The method of claim 18, wherein:

depositing one or more contact elements comprises depositing the diffusion barrier between the metal layer and the N+ amorphous silicon layer.

20. The method of claim 19, further comprising:

etching the one or more contact elements, wherein the one or more contact elements are etched in a single process.

21. The method of claim 14, wherein:

depositing one or more one silicon comprising layers comprises using plasma-enhanced chemical vapor deposition.

22. A semiconductor device, the semiconductor device comprising:

a flexible substrate;

a metal gate layer over the flexible substrate;

an amorphous silicon layer over the metal gate layer, wherein the amorphous silicon layer is deposited during a process at a temperature of at least 180°C;

an N+ amorphous silicon layer over the amorphous silicon layer;

a diffusion barrier; and

a metal layer;

wherein the diffusion barrier is positioned between the metal layer and the N+ amorphous silicon layer.

23. The semiconductor device of claim 22, wherein:

the flexible substrate comprises polyethylene naphthalate.

24. The semiconductor device of claim 22, wherein:

the diffusion barrier comprises tantalum.

25. The semiconductor device of claim 22, wherein:

the metal layer comprises aluminum.

26. The semiconductor device of claim 22, further comprising:

a mesa passivation layer between the amorphous silicon layer and the N+ amorphous silicon layer.

CLAIMS

1. A method of providing a semiconductor device, the method comprising:

providing a flexible substrate;

depositing at least one layer of material over the flexible substrate, wherein depositing the at least one layer of material over the flexible substrate occurs at a temperature of at least 180°C;

providing a diffusion barrier between a metal layer and an N+ amorphous silicon layer under the metal layer; and

providing a first dielectric material over the metal layer, wherein the first dielectric material comprises an organic siloxane-based dielectric material.

2. The method of claim 1, wherein:

depositing the at least one layer of material over the flexible substrate comprises at least one of:

depositing an amorphous silicon layer;

depositing a silicon nitride gate dielectric; or

depositing a silicon nitride intermetal dielectric layer.

3. The method of claim 1, wherein at least one of:

depositing the at least one layer of material over the flexible substrate occurs at a temperature of at least 188°C; or

depositing the at least one layer of material over the flexible substrate occurs at near vacuum pressure.

4. The method of claim 1, wherein at least one of:

the diffusion barrier comprises tantalum; or

the flexible substrate comprises polyethylene naphthalate.

5. The method of claim 1, wherein:

the flexible substrate comprises a planarized flexible substrate.

6. The method of any one of claims 1-5, further comprising:

providing a carrier substrate; and

coupling the carrier substrate to the flexible substrate.

7. The method of any one of claims 1-5, further comprising:

providing a second dielectric material, wherein the second dielectric material comprises silicon nitride and is deposited over the first dielectric material; and

baking the first dielectric material, the second dielectric material, the flexible substrate, and the at least one layer of material, wherein the temperature of the baking reaches at least 200°C.

8. The method of any one of claims 1-5, wherein:

providing a base dielectric material before providing the first dielectric material, wherein the base dielectric material comprises silicon oxide.

9. A method of providing a semiconductor device, the method comprising:

providing a carrier substrate;

providing a flexible substrate, wherein the flexible substrate is planarized;

coupling the carrier substrate to the flexible substrate;

depositing a gate metal layer over the flexible substrate;

depositing one or more silicon comprising layers over the gate metal layer, wherein the temperature of the depositing the one or more silicon comprising layers reaches at least 180°C;

depositing one or more contact elements over the one or more silicon comprising layers, wherein the one or more contact elements comprises a diffusion barrier;

depositing a first dielectric material over the one or more contact elements, wherein the first dielectric material comprises an organic siloxane-based dielectric material;

depositing a second dielectric material over the first dielectric material, wherein the second dielectric material comprises silicon nitride; and

baking the first dielectric material, the second dielectric material, the flexible substrate, the carrier substrate, the gate metal layer, the one or more silicon comprising layers, and the one or more contact elements, wherein the temperature of the baking reaches at least 200°C.

10. The method of claim 9, wherein:

the one or more silicon comprising layers comprises an amorphous silicon layer.

11. The method of claim 10, wherein:

the one or more silicon comprising layers further comprises a silicon nitride gate dielectric layer and a silicon nitride intermetal dielectric layer.

12. The method of claim 11, further comprising:

etching the silicon nitride intermetal dielectric layer, the amorphous silicon layer, and the silicon nitride gate dielectric layer so that a portion of the amorphous silicon layer is exposed; and

depositing a mesa passivation layer over the silicon nitride intermetal dielectric layer, the amorphous silicon layer, and the silicon nitride gate dielectric layer so that the mesa passivation layer covers the exposed portion of the amorphous silicon layer.

13. The method of any one of claims 9-12, wherein:

the diffusion barrier comprises tantalum; and

the one or more contact elements further comprises a metal layer and N+ amorphous silicon layer.

14. The method of claim 13, wherein:

depositing one or more contact elements comprises depositing the diffusion barrier between the metal layer and the N+ amorphous silicon layer.

15. The method of claim 14, further comprising:

etching the one or more contact elements, wherein the one or more contact elements are etched in a single process.

16. The method of any one of claims 9-12, wherein:

depositing one or more one silicon comprising layers comprises using plasma-enhanced chemical vapor deposition.

17. A semiconductor device, the semiconductor device comprising:

a flexible substrate;

a metal gate layer over the flexible substrate;

an amorphous silicon layer over the metal gate layer, wherein the amorphous silicon layer is deposited during a process at a temperature of at least 180°C;

an N+ amorphous silicon layer over the amorphous silicon layer;

a diffusion barrier; and

a metal layer;

wherein:

the diffusion barrier is positioned between the metal layer and the N+ amorphous silicon layer; and

at least one of: (i) the flexible substrate comprises polyethylene naphthalate, (ii) the diffusion barrier comprises tantalum, or (iii) the metal layer comprises aluminum.

18. The semiconductor device of claim 17, further comprising:

a mesa passivation layer between the amorphous silicon layer and the N+ amorphous silicon layer.

19. The method of any one of claims 9-12, wherein:

coupling the carrier substrate to the flexible substrate comprises coupling the carrier substrate to the flexible substrate with an adhesive configured so that upon adhesively coupling the carrier substrate to the flexible substrate, the flexible substrate is able to be decoupled from the carrier substrate by peeling the flexible substrate from the carrier substrate by hand; and

the method further comprises after baking the first dielectric material, decoupling the flexible substrate from the carrier substrate by peeling the flexible substrate from the carrier substrate by hand.

20. The semiconductor device of claim 17 or 18, further comprising:

a carrier substrate; and

an adhesive layer coupling the carrier substrate to the flexible substrate, the adhesive being configured so that upon adhesively coupling the carrier substrate to the flexible substrate, the flexible substrate is able to be decoupled from the carrier substrate by peeling the flexible substrate from the carrier substrate by hand.