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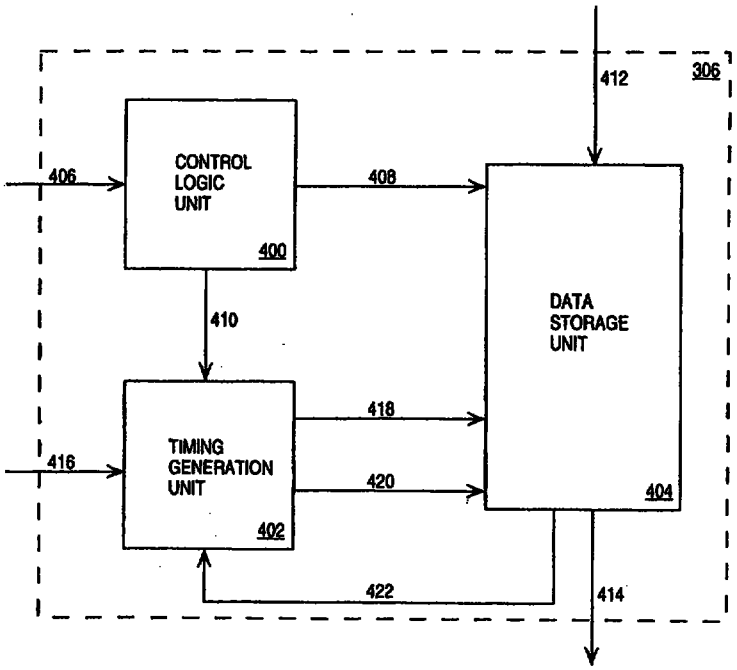
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(54) Title: HIGH FREQUENCY PIPELINE DECOUPLING QUEUE DESIGN



(57) Abstract

A method and apparatus for expediting the processing of a plurality of instructions in a processor. In one embodiment, said processor has a plurality of pipeline units to process a plurality of instructions. Each of said pipeline units has a plurality of pipeline stages (502). Further, a self–timed queue (306) is provided to decouple at least one of said pipe stages from another, wherein said self–timed queue supports both read and write operations triggered by non–overlapping read and write signals (902, 904) both occurring within the same single clock cycle (900) of said processor.