Chip-sized flip-chip semiconductor package and method for making the same.

The invention relates to a chip-sized flip-chip semiconductor package and to a method for assembling such a semiconductor package.

US 6 562 647 B2 shows a semiconductor package by which contacts are made to both sides of the dice manufactured on a wafer scale. The back side of the wafer is attached to a metal plate. The scribe lines separating the dice are saw cut to expose the metal plate but the cuts do not extend through the metal plate. After a metal layer is formed on the front of the dice, a second set of saw cuts are made coincident with the first set of saw cuts using a blade that is narrower than the blade used to make the first set of saw cuts.

The packaging of flip-chip semiconductor packages is known from Johnson et al IEEE Electronic Components and Technology Conference 1999 page 950 to 954 to be complex and time-consuming.

It is one object of the invention to provide a chip-sized flip-chip semiconductor package and a method to produce such a package simply and economically.

This object of the invention is solved by the subject matter of the independent claims. Further improvements arise from the subject matter of the dependent claims.

The present invention provides a chip-sized flip-chip semiconductor package comprising a semiconductor die with a plurality

of contact areas on its active surface. An electrically conductive bump or solder ball is connected to each contact area. The die and electrically conductive bumps are encapsulated in a plastic housing so that the plastic housing or mold material encapsulates sides of the die and sides of the electrically conductive bumps. The passive back side of the die remains uncoated. The electrically conductive bumps provide the external electrical connection of the device to, for example, a printed board or a re-distribution board.

The package according to the invention can be manufactured very cost effectively as it is produced by wafer-scale processing. This enables a large number of dies to be processed in one step. The encapsulation of the sides of the electrically conductive bumps, which are attached to the contact areas on the active surfaces of the dies, is advantageous as the plastic housing provides mechanical support to the electrically conductive bumps. Thus the reliability of the package is improved.

The plastic housing of the semiconductor package according to the invention preferably substantially fills the area between the electrically conductive bumps and the active surface of the die. Preferably the external ends of the electrically conductive bumps have a substantially flat surface and form a substantially flat surface adjacent to the outer substantially flat surface of the plastic housing of the package. The electrically conducting bumps preferably comprise solder, solder paste, electrically conductive paste or solder balls.

The substantially flat outer surface of the package including the substantially flat electrical connection areas is advanta-

geous. Firstly, the delicate electrical connections formed between the contact areas of the die and electrically conductive bumps are provided with mechanical support by the plastic encapsulation. The semiconductor package according to the invention is, therefore, more reliable.

The external electrical connections formed by the exposed ends of the electrically conductive bumps have an essentially flat surface forming essentially flat contact areas. In a conventional flip-chip package the solder balls protrude from the plastic housing. The outer essentially flat surface of the package including the essentially flat contact areas according to the invention is advantageous as it enables the package to be mounted onto the contact areas of a re-distribution board so that the gap between the package and board is virtually eliminated. This means that the problems associated with underfilling the mounted die during the encapsulation process are avoided. This leads to a much improved reliability of the package.

In one embodiment of the invention, the passive rear side of the die is not covered by mold material. This is advantageous if, for example, a heat spreading or heat dissipating device is to be attached to the package. The direct attachment of the heat spreader to the passive surface of the die leads to improved thermal contact and therefore improved heat dissipation.

Alternatively, the dies are completely encapsulated by the mold mass. This has the advantage of providing improved protection of the package from environmental effects. In this embodiment of the invention, an encapsulated chip-sized flip-

chip semiconductor package is mounted onto the printed board or re-distribution board.

The present invention also relates to methods of assembling such chip-sized flip-chip semiconductor packages.

The method comprises the steps of cutting a semiconductor wafer, which includes a plurality of semiconductor dies, to form an array of individual dies with the same lateral arrangement as they had previously within the wafer. Each die includes a plurality of contact areas on its active surface. The dies are preferably arranged in columns and rows in a square grid array in the wafer. This enables a simple sawing procedure to be used to separate the dies.

A first adhesive foil is then attached to the passive back side of the dies. A substrate including a plurality of electrically conductive bumps is provided. The electrically conducting bumps are deposited on the substrate by conventional processes.

The first adhesive foil including the dies and the substrate including the electrically conductive bumps are laterally aligned so that the electrically conductive bumps face, and are essentially vertically aligned with, the contact areas on the active surfaces of the dies. The first adhesive foil and the substrate are pressed together and heated to form connections between the contact areas on the die and the substrate. The pressure and heat are then removed and the first adhesive foil is removed from the passive surface of the dies.

In the next step of the process, the plurality of dies are embedded in a single mold mass so that at least sides of each die and sides of the electrically conductive bumps are encapsulated by the mold material of the mold mass. The mold material may comprise any plastic or molding compound.

The substrate is then removed from the mold mass. This exposes the ends of the electrically conductive bumps on the surface of the mold mass and forms the essentially flat contact areas of the package. A second adhesive foil is attached to the surface of the mold mass opposite the surface of the mold mass including the exposed electrically conductive bumps. The mold mass is then cut to form a plurality of chip-sized flip-chip semiconductor packages which are still attached to the second adhesive foil.

The semiconductor packages are tested, removed from the adhesive foil and mounted in packaging tape.

During the molding process according to the invention, the mold material of the mold mass preferably fills the areas between the solder balls, the active surface of the die and the upper surface of the substrate. In an alternative embodiment the mold mass additionally encapsulates the passive surface of the dies so that the die is completely encapsulated in the mold mass.

The connection of the electrically conductive bumps between the contact areas of the dies and the substrate is preferably formed by positioning the adhesive foil containing the dies over the substrate including the electrically conductive bumps. This arrangement is advantageous if the electrically

conducting bumps are not mechanically attached to the substrate. Alternatively, the substrate including the electrically conductive bumps is positioned over the adhesive foil containing the dies.

The lateral arrangement of the electrically conductive bumps is preferably a mirror image of the arrangement of the contact areas of the dies. This enables the arrangement of the contact areas of the dies to match the arrangement of the electrically conductive bumps on the substrate.

The substrate may comprise metal, ceramic or plastic. The adhesive foil may comprise an adhesive layer on a metal, ceramic or plastic sheet or plate as an alternative to conventional adhesive foil. During the pressing step of the process, additional plates may be positioned on one or both of the back surfaces of the adhesive foil or the substrate in order to provide a more homogeneous pressure.

The substrate is preferably chemically removed from the mold mass containing the plurality of embedded dies with electrically conductive bumps by, for example, an etching process. This is advantageous as mechanical stress on the electrically conductive bumps and mold mass is largely avoided. Alternatively, the substrate may be mechanically removed by, for example, a grinding process. This is advantageous if a thick substrate is used.

Alternatively, the first adhesive foil may be laterally stretched to increase the distance between the dies. This enables a thicker plastic coating on the sides of the packages and after they are separated from the mold mass. This enables

improved protection of the package. If a wafer saw is used to separate the packages from the mold mass, this embodiment allows a thicker saw blade to be used. This is advantageous as a thicker blade is more robust. Also the alignment of the saw blade between the dies of the packages is simplified.

As an alternative, the package may include electrical connections which protrude from the plastic housing. This alternative embodiment is fabricated using the method of the invention except that a substrate which includes recesses arranged in a mirror image of the arrangement of the contact areas is used. The electrically conductive bumps are then positioned at least partly in the recesses of the substrate. This method results in a package in which the electrically conductive bumps from contacts which protrude from the plastic housing of the package.

Wafer-sized processing is advantageous as the speed of the bonding process is significantly increased over a one die at a time methodology. Wafer-sized processing also reduces production costs, material wastage and a greater throughput in the manufacturing process can be achieved. A large quantity of dies, 100,000 or more is possible, can be bonded at the same time and productivity is significantly increased.

An embodiment of the invention will now be described by way of example with reference to the drawings.

Figure 1 shows a cross-sectional view of a semiconductor package assembled according to the method of the invention,

Figure 2 shows a top view of a semiconductor wafer including a plurality of dies,

Figure 3 shows the positioning of the dies of Figure 2 above a substrate including a plurality of solder balls,

Figure 4 shows the attachment of the solder balls of Figure 3 to the contact areas of the dies,

Figure 5 shows the encapsulation of the dies of Figure 4 in a single mold mass,

Figure 6 shows the removal of the substrate of Figure 5 from the mold mass,

Figure 7 shows the separation of encapsulated semiconductor packages of Figure 6 from the mold mass, and

Figure 8 shows the method step of Figure 7 for an alternative embodiment of the invention.

Figure 1 shows an encapsulated semiconductor package 10 assembled using the method of the invention. The package 10 includes a semiconductor die 2 with a plurality of contact areas 4 on its active surface. A solder ball 7 is mounted on each contact area 4. The die 2 and solder balls 7 are encapsulated in a plastic housing 11. The plastic housing 11 encapsulates the die 2 and the space 13 between the solder balls 7. The end surfaces of the solder balls 7 form a flat surface adjacent to the flat outer surface of the plastic housing 11. The flat external surfaces of the solder balls 7 form the external contacts of the package.

Figure 2 shows a semiconductor wafer 1 comprising a plurality of dies 2 arranged in a two-dimensional square grid array, defined by sawing grooves 3. For improved clarity, only one of the plurality of dies 2 and sawing grooves 3 are indicated by a reference number. Each die 2 includes one or more semicon-

ductor devices and a plurality of contact areas 4 on its active surface which cannot be seen in Figure 2. The wafer 1 is cut along the sawing grooves 3 to separate the wafer 1 into a plurality of dies 2 having the same lateral arrangement as they had previously within the wafer 1.

Figure 3 shows that a first adhesive foil 5 is then attached to the passive back side of the separated dies 2. The first adhesive foil 5 is orientated horizontally so that the contact areas 4 of the dies 2 face downwards. A substrate 6 which is laterally at least as large as the wafer 1 is provided with a plurality of solder balls 7 arranged on its upper surface. The lateral arrangement of the solder balls 7 substantially matches the arrangement on the contact areas 4 on the dies 2 when the first adhesive foil 5 is positioned over the substrate. The lateral arrangement of the solder balls 7 is substantially a mirror image of the lateral arrangement of the contact areas 4. The substrate 6 including the solder balls 7 is positioned beneath the first adhesive foil 5 including the semiconductor dies 2 so that the contact areas 4 of the dies 2 face and are positioned directly above the solder balls 7.

Figure 4 shows that in the next step of the process the first adhesive foil 5 including the dies 2 and substrate 6 including the solder balls 7 are brought together so that the upper surface of the solder balls 7 are in contact with the surface of the corresponding contact areas 4 and the substrate 6. Heat and a compressive force is applied so that the solder ball 7 is bonded to the contact area 4. This process or solder reflow is illustrated by a plurality of arrows 12 in Figure 4. The heat and force are removed, then the first adhesive foil 5 is

removed leaving an array of dies 2 bonded via the solder balls 7 to the substrate 6.

In the next step, Figure 5, the substrate including the attached dies 2 is covered by mold material to form a mold mass 8 so that the passive surface and sides of each die 2 and sides of solder balls 7 are encapsulated. The space 13 between the solder balls 7, active surfaces of the dies 2 and upper surface of the substrate 6 is also filled by the mold material of the mold mass 8. All of the attached dies 2 and the upper surface of the substrate 6 are covered by a single mold mass 8.

In the next step, shown in Figure 6, the substrate 6 is removed from the mold mass 8, which includes the encapsulated dies 2 and solder balls 7, by an etching process. The bottom surfaces of the solder balls 7, which were previously in contact with the substrate 6, are exposed in the bottom surface of the mold mass 8 by this process. The exposed surfaces of the solder balls 7 and the bottom surface of the mold mass 8 form a common essentially flat surface.

In the next step, shown in Figure 7, a second adhesive foil 9 is placed onto the upper surface of the mold mass 8. The mold mass is cut between the dies 2 to form separate encapsulated semiconductor packages 10 which are still attached to the second adhesive foil 9. In the next step the individual encapsulated chip-sized flip-chip semiconductor packages 10 are tested, removed from the adhesive foil 9 and packed into a packing tape. These steps are not illustrated by a Figure.

Figure 8 shows the method step of Figure 7 for an alternative embodiment of the invention. Semiconductor package 14 comprises a semiconductor die 2' which includes a plurality of contacts areas 4, which are not shown in the diagram, on its active surface. A solder ball 7 is attached to each contact area. In this embodiment of the invention, the plastic housing 11 of each semiconductor package 14 covers sides of the dies 2' and solder balls 7 and fills the space 13 between the solder balls 7 and active surface of the die 2'. The passive rear side of the die 2' is not covered by the plastic housing 11. The end surfaces of the solder balls 7 form a essentially flat surface adjacent to the essentially flat outer surface of the plastic housing 11.

In this alternative embodiment of the invention the method steps are the same as those shown in Figures 2 to 7 except that the passive back surface of the dies 2' is not encapsulated by a mold mass. The second adhesive foil 9 is attached to the passive back surface of the dies 2' and the mold mass cut between the dies 2' to form a plurality of packages 14 which are attached to the second adhesive foil 9.

The encapsulated or partially encapsulated chip-sized flip-chip semiconductor packages 10; 14 made by the method of the invention are then mounted on a conventional printed board or re-distribution board.

Claims

1. A method to assemble a semiconductor package (10; 14) comprising the following steps:
   - providing a semiconductor wafer (1) including a plurality of dies (2; 2'), each having a plurality of contact areas (4) on its active surface,
   - cutting the wafer (1) to form individual dies (2; 2'),
   - attaching a first adhesive foil (5) to the passive side of the dies (2; 2'),
   - providing a substrate (6) including a plurality of electrically conductive bumps (7) on its surface,
   - laterally aligning the first adhesive foil (5) including the dies (2; 2') and the substrate (6) including the electrically conductive bumps (7), so that the electrically conductive bumps (7) face and are essentially vertically aligned with the contact areas (4) on the active surfaces of the dies (2; 2'),
   - pressing the first adhesive foil (5) and the substrate (6) together and heating to form connections between the contact areas (4) on the dies (2; 2') and the substrate (6),
   - removing the first adhesive foil (5),
   - embedding the plurality of dies (2; 2') in a mold mass (8) so that at least sides of each die (2; 2') and sides of the electrically conductive bumps (7) are encapsulated by the mold mass (8),
   - removing the substrate (6) to expose the ends of the electrically conductive bumps (7) on the surface of the mold mass (8),
   - attaching a second adhesive foil (9) to the side of the mold mass (8) opposite the surface including the elec-

trically conductive bumps (7) or attaching a second adhesive foil (9) to the passive surfaces of the dies (2'),

- cutting the mold mass (8) to form encapsulated semiconductor packages (10; 14).

2. A method according to claim 1, characterised in that the semiconductor packages (10; 14) are tested, removed from second adhesive foil (9) and mounted in packaging tape.

3. A method according to claim 1, characterised in that the substrate (6) including the electrically conductive bumps (7) is positioned over the first adhesive foil (5) including the dies (2; 2').

4. A method according to claim 1, characterised in that the first adhesive foil (5) including the dies (2; 2') is positioned over the substrate (6) including the electrically conductive bumps (7).

5. A method according to claim 1, characterised in that the first (5) or second (9) adhesive foil comprises an adhesive layer on a metal, ceramic or resin foil or sheet.

6. A method according to claim 1, characterised in that

the first adhesive foil (5) including the dies (2; 2') is stretched to increase lateral separation of the dies (2;2').

7. A method according to claim 1, characterised in that the plastic housing (11) fills the area (13) between the electrically conducting bumps (7) and the active surface of the die (2;2').

8. A method according to claim 1, characterised in that the passive surface of the dies (2) is encapsulated by the mold mass (8).

9. A semiconductor package (10; 14) comprising the following features:
- a semiconductor die (2; 2') with a plurality of contact areas (4) on its active surface
- an electrically conductive bump (7) on each contact area (4),
- the die (2; 2') and electrically conductive bumps (7) being encapsulated in a plastic housing (11), the plastic housing (11) encapsulating at least sides of the die (2; 2') and sides of the electrically conductive bumps (7).

10. A semiconductor package (10; 14) according to claim 9, characterised in that the plastic housing (11) fills the space (13) between the electrically conducting bumps (7) and the active surface of the die (2;2').

11. A semiconductor package (10) according to claim 9 or claim 10,
characterised in that
the passive surface of the dies (2) is encapsulated by the mold mass (8).

12. A semiconductor package (10; 14) according to one of claims 9 to 11,
characterised in that
the end surface of the conductive lumps (7) forms a common substantially flat surface with the outer substantially flat surface of the plastic housing (11).

13. A semiconductor package (10; 14) according to one of claims 9 to 12,
characterised in that
the electrically conductive bumps (7) comprise solder balls.