

INTERCONNECT STRUCTURES WITH COBALT-INFUSED RUTHENIUM LINER AND A COBALT CAP**BACKGROUND**

[0001] The present invention generally relates to the field of complementary metal-oxide semiconductor (CMOS) devices, and more particularly to fabricating copper interconnect structures having a cobalt-infused ruthenium liner and a cobalt cap.

[0002] Typical components of an integrated circuit (IC) include transistors, capacitors, and the like. In semiconductor chip fabrication, these IC components are coupled by interconnect structures that conduct current through the different circuit layers. These interconnect structures typically take the shape of wires, trenches, or vias formed in dielectric layers above the microelectronic devices or metallization levels of the IC. Interconnect structures are typically formed by depositing a dielectric layer, etching a recess in the dielectric layer and filling the recess with a metal. Typically, interconnect structures are made of copper and can be formed using single-damascene or dual-damascene fabrication processes. In the single-damascene process, interconnect structures are manufactured independently, while in the dual-damascene process are manufactured at the same time.

[0003] Generally, interconnect structures are lined with a barrier layer located at the interface between the dielectric layer and the metal level underneath. The presence of the barrier layer can reduce electromigration (EM) problems in the IC. Electromigration may be defined as the material transport induced by the electron flow during operation under current, being the interface between the interconnect structure and the surrounding dielectric the primary path for the material transport in metal lines. In 7 nm technologies and beyond, a ruthenium (Ru) liner is used for better copper (Cu) fill. However, cobalt (Co) from the cobalt cap used to encapsulate the copper fill can diffuse into the ruthenium liner causing EM degradation, and thus representing a critical electromigration resistance (yield) concern for back-end-of-the-line (BEOL) technologies. Therefore, alternative designs and techniques for forming interconnect structures would be desirable.

SUMMARY

[0004] Shortcomings of the prior art are overcome and additional advantages are provided through the provision of a method for forming an interconnect structure that includes forming a recess within a dielectric layer, conformally depositing a barrier layer within the recess, and forming a cobalt-infused ruthenium liner above the barrier layer. The cobalt-infused ruthenium liner includes a first liner above the barrier layer and a second liner above the first liner. The first liner includes ruthenium while the second liner includes cobalt. Cobalt atoms from the second liner migrate to the first liner to form the cobalt-infused ruthenium liner. A conductive material is deposited above the cobalt-infused ruthenium liner to fill the recess, followed by the formation of a capping layer above a top surface of the conductive material, the capping layer including cobalt. The formation of the cobalt-infused ruthenium liner reduces a cobalt concentration gradient between the capping layer and the first liner that prevents cobalt migration

from the capping layer.

[0005] Another embodiment of the present invention provides an alternate method for forming an interconnect structure that includes forming a recess within a dielectric layer, conformally depositing a barrier layer within the recess followed by conformal deposition of a first liner above the barrier layer and a second liner above the first liner. The first liner includes ruthenium while the second liner includes cobalt. A third liner is subsequently formed above the second liner, the third liner including ruthenium. The migration of cobalt atoms from the second liner to the first liner and the third liner form a cobalt-infused ruthenium liner. A conductive material is formed above the cobalt-infused ruthenium liner to fill the recess followed by the deposition of a capping layer above a top surface of the conductive material, the capping layer includes cobalt. The formation of the cobalt-infused ruthenium liner reduces a cobalt concentration gradient between the capping layer and the first liner and third liner that prevents cobalt migration from the capping layer.

[0006] Another embodiment of the present invention provides a semiconductor structure that includes an interconnect structure within a dielectric layer, the interconnect structure includes a barrier layer located on a bottom surface and sidewalls of the interconnect structure, a first liner directly above the barrier layer, the first liner includes ruthenium, a second liner directly above the first liner, the second liner includes cobalt, a conductive material above the second liner substantially filling the interconnect structure, and a capping layer directly above the conductive material, the capping layer including cobalt, the migration of cobalt atoms from the second liner to the first liner reduces a concentration gradient between the capping layer and the first liner that prevents diffusion of cobalt atoms from the capping layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The following detailed description, given by way of example and not intended to limit the invention solely thereto, will best be appreciated in conjunction with the accompanying drawings, in which:

FIG. 1A is a cross-sectional view of a simplified semiconductor structure depicting forming recesses in a dielectric layer and depositing a barrier layer within the recesses, according to an embodiment of the present invention;

FIG. 1B is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a first liner above the barrier layer, according to an embodiment of the present invention;

FIG. 1C is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a second liner above the first liner, according to an embodiment of the present invention;

FIG. 1D is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a first conductive material above the second liner, according to an embodiment of the present invention;

FIG. 1E is a cross-sectional view of the simplified semiconductor structure after a planarization process, according to an embodiment of the present invention;

FIG. 1F is a cross-sectional view of the simplified semiconductor structure depicting first interconnect

structures including a first capping layer above the first conductive material, according to an embodiment of the present invention;

FIG. 2A is a cross-sectional view of the simplified semiconductor structure depicting forming recesses in the dielectric layer and depositing the barrier layer within the recesses, according to another embodiment of the present invention;

FIG. 2B is a cross-sectional view of the simplified semiconductor structure depicting the deposition of the first liner above the barrier layer and the deposition of the second liner above the first liner, according to another embodiment of the present invention;

FIG. 2C is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a third liner above the second liner, according to another embodiment of the present invention;

FIG. 2D is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a second conductive material above the third liner, according to another embodiment of the present invention;

FIG. 2E is a cross-sectional view of the simplified semiconductor structure after a planarization process, according to another embodiment of the present invention;

FIG. 2F is a cross-sectional view of the simplified semiconductor structure depicting second final interconnect structures including a second capping layer above the second conductive material, according to another embodiment of the present invention;

FIG. 3A is a cross-sectional view of the simplified semiconductor structure depicting forming recesses in the dielectric layer and depositing the barrier layer within the recesses, according to yet another embodiment of the present invention;

FIG. 3B is a cross-sectional view of the simplified semiconductor structure depicting the deposition of the first liner, second liner, and third liner, according to yet another embodiment of the present invention;

FIG. 3C is a cross-sectional view of the simplified semiconductor structure depicting removing horizontal portions of the first liner, second liner, and third liner, according to yet another embodiment of the present invention;

FIG. 3D is a cross-sectional view of the simplified semiconductor structure depicting the deposition of a second conductive material above the third liner, according to another embodiment of the present invention;

FIG. 3E is a cross-sectional view of the simplified semiconductor structure after a planarization process, according to yet another embodiment of the present invention;

FIG. 3F is a cross-sectional view of the simplified semiconductor structure depicting second final interconnect structures including the second capping layer above the second conductive material, according to yet another embodiment of the present invention;

[0008] The drawings are not necessarily to scale. The drawings are merely schematic representations, not intended to portray specific parameters of the invention. The drawings are intended to depict only typical embodiments of the invention. In the drawings, like numbering represents like elements.

DETAILED DESCRIPTION

[0009] Detailed embodiments of the claimed structures and methods are disclosed herein; however, it can be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. In the description, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments.

[0010] For purposes of the description hereinafter, terms such as "upper", "lower", "right", "left", "vertical", "horizontal", "top", "bottom", and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. Terms such as "above", "overlying", "atop", "on top", "positioned on" or "positioned atop" mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure may be present between the first element and the second element. The term "direct contact" means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary conducting, insulating or semiconductor layers at the interface of the two elements.

[0011] It will be understood that, although the terms first, second, etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the scope of the present concept.

[0012] In the interest of not obscuring the presentation of embodiments of the present invention, in the following detailed description, some processing steps or operations that are known in the art may have been combined together for presentation and for illustration purposes and in some instances may have not been described in detail. In other instances, some processing steps or operations that are known in the art may not be described at all. It should be understood that the following description is rather focused on the distinctive features or elements of various embodiments of the present invention.

[0013] Copper (Cu) has been used for many years in the fabrication of integrated circuit (IC) chips. Copper is a better conductor than aluminum (Al), and allows for metal components to be smaller. But, copper can cause problems if not properly contained within the interconnect structures. To properly contain copper, cobalt (Co) has been used in current 7 nm (nanometer) interconnects, both as a cobalt liner and as a cobalt cap for copper encapsulation. Unfortunately, movement/diffusion of cobalt has been linked with degraded electromigration lifetimes, particularly when the cobalt cap is combined with the ruthenium (Ru) liner typically used in 7 nm technologies to enhance copper fill.

[0014] Therefore, embodiments of the present invention provide a method and associated structure for fabricating

copper interconnect structures having a cobalt-containing ruthenium liner and a cobalt cap. The proposed embodiments prevent the diffusion of cobalt atoms from the cobalt cap to the ruthenium liner thereby improving electromigration performance. A way of preventing cobalt diffusion from the cobalt cap includes forming a tantalum nitride layer followed by a ruthenium liner and a substantially thin cobalt liner capable of saturating the underlying ruthenium liner with cobalt atoms to form the cobalt-containing ruthenium liner which may halt the driving force for cobalt diffusion from the cobalt cap. An embodiment by which the cobalt-containing ruthenium liner can be formed in copper interconnect structures is described in detailed below by referring to the accompanying drawings in FIGS. 1A-1F. Alternate embodiments by which the cobalt-containing ruthenium liner can be formed to prevent cobalt diffusion in copper interconnects are described in detailed below by referring to the accompanying drawings in FIGS. 2A-3F.

[0015] Referring now to FIGS. 1A-1F, cross-sectional views of a simplistically depicted semiconductor structure 100 during a sequence of processing steps are shown, according to an embodiment of the present invention. The sequence of processing steps shown in FIGS. 1A through 1F illustrate the formation of an interconnect structure 160 in the simplistically depicted semiconductor structure 100 (hereinafter "semiconductor structure").

[0016] With reference to FIG. 1A, at this step of the manufacturing process, the semiconductor structure 100 includes a dielectric layer 106 in which recesses 108 have been formed using standard etching techniques. For illustration purposes only, without intent of limitation, only two recesses 108 are depicted within the dielectric layer 106. As known by those skilled in the art, any number of recesses 108 can be formed depending on circuit design and/or requirements.

[0017] The dielectric layer 106 is typically formed above device or metal levels (not shown) of the semiconductor structure 100. Specifically, as known by those skilled in the art, a layer of dielectric material, such as the dielectric layer 106, is deposited above active regions (not shown) of the semiconductor structure 100 and then etched to form openings or recesses that will later be filled with a conductive material to form the interconnect structure(s).

[0018] The dielectric material forming the dielectric layer 106 may include, for example, a low-k dielectric material having a dielectric constant, k , in the range of approximately 2.4 to approximately 2.7. In some embodiments, the dielectric layer 106 may include silicon oxide, silicon nitride, hydrogenated silicon carbon oxide, silicon based low-k dielectrics, or porous dielectrics. The dielectric layer 106 may be formed by any suitable deposition process such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or the like.

[0019] As mentioned above, the dielectric layer 106 is etched to form the recesses 108. The recesses 108 can be formed using lithography and etch processing techniques typically used in single-damascene and dual-damascene processes. The recesses 108 may be shaped to accommodate a variety of interconnect structures (e.g., trenches, lines or vias). Typically, the recesses 108 may extend through the dielectric layer 106 to expose active regions (not shown) of the semiconductor structure 100. The recesses 108 are then filled with a conductive metal, as will be

described in detailed below.

[0020] As may be known by those skilled in the art, the recesses 108 shown in FIG. 1A has been etched into the dielectric layer 106 with a determined aspect ratio (H/D) of height (=H) to width (=D). In some embodiments, the range of aspect ratios varies from approximately 0.5 to approximately 20, with aspect ratios of 1 to 10 being preferred. However, in the actual device, there may be high aspect ratios (H/D) which are greater than 20:1.

[0021] With continued reference to FIG. 1A, a barrier layer 110 is deposited on horizontal and vertical surfaces of the dielectric layer 106. Stated differently, the barrier layer 110 is deposited on a bottom surface, sidewalls and top surfaces of the dielectric layer 106, as shown in the figure. The barrier layer 110 may include any barrier material suitable for preventing the diffusion of subsequently deposited metal layers (e.g., cobalt, ruthenium or copper) into the dielectric layer 106. More particularly, the barrier layer 110 may prevent the diffusion of atoms from the subsequently formed ruthenium and cobalt liners into the dielectric layer 106, acting also as an adhesion promoting layer so that the ruthenium and cobalt liners are bonded to the dielectric layer 106. Experimental results have shown that direct deposition of ruthenium on dielectric materials may produce poor adhesion and cause delamination related reliability problems.

[0022] According to an embodiment, the barrier layer 110 includes tantalum nitride (TaN). In other embodiments, the barrier layer 110 may include alternative metal nitrides including, for example, titanium nitrate (TiN), tungsten nitride (WN), or the like. Standard deposition process can be used to form the barrier layer 110. For example, in some embodiments, the barrier layer 110 can be formed via CVD, PVD, or atomic layer deposition (ALD) processes.

[0023] The barrier layer 110 may have a thickness varying from approximately 0.5 nm to approximately 5 nm and ranges there between, although a thickness less than 0.5 nm and greater than 5 nm may be acceptable.

[0024] The process continues by conformally depositing a first liner 120 directly above the barrier layer 110, as depicted in FIG. 1B. In a preferred embodiment, the first liner 120 is composed substantially of, if not entirely of, ruthenium (Ru) and can be formed by standard deposition processes such as PVD, CVD, electroless plating, evaporation, or any other deposition method that deposits conformal thin films. As described above, ruthenium-containing liners, such as the first liner 120, are used in 7 nm technologies and beyond to improve copper (Cu) fill. Specifically, liners including ruthenium may adhere better to the copper seed, enabling it to be more conformal (i.e., eliminating voids) and thinner.

[0025] The first liner 120 may have a thickness varying from approximately 0.5 nm to approximately 5 nm and ranges there between, although a thickness less than 0.5 nm and greater than 5 nm may be acceptable. In an embodiment, the first liner 120 may have a thickness of approximately 10 nm.

[0026] Following the formation of the first liner 120, a second liner 130 is formed directly above the first liner 120, as shown in FIG. 1C. The second liner 130 may include a very thin layer of a (metal) material conformally deposited on the first liner 120. In a preferred embodiment, the second liner 130 is composed substantially of, if not entirely of, cobalt (Co). Standard deposition processes such as PVD, CVD, electroless plating, evaporation, or any other deposition method that deposits conformal thin films can be used to form the second liner 130.

[0027] By forming the second liner 130 in direct contact with the first liner 120, cobalt atoms from the second liner 130 migrate to the first liner 120 (i.e., ruthenium liner) saturating the first liner 120 with cobalt such that there is no driving force for cobalt diffusion from a subsequently formed cobalt cap (e.g., first capping layer 156 in FIG. 1F). Therefore, depletion of the subsequently formed cobalt cap is prevented, which may in turn improve electromigration performance of the (first) interconnect structure(s) 160 (FIG. 1F).

[0028] It should be noted that, cobalt diffusion into the ruthenium liner (e.g., first liner 120) typically happens during thermal treatment(s) conducted on the semiconductor structure 100 during processing steps such as, for example, annealing or high temperature film deposition. Since the driving force for cobalt diffusion is the cobalt concentration gradient between the subsequently formed cobalt cap (e.g., first capping layer 156 in FIG. 1F) and the first liner 120 (i.e., the ruthenium liner), the incorporation of cobalt atoms from the second liner 130 into the first liner 120 reduces the cobalt concentration gradient between the cobalt cap and the first liner 120, thereby effectively suppressing or mitigating cobalt diffusion in the semiconductor structure 100.

[0029] A thickness of the second liner 130 may be less than the thickness of the first liner 120. According to an embodiment, the second liner 130 may have a thickness of less than approximately 5 nm. In other embodiments, the second liner 130 may have a thickness varying from approximately 0.1 nm to approximately 5 nm. In yet another embodiment, the second barrier liner may be thicker than the first liner 120.

[0030] With reference now to FIG. 1D, a first conductive material 142 may be conformally deposited directly above a top surface of the second liner 130. According to an embodiment, the first conductive material 142 includes copper (Cu). In some embodiments, the first conductive material 142 may further include dopants such as, for example, manganese, magnesium, copper, aluminum, or other known dopants. The first conductive material 142 may be formed by electroplating, electroless plating, PVD, CVD, or any combination thereof.

[0031] A thickness of the first conductive material 142 may be enough to entirely fill the remaining space within the recesses 108. However, in some cases, the thickness of the first conductive material 142 may exceed the depth of the recesses 108 as shown in FIG. 1D. In these cases, a planarization process can be conducted on the semiconductor structure 100 to remove areas of the first conductive material 142 exceeding the depth of recesses 108, as depicted in FIG. 1E.

[0032] As shown in FIG. 1E, excess portions of the first conductive material 142 may be removed from the

semiconductor structure 100 by any planarization method known in the art including, for example, chemical mechanical polishing (CMP). Additionally, during the planarization process, (horizontal) portions or areas of the barrier layer 110, first liner 120, and second liner 130 parallel to the dielectric layer 106 may also be removed.

[0033] The process continues with the formation of the first capping layer 156 depicted in FIG. 1F. The first capping layer 156 is composed substantially of, if not entirely of, cobalt (Co). The first capping layer 156 may be deposited by any suitable deposition process and may have a thickness varying from approximately 0.5 nm to approximately 5 nm. As known by those skilled in the art, the first capping layer 156 is typically used in back-end-of-the-line (BEOL) technologies for encapsulating the copper (Cu) in the first conductive material 142 reducing Cu electromigration in the interconnect structure 160 and improving the overall reliability of the semiconductor structure 100.

[0034] With continued reference to FIG. 1F, a final step in the formation of the first interconnect structures 160 is shown. According to an embodiment, each of the resulting first interconnect structures 160 includes the first barrier liner 120 directly above the barrier layer 110 and the (thin) second liner 130 directly above the first liner 120, the first conductive material 142 above the second liner 130 substantially filling the first interconnect structure 160 and the first capping layer 156 above a top surface of the first conductive material 142. This configuration may prevent cobalt diffusion from the first capping layer 156 to the first liner 120. By preventing the diffusion of cobalt atoms from the first capping layer 156, depletion of the first capping layer 156 can be avoided enhancing electromigration performance. More specifically, cobalt from the second liner 130 saturates the first liner 120 made of ruthenium forming a cobalt-infused ruthenium liner capable of halting the driving force for cobalt diffusion from the first capping layer 156 due to the reduced (cobalt) concentration gradient.

[0035] Referring now to FIGS. 2A-2F, cross-sectional views of the semiconductor structure 100 during an alternate processing sequence for forming an interconnect structure are shown, according to another embodiment of the present invention. The sequence of processing steps shown in FIGS. 2A through 2F illustrate an alternate method of forming second interconnect structures 260 in the semiconductor structure 100. The second interconnect structures 260 are formed similarly to the first interconnect structures 160 described above with reference to FIGS. 1A-1F. However, in this embodiment, after forming the second barrier liner 130 (FIG. 2B), a third barrier liner 240 is formed directly above the second barrier liner 130, as depicted in FIG. 2C.

[0036] As can be appreciated in FIG. 2C, in this embodiment, the second liner 130 is positioned between the first liner 120 and the third liner 240. According to an embodiment, the third liner 240 is made of substantially the same material as the first liner 120 (i.e., ruthenium) and can be formed using analogous deposition processes. The third liner 240 may have a thickness varying from approximately 0.5 nm to approximately 5 nm. As explained above, ruthenium-containing liners are typically used in advanced BEOL fabrication to enhance copper fill. However, the combination of ruthenium liners with cobalt caps (e.g., first capping layer 156 of FIG. 1F and second capping layer 256 of FIG. 2F) used for copper encapsulation has been linked with degraded electromigration lifetimes.

[0037] Therefore, by interposing the second liner 130 between the first liner 120 and the third liner 240, saturation of the first liner 120 and the third liner 240 by cobalt atoms from the second liner 130 can occur such that cobalt migration from the subsequently formed cobalt cap layer (e.g., capping layer 256 in FIG. 2F) can be prevented. Additionally, in this embodiment, the ruthenium (Ru)/copper (Cu) interface is maintained, enhancing copper fill performance for either copper plating or PVD copper reflow. Specifically, by depositing the third liner 240 above the second liner 130, the Ru/Cu interface remains after deposition of the second conductive material 242.

[0038] In some embodiments, after depositing the third liner 240, an etching process can be conducted on the semiconductor structure 100 to selectively remove horizontal portions of the first, second, and third liners 120, 130 and 240 from the dielectric layer 106, as depicted in FIG. 3C. Stated differently, portions of the first, second, and third liners 120, 130 and 240 parallel to the dielectric layer 106 are selectively removed by any suitable etching process. For example, an argon (Ar) plasma etching can be conducted to remove the horizontal portions of the first, second, and third liners 120, 130 and 240 from the semiconductor structure 100.

[0039] The removal of these portions of the first, second, and third liners 120, 130 and 240 exposes top (horizontal) surfaces of the barrier layer 110, as depicted in FIG. 3C. Stated differently, after the etching step of FIG. 3C, the first, second, and third liners 120, 130 and 240 remain only on opposing sidewalls of the second interconnect structures 260, as depicted in FIG. 3F. By performing this etching step (FIG. 3C), the resulting second interconnect structures 260 (FIG. 3F) may exhibit, in addition to reduced cobalt diffusion from the second capping layer 256, a reduced via resistance due to the absent of the first, second, and third liners 120, 130 and 240 on the bottom portion of the second interconnect structures 260.

[0040] With reference now to FIG. 2D, the process continues with the deposition of a second conductive material 242, similar to the first conductive material 142 in FIG. 1D. The second conductive material 242 may be made of analogous materials and deposited in similar ways as the first conductive material 142 (FIG. 1D). It should be noted that with or without the etching step depicted in FIG. 3C, the process continues with the deposition of the second conductive material 242.

[0041] As shown in FIG. 2E, excess portions of the second conductive material 242 may be removed from the semiconductor structure 100 by any planarization method known in the art including, for example, CMP. Additionally, during the planarization process, horizontal portions or areas of the barrier layer 110, first liner 120, second liner 130, and third liner 240 parallel to the dielectric layer 106 may also be removed from the semiconductor structure 100.

[0042] The process continues with the formation of the second capping layer 256 shown in FIG. 2F. The second capping layer 256 is composed of analogous materials and deposited in similar ways as the first capping layer 156 (FIG. 1F).

[0043] With continued reference to FIG. 2F, a final step in the formation of the second interconnect structures 260 is shown. According to an embodiment, each of the resulting second interconnect structures 260 includes the first liner 120 directly above the barrier layer 110 and the (thin) second liner 130 interposed between the first liner 120 and the third liner 240, the second conductive material 242 above the third liner 240 substantially filling the interconnect structures 260 and the second capping layer 256 above a top surface of the second conductive material 242. As explained above, this configuration may prevent cobalt diffusion from the second capping layer 256 to the ruthenium-containing liners (i.e., the first liner 120 and the third liner 240). By preventing the diffusion of cobalt from the second capping layer 256, depletion of the second capping layer 256 can be avoided enhancing electromigration performance. More specifically, cobalt atoms from the second liner 130 saturates the first and third liners 120, 240 made of ruthenium halting the driving force for cobalt diffusion from the second capping layer 256.

[0044] Therefore, embodiments of the present invention provide copper interconnect structures with enhanced electromigration performance. In an embodiment, the improved electromigration performance is achieved by forming a (thin) cobalt liner in direct contact with a ruthenium liner to form a cobalt-infused ruthenium liner caused by the migration of cobalt atoms from the cobalt liner to the ruthenium liner, this may in turn reduce the driving force for cobalt diffusion from the cobalt cap. In another embodiment, the thin cobalt liner is formed within or interposed between ruthenium liners, in these embodiments the Ru/Cu interface can be maintained further enhancing copper fill. In yet another embodiment, the cobalt/ruthenium liners can be removed from a bottom surface of the interconnect structures reducing via resistance in addition to the reduction in cobalt diffusion from the cobalt cap thereby further enhancing device performance and reliability.

[0045] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.