COMPOSITE STRUCTURE WITH HIGH HEAT DISSIPATION

FIELD OF THE INVENTION

This invention relates to a composite structure for optical, optoelectronic or electronic applications, comprising a support wafer and a layered structure comprising at least one layer made of a material chosen from among monocrystalline materials. In particular, such a composite structure is aimed to be a substrate for the formation of a monocrystalline useful layer, or is aimed to include such a monocrystalline useful layer, this useful layer including devices or components which cause a strong temperature increase in the useful layer during their operation.

BACKGROUND OF THE INVENTION

For this type of useful layer, it is clear that dissipation of heat released by components becomes a critical problem when the operating frequencies of these components and / or their degree of miniaturisation increase.

For example, there is the case of CMOS applications for which miniaturisation of components and reduction of the thickness of useful layers exacerbates heat dissipation problems, particularly in the case in which these useful layers are more or less thermally separated from the support substrate on

which they are formed. In particular, CMOS components made in SOI (Silicon-On-Insulator), SiGeOI (SiGe-On-Insulator), GeOI (Ge-On-Insulator) or SGOI (Si/SiGe-On-Insulator) structures can create problems with temperature rising (causing disturbances in the behaviour of components), particularly due to the fact that the oxide layer (typically forming the insulation for these structures) forms a thermal barrier between a substrate for example made of silicon, and the useful layer. For example, this type of SOI, SiGeOI, SGOI, GeOI structure may be made by Smart-Cut®, as described in US 2004/0053477.

For example, there is also the case of components operating at a high power frequency (typically more than 900 MHz) that can cause temperature rises that could disturb or even damage them. To overcome this disadvantage, the useful layers are normally made of a nitride semiconductor with better charge carrying properties (high saturation rate of carriers at high voltage, high breakdown voltage, etc.) than materials such as AsGa. This is particularly true for HEMT (High Electron Mobility Transistor) transistor type components. To form this type of nitride semiconductor based layers, growth supports made of monocrystalline bulk SiC, bulk <111> Si or bulk sapphire (Al_2O_3) are used, for which the lattice parameters are very similar to the lattice parameters of monocrystalline bulk <100> silicon.

However, the thermal impedances of <111> Si and sapphire are still too high for some high power frequency applications that require greater dissipation of released heat, and although monocrystalline bulk SiC is a reference material in terms of heat dissipation, this material is still too expensive.

US 6,328,796 and US 2003/0064735 documents disclose composite structures made by bonding thin layers to support wafers made of polycrystalline materials chosen for their thermal, electrical conductivity and thermal expansion properties (such as polycrystalline SiC substrates), by means of a bonding layer made of a dielectric material with the function of improving bond between the

thin layer and the support wafer and to encourage the appearance of possible compliance phenomena.

However, the materials and dimensions of the different layers and support wafers, and methods of manufacturing the structure, are chosen so as to satisfy physical specifications such as thermal conduction, electrical conduction and thermal expansion. Therefore, to satisfy these various specifications, a choice of a structure that implies compromise solutions, cannot give complete satisfaction. Therefore, composite structures described in these documents are not optimised for high power frequency applications requiring strong thermal dissipation.

A first purpose of the invention is to propose a composite structure with good thermal dissipation.

A second purpose of the invention is to propose such a composite structure manufactured in such manner that its economic cost is lower than the economic cost of a structure made of monocrystalline bulk SiC, and that it is available in sizes larger than 3 inches.

A third purpose of the invention is to improve the operation of miniaturised HEMT or CMOS components at a low cost.

A fourth purpose of the invention is to make a structure for HEMT applications with good thermal conductivity and a semi-insulating electrical characteristic (i.e. highly resistive).

SUMMARY OF THE INVENTION

According to a first aspect, the invention proposes a composite structure for applications in optics, optoelectronics or electronics, comprising a support wafer and a layer made of a material chosen from among monocrystalline materials and a layer made of a dielectric material, characterised in that the materials from which the support wafer is made, the layer made of monocrystalline material and the dielectric layer are chosen, and the thickness of each layer is adjusted, such that the thermal impedance of the composite

structure is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure.

Note that the thermal impedance of a structure ϕ is calculated from the thermal resistivities R_i of the different layers i of the structure ($\phi = 1/\sum_i R_i$). The thermal resistivity of a material is defined by its increase in °C, or in °K, over a 1 square metre surface area (the surface area of the layer or substrate considered) per input power in Watts. The thermal resistivity is also equal to the ratio between the thickness of the layer (or the substrate) considered, and the thermal conductivity of the material used.

This composite structure includes the following other characteristics:

- the support wafer is made of a material with a significantly lower thermal impedance than the thermal impedance of monocrystalline bulk silicon;
- the material from which the support wafer is made also has an electrical resistivity of more 10^4 ohms.cm;
- the support wafer is made of polycrystalline bulk SiC, polycrystalline bulk AlN or ceramic;
- the thickness of the layer made of dielectric material and the thickness of the layer made of monocrystalline material are chosen such that the thermal impedance of the composite structure is, between the ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a crystalline bulk SiC wafer with the same dimensions as the composite structure;
- the dielectric material is SiO_2 and / or Si_3N_4 and / or $Si_xO_yN_z$;
- the thickness of the layer made of a dielectric material is chosen to be less than about 0.20 micrometre, and possibly more than about 0.02 micrometre, the thickness of the layer made of a monocrystalline material then being chosen as a function of this thickness such that the thermal impedance of the composite structure is, between ambient temperature at 600°K, less than or

equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure;

- the material in the layer made of a monocrystalline material is chosen from among semiconductor materials so as to be able to form electronic components;
- the monocrystalline material is Si, SiGe or Ge;
- the layer made of a semiconductor material comprises at least one CMOS type electronic component;
- the monocrystalline material in the layer made of a monocrystalline material is chosen so that a monocrystalline nitride semiconductor can be successfully grown, the composite structure thus acting as a substrate for the growth of this nitride semiconductor, and to have an electrical resistivity of more than about 10^4 ohms.cm;
- the said monocrystalline material is SiC, <111> Si, or GaN;
- the thickness of the layer of monocrystalline material is more than a threshold thickness of about 0.06 micrometre, and possibly less than about 1 micrometre;
- the support wafer is made of polycrystalline SiC; the layer of monocrystalline material is made of <111> Si and its thickness is chosen between 0.2 and 1 micrometre; and the layer of dielectric material is made of SiO_2 and its thickness is about 0.2 micrometre;
- the support wafer is made of polycrystalline SiC; the layer of monocrystalline material is made of <111> Si and its thickness is chosen between 0.06 and 1 micrometre; and the layer of dielectric material is made of SiO_2 and its thickness is about 0.05 micrometre.

According to a second aspect, the process according to the invention proposes a hybrid structure, comprising the said composite structure and an upper monocrystalline structure on top of the monocrystalline material layer, the material(s) forming the upper structure being adapted to make the quality of the

layer of nitride semiconductor to be formed on the hybrid structure better than in the case in which the nitride semiconductor layer was formed directly on the layer made of monocrystalline material.

Other characteristics of this hybrid structure include:

- the layer of monocrystalline material is made of SiC, <111> Si, or GaN, the upper structure comprises a layer made of a material chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$;
- the concentration of at least one of the alloy elements chosen from among the alloys $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $O \leq x \leq 1$ and $O \leq y \leq 1$, varies progressively through the thickness.

According to a third aspect, the invention proposes a structure to be applied in HEMTs, comprising the said composite structure or the said hybrid structure, and an over-epitaxied layer made of monocrystalline GaN.

According to a fourth aspect, the invention proposes a process for manufacturing a composite structure starting from a donor wafer comprising a monocrystalline material, comprising the following steps:

(a) bonding a support wafer to the donor wafer;

(b) reduction of the donor wafer so as to only leave a remained structure on the support wafer, including the said monocrystalline material in the form of a layer, the nature and thickness of the material being such that the thermal impedance of the composite structure thus formed is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure.

Other characteristics of the process for manufacturing a composite structure are as follows:

- the said process also comprises a choice of a bulk material for the support wafer for which the thermal impedance is significantly less than the

thermal impedance of monocrystalline bulk silicon between ambient temperature and 600°K;

- the support wafer is chosen to be made of polycrystalline bulk SiC, polycrystalline bulk AlN or ceramic;
- step (a) includes the formation of a bonding layer made of a dielectric material between the support wafer and the donor wafer, such that the thickness of this bonding layer is less than a maximum thickness above which the thermal impedance of the composite structure is not, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure;
- the said process also comprises a step, before step (a), of implantation of atomic species under the bonding surface of the donor wafer at a determined depth so as to form a zone of weakness in it, and step (b) comprises energy input so as to detach the remained structure from the donor wafer at the zone of weakness, the implantation depth being determined such that the zone of weakness and the bonding surface together define the remained structure;
- step (b) is applied by mechanical and / or chemical means capable of reducing the thickness of the donor wafer;
- the donor wafer is made of monocrystalline bulk material, and step (b) is implemented so as to only keep a layer of the donor wafer with a thickness chosen such that the thermal impedance of the composite structure formed is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as a composite structure;
- the donor wafer is made of monocrystalline bulk Si or monocrystalline bulk Ge;
- the donor wafer is made of monocrystalline bulk Sic;

- the donor wafer initially comprises the said layer made of monocrystalline material and an adapted growth substrate, and the process also comprises a step before step (a) to form the donor wafer including crystalline growth of the layer made of monocrystalline material on the adapted growth substrate;

- the growth substrate comprises bulk Si or bulk Ge and a buffer layer made of SiGe, and the layer made of monocrystalline material is of <100> Si or SiGe;

- the growth substrate includes bulk sapphire (Al_2O_3), monocrystalline bulk SiC, bulk ZnO or bulk <111> Si, and the layer made of monocrystalline material is made of SiC, <111> Si, GaN, AlN, InN, $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{1-x}N$ where $O \leq x \leq 1$ and $O \leq y \leq 1$;

According to a fifth aspect, the invention proposes a process for manufacturing a hybrid structure comprising production of a composite structure according to the said process for manufacturing a composite structure, further comprising crystalline growth of an upper monocrystalline structure on the layer made of a monocrystalline material such that the configuration of the upper structure and the materials from which it is composed enable making a layer of nitride semiconductor layer with a better quality than it would have been if the nitride semiconductor were made directly on the layer made of a monocrystalline material.

Other characteristics of the process for manufacturing a composite structure include:

- the upper structure comprises a layer chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$;

- the upper structure comprises a layer chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y$

≤ 1, the concentration of at least one of the elements in the chosen alloy varying progressively through the thickness.

Other characteristics, purposes and advantages of the invention will become clearer after reading the following detailed description of the invention, given as a non-limitative example with reference to the appended figures, wherein:

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 diagrammatically shows a first composite structure according to the invention.

Figure 2 diagrammatically shows a second composite structure according to the invention.

Figure 3 diagrammatically shows a third composite structure according to the invention.

Figure 4 diagrammatically shows a fourth composite structure according to the invention.

Figures 5a to 5e show steps in the method of production of a composite structure according to the invention.

Figures 6 and 7 show the results of simulations of thermal behaviours made on different GaN supports, including a composite structure according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1, 2, 3 and 4 show four examples of composite and hybrid structures according to the invention, each intended for use in optical, optoelectronic or electronic applications. Each composite structure 40 comprises a support wafer 20 and a monocrystalline layer 11 made of a material chosen from among monocrystalline materials.

The material(s) forming the support wafer 20 is (are) chosen mainly for its (their) high thermal conductivity properties (high thermal conductivity means conductivity significantly greater than the conductivity of monocrystalline bulk <100> silicon). The material from which the support wafer 20 will be chosen will be a material with a thermal conductivity such that its thermal impedance is, between ambient temperature and 600°K, significantly less than or equal to 30% more than the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure. In this case, monocrystalline bulk SiC is a reference in the field of thermal conductivity of crystalline materials, its thermal conductivity typically being about 440 W/m.°K at ambient temperature (i.e. 300°K), within $\pm$20% depending on the quality and structure of the material. It can also be chosen to use the thermal conductivity of 6H-SiC (about 490 W/m.°K), or 4H-SiC (about 370 W/m.°K), or 3C-SiC (about 360 W/m.°K), as the reference thermal conductivity.

The choice of material for composition of the support wafer 20 also depends on economic cost constraints of the material (the cost must be significantly lower for monocrystalline bulk SiC), and availability and size constraints. In terms of size, a support wafer 20 larger than 3 inches might be required.

In particular, we might also choose a support wafer 20 made of polycrystalline SiC, polycrystalline AlN or a thermally adapted ceramic.

It would also be advantageous, particularly in HEMT applications, to choose a support wafer 20 with high resistivity, in other words more than 10^4 ohms.cm.

The support wafer 20 is covered by a monocrystalline layer 11 for which the component material(s) is (are) chosen, and for which the thickness is adjusted such that the thermal impedance of the complete composite structure 40 including the support wafer 20 is less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same

dimensions as the composite structure 40 between ambient temperature and 600°K (typical operating temperatures of high power frequency components). In particular, the thickness of the monocrystalline layer 11 could be chosen to be more than a threshold thickness, below which the impedance of the composite structure would not be less than or equal to about 1.3 times the thermal impedance of a wafer made of monocrystalline bulk SiC with the same dimensions as the composite structure 40 between ambient temperature and 600°K. In particular, this threshold thickness may be about 0.06 µm for materials such as Si, SiGe, Ge, <111> Si or GaN. For example, we could choose a monocrystalline layer 11 with a thickness between the threshold thickness and 1 µm.

According to a first configuration of the composite structure 40 according to the invention, the monocrystalline structure 11 is designed to be fitted with electronic, optical or optoelectronic components such as CMOS type transistors. In this case, the materials chosen for the monocrystalline layer 11 may be made of Si, SiGe or Ge. In this case, the components that will be formed in the monocrystalline layer 11 or that are already formed in the monocrystalline layer 11, will benefit from the particular structure of the composite structure 40 to evacuate the large amount of heat that they will release during operation, thus reducing risks of disturbance or even deterioration.

According to a second configuration, the composite structure 40 is a substrate for the formation of a useful layer composed of a material capable of including components operating at high power frequency, such as a nitride semiconductor (for example GaN). The materials chosen to form the monocrystalline layer 11 may then for example be SiC, <111> Si, or GaN, AlN or other nitride semiconductors. These materials are also chosen to have a high electrical resistivity (more than 10^4 ohms.cm). When the useful layer has been formed, the composite structure 40 according to the invention can then be used to dissipate large quantities of heat released by the components, particularly in

the case in which these components operate at a high power frequency, which is the case for example for HEMT transistors.

Preferably, and with reference to Figures 2 and 4, the layered structure 10 also comprises an insulating layer 13 made of a dielectric material such as SiO_2 and / or Si_3N_4 and / or $Si_xO_yN_z$, and arranged at the interface with the support wafer 20. This insulation layer 13 may be particularly useful when making this composite structure 40 (as described later) because it is chosen to have interesting bond properties when the composite structure 40 is made using a bonding technique. Furthermore, the material from which this insulating layer 13 is made can be chosen to have a large electrical resistivity, which may be an important advantage during operation of HEMT power components. The thickness of the insulating layer 13 is chosen to be less than a threshold thickness above which the thermal impedance of the composite structure is not, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure 40. The choice of thicknesses for the insulating layer 13 and for the monocrystalline layer 11 may be made one before the other, or using a method by successive approximations.

In particular, the thickness of the monocrystalline layer 11 may be adapted such that its free surface is at a given distance from the insulating layer 13. This insulating layer 13, even if it is chosen to be thin remains a thermal barrier that can introduce heat dissipation problems during operation of components included within a useful layer epitaxied on the monocrystalline layer 11. Therefore, moving the epitaxied surface (i.e. the surface of the monocrystalline layer 11) away from the buried insulation layer 13 thus improves heat dissipation.

Figure 1 shows a first composite structure 40 according to the invention, in which the layered structure 10 is composed only of the monocrystalline layer 11 directly in contact with the support wafer 20. In this configuration, the main

parameters that have to be adjusted are materials chosen to form the support wafer 20 and the monocrystalline layer 11, and the thickness of the monocrystalline layer 11 such that the thermal impedance of this composite structure 40 is less than or equal to 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure 40, between ambient temperature and 600°K.

We can thus choose a monocrystalline layer 11 with a thickness of between 0.06 and 1 µm.

Figure 2 shows a second composite structure 40 according to the invention in which the layered structure 10 is composed of a monocrystalline layer 11 and a layer of dielectric material 13 between the support wafer 20 and the monocrystalline layer 11. The thickness of this insulating layer 13 is chosen to be less than a threshold thickness above which the thermal impedance of the composite structure would no longer be less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure 40 between ambient temperature and 600°K, obviously considering that the materials chosen for the support wafer 20 and the monocrystalline layer 11, and the thickness of the monocrystalline layer 11, are already established.

Thus, the thickness of the insulating layer 13 may be between 0.02 µm and 0.2 µm.

For example, the component material could be chosen to be SiO_2 and / or Si_3N_4 and / or $Si_XO_yN_z$.

Knowing this, we could also choose a monocrystalline layer 11 with a thickness of between 0.06 and 1 µm.

For example, the following composite structure 40 would be possible:

- the support wafer 20 is made of polycrystalline SiC;
- the layer of monocrystalline material 11 is made of <111> Si, and its thickness is chosen to be between 0.2 and 1.0 micrometre; and

- the dielectric material layer (13) is made of SiO_2 and its thickness is about 0.20 micrometre.

For example, the following composite structure 40 would be possible:

- the support wafer 20 is made of polycrystalline SiC;
- the layer of monocrystalline material 11 is made of <111> Si, and its thickness is chosen to be between 0.06 and 1.0 micrometre; and
- the dielectric material layer (13) is made of SiO2 and its thickness is about 0.05 micrometre.

With reference to Figures 3 and 4, a hybrid structure 50 is made by adding an upper structure 12 to the layered structure 10 on the monocrystalline layer 11, the material(s) forming this upper structure 12 being adapted to improve the quality of a layer of crystalline material to be formed on the hybrid structure 50. Therefore these hybrid structures 50 are particularly well-arranged to act as a substrate for the crystalline growth of a useful layer made of a material adapted to high power frequencies, such as a nitride semiconductor such as GaN. In this case, the nature and configuration of the upper structure 12 are chosen to improve the quality of the useful layer to be formed compared with the case in which this useful layer is formed directly on the monocrystalline layer 11, adapting a lattice parameter starting from the composite structure 40 so as to become closer to the lattice parameter of the useful layer to be formed (thus particularly avoiding the creation of an excessive density of dislocations, and generated in a useful layer that would be constrained to resist excessive lattice mismatches with its growth support). For example, we could choose an upper structure 12 similar or equivalent to buffer structures divulged in documents US 2003/136333 and US 6,617,060, namely an upper structure 12 comprising at least one layer made of $Al_xIn_yGa_{(1-x-y)}N$, $In_xGa_{1-y}N$, or $Al_xGa_{1-x}N$ (where x is between 0 and 1 and y is between 0 and 1), with a layer with a composition that does not vary within its thickness and / or a layer with a composition that varies progressively within the thickness according to the most technically and

economically attractive configurations. This upper structure 12, made so that a high quality useful layer can be formed later, also means that this useful layer can be moved further away from the interface with the support wafer 20, which has an advantage in the case (with reference to Figure 4) in which an insulating layer 13 is interfaced with the support wafer 20 (this insulating layer 13 may slow down dissipation of heat if its thickness is greater than a threshold thickness).

Different steps of a process for manufacturing a composite structure 40 according to the invention are shown in Figures 5a to 5e.

Figure 5a shows a donor wafer 30, this donor wafer 30 comprising a monocrystalline material.

According to a first configuration, the donor wafer 30 may be composed of a monocrystalline bulk material.

If it is required to make a composite structure 40 for a CMOS type application, we could thus choose a donor wafer 30 made of <100> Si or monocrystalline bulk Ge.

If it is required to make a composite structure 40 acting as a substrate for crystalline growth of a subsequent layer made of nitride semi-conductor, we could choose a monocrystalline SiC or monocrystalline <111> Si material.

According to a second configuration, the donor wafer 30 initially comprises a growth substrate adapted to growth of a layer of monocrystalline material to be transferred. This growth substrate typically comprises a support made of a monocrystalline bulk material.

We could thus have a growth substrate made of sapphire (Al_2O_3), SiC, bulk ZnO or monocrystalline bulk <111> Si, and we could form a layer made of an SiC, <111> Si, GaN, AlN, InN, $Al_xIn_yGa_{(1-x-y)}$, $In_yGa_{(1-y)}N$, or $Al_xGa_{1-x}N$ monocrystalline material layer, where $0 \leq x \leq 1$ and $0 \leq y \leq 1$.

This growth substrate may further comprise an intermediate structure between the support and the layer made of monocrystalline material to be transferred, this intermediate structure acting as a buffer structure, and possibly

being arranged so as to compensate for differences of thermal expansion and / or differences of lattice parameters and / or to confine defects. Thus for example, we could make a monocrystalline layer made of <100> Si, or relaxed SiGe, forming it by crystalline growth on a buffer layer made of SiGe, the composition of the buffer layer varying progressively through its thickness starting from a support made of <100> Si or monocrystalline bulk Ge.

With reference to Figure 5b, the donor wafer 20 is then implanted by atomic species according to the dosing and energy conditions determined so as to form an area of weakness 35 at a determined depth in the donor wafer 30 with a determined mechanical weakening. For example, we could implant atomic species such as hydrogen ions, with between 5×10^{16} and 8×10^{16} atoms per square centimetre implanted at an energy of between 10 and 200 keV.

The depth of the zone of weakness 35 is chosen so as to define a material thickness (between the zone of weakness 35 and the surface of the donor wafer 30 that will be bonded to a support wafer 40 according to the step shown on Figure 5c) that includes at least part of the layered structure (not shown) to be transferred onto the support wafer 20. In particular, this implantation is applied such that the layered structure thus delimited includes a monocrystalline material in the form of a layer and for which the nature and thickness of each layer composing it are such that the thermal impedance of this composite structure 40 to be formed (including this layered structure after transfer and the support wafer 20 to be bonded) is, between ambient temperature and 600°K, less than or equal to 1.3 times the thermal impedance of monocrystalline bulk SiC.

Optionally, an insulating layer 13 is formed on the implantation surface before or after this implantation. For example, this insulating layer 13 may be an oxide (SiO_2) and / or a nitride (Si_3N_4 and / or $Si_xO_yN_z$) with a thickness such that the thermal impedance of the composite structure 40 to be formed (see Figure 5e) is less than or equal to about 1.3 times the thermal impedance of

monocrystalline bulk SiC between ambient temperature and 600°K. For example, we could form a layer of SiO_2 and / or Si_3N_4 and / or $Si_xO_yN_z$ with a thickness varying from 0.02 µm to 0.2 µm.

The bond surface (i.e. the surface on which this implantation was done) of the donor wafer 30 is then optionally prepared for bonding. It may thus be cleaned to eliminate contaminants (metallic, particulate, hydrocarbon element) and to make the surface more hydrophilic, mechanochemically polished, activated by plasma, etc. Optionally, if we have formed an insulating layer 13 on the implantation surface, the insulating layer may be completely removed during this cleaning step.

With reference to Figure 5c, a support wafer 20 is put into contact with the donor wafer 30 at the implanted surface.

Preferably, an insulating layer was previously formed on the surface of the support wafer 20 that is to be bonded. In all cases, the thickness of the insulating layer 13 between the support wafer 20 and the donor wafer 30 is chosen so as not to form an excessive thermal barrier to heat dissipation, in other words the thickness of the wafer is chosen such that the thermal impedance of the composite structure 40 to be formed (see Figure 5e) is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure 40.

Before bringing the support wafer 20 and the donor wafer 30 into contact, the bond surface of the support wafer 20 was prepared for bonding for example by applying cleaning treatments to make it more hydrophilic and / or to remove contaminants.

Optionally, other preparations of the two surfaces to be bonded may be used, such as CMP (Mechanochemical Planarisation) or plasma activation in order to improve the bond energy.

The donor wafer 30 and the support wafer 20 thus prepared may possibly be brought into contact at ambient temperature.

Once the two substrates have been bonded, the bond can be reinforced by inputting thermal energy, for example by baking at more than 200°C for 2h00. With reference to Figure 5d, energy is added on such that weak bonds located at the zone of weakness 35 will break and that a remained structure 36 is detached from it, this remained structure 36 then remaining bonded to the support wafer 20.

This remained structure 36 at least partly comprises the layered structure 10 to be formed on the support wafer 40. The energy supplied may be thermal and / or mechanical, this technique for transferring the layers then being well known to those skilled in the art under the expression Smart-Cut®, and is described particularly in "Silicon-On-Insulator technology: Material to LVSI, 2nd edition" by J-P Colinge (Kluwer Academic Publishers, p. 50 and 51).

According to one variant, the donor wafer 30 can be reduced from the structure shown in Figure 5c by a technique other than Smart-Cut®, the steps preceding the bonding and bonding itself then being the same as those presented above, except for the implantation (shown in Figure 5b). This other technique for reducing the donor wafer 30 uses mechanical thinning (polishing, lapping, etc.) and / or dry chemical etching on the back face until the determined thickness is reached, which may be a few tens of microns. Different mechanochemical polishing steps can then be used to thin the donor wafer 30 to only leave the remained structure 36 like that shown on Figure 5d. Regardless of the technique used for reducing this donor wafer 30, a surface finishing step is applied for the remained structure 36 in order to remove any roughness and contaminants on the surface.

This detachment surface may be prepared to become an "epi-ready" surface (namely ready to receive elements to be epitaxied), for example using CMP and / or wet or dry chemical etching (for example by RIE plasma).

We could also use techniques for selectively removing material, such as a selective chemical etching. In this respect, we could then provide a stop layer for this selective material removal in the remained structure 36. Optionally, this stop layer could then be removed in order to obtain a final layered structure 10 with good surface quality with little roughness (see Figure 5e).

With reference to Figure 5e, the final result is a composite structure 40 according to the invention comprising a layered structure 10 comprising the remained structure 36 and possibly the insulating layer 30, according to the composite structure 40 shown in Figure 1 or 2.

Eventually, and after this transfer of the remained layer 36 from the donor wafer 30 onto the support wafer 20, a crystalline growth of a monocrystalline upper structure 12 on the layered structure 10 may be applied so as to obtain one of the hybrid structures 50 shown in Figures 3 and 4.

Example 1:

The applicant performed comparative studies for composite structures according to the invention including a support wafer 20 made of polycrystalline SiC, and a layered structure 10 composed of monocrystalline layer 11 made of <111> silicon and an insulating layer 13 made of SiO_2. In this case, the resistivity of the support wafer 20 made of polycrystalline SiC was greater than 10^5 Ohm/cm. These composite structures 30 were made using Smart-Cut® (for which the main steps were illustrated with reference to Figures 5a to 5e).

The comparative study made by the Applicant consisted of simulating the thermal behaviour of such a composite structure 40 when it supports a GaN layer including HEMT components in operation, compared with other types of supports of the same layer of GaN.

One purpose of this study is to know how the temperature in the GaN layer is influenced by the different parameters such as the thickness of the

insulating layer 13, the thickness of the monocrystalline layer 11, the nature of the support wafer 20, and the power dissipated by HEMT components.

The results are given in Figures 6 and 7.

Figure 6 contains a graph showing the estimated surface temperature Ts (normalised in the figure) at the component (i.e. under the component grid), depending on the support type chosen for the GaN layer. Thus:

- the support I is made of monocrystalline bulk SiC;
- the support II is made of polycrystalline bulk SiC,
- the support III is made of <111> Si / SiO2 / polycrystalline bulk SiC,
- the support IV is a support made of monocrystalline bulk <111> Si

All these supports (I, II, III, IV) had the same dimensions.

Curve 1 (in dotted lines) shows the case in which the applied power is 5 W/mm, curve 2 (dashed lines) the case in which the applied power is 10 W/mm, curve 3 (continuous lines) the case in which the applied power is 15 W/mm, which are powers typically dissipated by a power component.

The composite structure 40 according to the invention (represented as configuration III on the graph) comprises a layered structure 10 composed of a 2 µm thick monocrystalline layer made of <111> Si and a 1 µm thick insulating layer 13 made of SiO_2.

The results of this simulation show that a composite structure 40 according to the invention has much greater heat dissipation (of the order of 20 to 30%) than in the case of a support IV made of monocrystalline bulk silicon, and only of the order of 10 to 20% less than in the case of a support I made of monocrystalline bulk SiC, and the difference is even lower compared with a support II made of polycrystalline bulk SiC (depending on the powers applied to the useful layer of GaN). Therefore the temperature increase of a component in the GaN layer in the simulated composite structure is approximately the same as the temperature increase obtained on a monocrystalline bulk SiC substrate.

The Applicant deduced that these results implied a composite structure with a thermal impedance less than or equal to 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure 40 between ambient temperature and 600°K.

Even if this thermal impedance seems a little higher than the thermal impedance of an equivalent monocrystalline bulk SiC or even polycrystalline bulk SiC, it is satisfactory during operation of an HEMT transistor in GaN layers with high power frequencies.

Moreover, this composite structure 40 enables epitaxy of high quality GaN layers, unlike a support II made of polycrystalline SiC.

This composite structure 40 is further economically much more attractive than a support I made of monocrystalline SiC.

Figure 7 shows a simulation of the maximum temperature T (normalised) of a GaN layer when different powers are applied to it (shown on the abscissa), this useful layer of GaN having been formed on a composite structure 40 comprising a polycrystalline SiC support wafer and a 2 µm thick monocrystalline layer of <111> Si. This graph is a comparison between the case in which this composite structure 40 comprises a 1 µm thick SiO_2 insulating layer (curve 4) and the case in which it does not include such an insulating layer (curve 5).

The results of this simulation show that a thin insulating layer (less than 1 µm thick) does not significantly modify the thermal dissipation properties of the composite structure 40 (of the order of 0% for a power of 5 W/mm to 5% for a power of 15 W/mm).

The Applicant has thus demonstrated that a composite structure 40 can very well contain an insulating layer 13 without significantly attenuating its thermal dissipation properties.

CLAIMS

1. Composite structure for applications in optics, optoelectronics or electronics, comprising a support wafer and a layer made of a material chosen from among monocrystalline materials and a layer made of a dielectric material, characterised in that the component materials of the support wafer, of the layer made of monocrystalline material, and of the dielectric layer are chosen, and the thickness of each layer is adjusted, such that the thermal impedance of the composite structure is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure.

2. Composite structure according to claim 1, characterised in that the support wafer is made of a material with a significantly lower thermal impedance than the thermal impedance of monocrystalline bulk silicon.

3. Composite structure according to the preceding claim, characterised in that the material is also chosen to have an electrical resistivity of more than about 10^4ohms.cm.

4. Composite structure according to one of the preceding two claims, characterised in that the support wafer is made of polycrystalline bulk SiC, polycrystalline bulk AlN or ceramic.

5. Composite structure according to one of the preceding claims, characterised in that the said adjustment to the thickness of the layer of dielectric material was such that the thickness of the layer made of a dielectric material is less than or equal to a maximum thickness and that the

thickness of the layer made of monocrystalline material is greater than or equal to a threshold thickness.

6. Composite structure according to one of the preceding claims, characterised in that the dielectric material is SiO_2 and / or Si_3N_4 and / or $Si_xO_yN_z$.

7. Composite structure according to the preceding two claims, characterised in that the thickness of the layer made of a dielectric material is chosen to be less than about 0.20 micrometres, and in that the thickness of the layer made of a monocrystalline material is chosen as a function of this thickness of the layer made of a dielectric material, such that the thermal impedance of the composite structure is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure.

8. Composite structure according to the preceding claim, characterised in that the thickness of the layer made of a dielectric material is also chosen to be more than about 0.02 micrometre.

9. Composite structure according to one of claims 1 to 7, characterised in that the material in the layer made of a monocrystalline material is chosen from among semiconductor materials so as to be able to form therein at least one electronic component.

10. Composite structure according to the preceding claim, characterised in that the layer made of a monocrystalline material comprises at least one CMOS type electronic component.

11. Composite structure according to one of the preceding two claims, characterised in that the monocrystalline material is Si, SiGe, or Ge.

12. Composite structure according to one of claims 1 to 8, characterised in that the monocrystalline material in the layer made of a monocrystalline material is chosen so that a monocrystalline nitride semiconductor can be successfully grown, the composite structure thus acting as a substrate for the growth of this nitride semiconductor, and so as to have an electrical resistivity of more than about 10^4 ohms.cm.

13. Composite structure according to the preceding claim, characterised in that the said monocrystalline material is SiC, <111> Si, or GaN.

14. Composite structure according to claim 7 or 8 combined with claim 11 or 13, characterised in that the thickness of the layer of monocrystalline material is more than a threshold thickness of about 0.06 micrometre.

15. Composite structure according to the preceding claim, characterised in that the thickness of the layer of monocrystalline material is also chosen to be less than about 1 micrometer.

16. Composite structure according to claim 1, characterised in that:

- the support wafer is made of polycrystalline SiC;
- the monocrystalline material layer is made of <111> Si and its thickness is chosen to be between about 0.2 and about 1 micrometre, and
- the dielectric material layer is made of SiO_2 and its thickness is about 0.20 micrometre.

17. Composite structure according to claim 1, characterised in that:

- the support wafer is made of polycrystalline SiC;
- the monocrystalline material layer is made of <111 > Si and its thickness is chosen to be between about 0.06 and about 1 micrometre, and
- the dielectric material layer is made of SiO_2 and its thickness is about 0.05 micrometre.

18. Hybrid structure intended to be a substrate for the crystalline growth of a nitride semiconductor, comprising a composite structure according to one of the preceding claims and an upper monocrystalline structure on top of the monocrystalline material layer, the material(s) forming the upper structure being adapted to improve the quality of the layer of nitride semiconductor to be formed on the hybrid structure in comparison with the case in which the nitride semiconductor layer would have been formed directly on the layer made of monocrystalline material.

19. Hybrid structure according to the preceding claim, characterised in that the layer of monocrystalline material is made of SiC, <111> Si, or GaN, and in that the upper structure comprises a layer made of a material chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$.

20. Hybrid structure according to the preceding claim, characterised in that the concentration of at least one of the alloy elements chosen from among the alloys $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, varies progressively through the thickness.

21. Structure to be applied in HEMTs, comprising a composite structure according to one of claims 12 to 17 or a hybrid structure according to one of claims 18 to 20, and an over-epitaxied layer made of monocrystalline GaN,

22. Process for manufacturing a composite structure starting from a donor wafer comprising a monocrystalline material, comprising the following steps:

(a) bonding a support wafer to the donor wafer;

(b) reduction of the donor wafer so as to only leave a remained structure on the support wafer, including the said monocrystalline material in the form of a layer, the nature and thickness of the material being such that the thermal impedance of the composite structure thus formed is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a monocrystalline bulk SiC wafer with the same dimensions as the composite structure.

23. Process for manufacturing a composite structure according to claim 22, further comprising a choice of a bulk material for the support wafer for which the thermal impedance is, between ambient temperature and 600°K, significantly less than the thermal impedance of monocrystalline bulk silicon.

24. Process for manufacturing a composite structure according to the preceding claim, characterised in that the support wafer is chosen to be made of polycrystalline bulk SiC, polycrystalline bulk AlN or ceramic.

25. Process for manufacturing a composite structure according to one of claims 22 to 24, characterised in that step (a) includes the formation of a bonding layer made of a dielectric material between the support wafer and the donor wafer, such that the thickness of this bonding layer is

less than a threshold thickness above which the thermal impedance of the composite structure is not less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure between ambient temperature and 600°K.

26. Process for manufacturing a composite structure according to one of claims 22 to 25, further comprising a step, before step (a), of implantation of atomic species under the bonding surface of the donor wafer at a depth determined so as to form a zone of weakness in it, and in that step (b) includes energy input so as to detach the remained structure from the donor wafer at the zone of weakness, the implantation depth being determined such that the zone of weakness and the bonding surface together define the remained structure.

27. Process for manufacturing a composite structure according to one of claims 22 to 25, characterised in that step (b) is applied by mechanical and / or chemical means capable of reducing the thickness of the donor wafer.

28. Process for manufacturing a composite structure according to one of claims 22 to 27, characterised in that the donor wafer is made of monocrystalline bulk material, and step (b) is implemented so as to only keep a layer of the donor wafer with a thickness chosen such that the thermal impedance of the composite structure formed is, between ambient temperature and 600°K, less than or equal to about 1.3 times the thermal impedance of a wafer of monocrystalline bulk SiC with the same dimensions as the composite structure.

29 Process for manufacturing a composite structure according to the preceding claim, characterised in that the donor wafer is made of monocrystalline bulk Si or monocrystalline bulk Ge.

30. Process for manufacturing a composite structure according to claim 28, characterised in that the donor wafer is made of monocrystalline bulk Sic.

31. Process for manufacturing a composite structure according to one of claims 22 to 27, characterised in that the donor wafer initially comprises the said layer made of monocrystalline material and an adapted growth substrate, and in that the process also comprises a step before step (a) to form the donor wafer including crystalline growth of the layer made of monocrystalline material on the adapted growth substrate.

32. Process for manufacturing a composite structure according to the preceding claim, characterised in that the growth substrate comprises bulk Si or bulk Ge and a buffer layer made of SiGe, and in that the layer made of monocrystalline material is <100> Si or SiGe.

33. Process for manufacturing a composite structure according to claim 31, characterised in that the growth substrate includes bulk sapphire (Al_2O_3), monocrystalline bulk SiC, bulk ZnO or bulk <111> Si, and the layer made of monocrystalline material is made of SiC, <111> Si, GaN, AlN, InN, $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{1-x}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$.

34. Process for manufacturing a hybrid structure comprising production of a composite structure according to the process for manufacturing a composite structure according to one of claims 22 to 33, further comprising

crystalline growth of an upper monocrystalline structure on the layer made of a monocrystalline material such that the configuration of the upper structure and the materials from which it is composed are such that the quality of the layer of nitride semiconductor layer is better than it would have been if the nitride semiconductor were made directly on the layer made of a monocrystalline material.

35. Process for manufacturing a hybrid structure according to the preceding claim, characterised in that the upper structure comprises a layer chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$.

36. Process for manufacturing a hybrid structure according to one of the preceding two claims, characterised in that the upper structure comprises a layer chosen from among the following alloys: $Al_xIn_yGa_{(1-x-y)}N$, $In_yGa_{(1-y)}N$, $Al_xGa_{(1-x)}N$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, the concentration of at least one of the elements in the chosen alloy varying progressively through the thickness.