PROGRAMMABLE READ/WRITE ACCESS SIGNAL AND METHOD THEREFOR

ABSTRACT OF THE DISCLOSURE

A system bus controller (103) within a processor (101) includes programmable logic for different modes of chip enable signals on a per-address-space basis. This allows for a "glueless" interface (107) between the processor (101) and different types of external devices (111, 112, 113), such as memory devices. A chip select register value 604, 608, 612 is preprogrammed with respect to each external device coupled to the processor (101). This preprogrammed register value 604, 608, 612 is used by the system bus controller (103) to uniquely configure a read/write access signal to be sent to each of the external devices (111, 112, 113).

Figure 1 accompanies this abstract.