[0053] Generally, the drain 120 can be formed above the substrate 102, thereby forming an elevated drain on the substrate 102. In such cases, the drain 120 is not formed within the substrate 102, which allows the drift region 114 to occupy a portion of the substrate 102 traditionally used for a drain region by previous LDMOS structure methodologies. By forming the drain 120 directly on the drift region 114 and completely above the top surface 118 of the substrate 102, the drift region 114 may occupy a larger volume ~~within the~~ including the top surface 118 of the substrate 102 without consuming additional device surface area (i.e., the dimensions of the drift region 114 do not need to be increased to reduce problematic substrate currents). Notably, the present inventors have discovered that the elevated drain system and method of the present embodiments produces a device with substrate currents (I_{submax}) that are reduced by about one order of magnitude when compared to traditional similar dimensioned LDMOS structures, which form the drain region in the substrate 102. For example, traditional LDMOS structures exhibit an I_{submax} of about 25 micro-ampere/micro-meter, while the elevated drain system and method of the present embodiments produces an I_{submax} of about 3.8 micro-ampere/micro-meter.

[0054] The present inventors have also discovered that the elevated drain system and method of the present embodiments produces a device with substantially similar threshold voltage (V_t) characteristics, drive current (I_{dsat}) characteristics, and device breakdown voltage (BVDSS) characteristics as a traditional similar dimensioned LDMOS structure.

[0055] The elevated drain system and method of the present embodiments displaces the drain 120 vertically above the drift region 114, thereby allowing the drift region 114 to increase its volume by occupying the volume previously occupied by a traditional LDMOS drain. Accordingly, the system and method of the present embodiments helps to reduce the active device 104 pitch because the drift region 114 will not need to be made longer/wider to reduce the substrate 102 current. In at least one embodiment, it has been discovered by the present inventors that the elevated drain system and method of the present embodiments can provide about a twenty (20) percent reduction in pitch over that of a traditional LDMOS device configuration.

[0056] Moreover, it will be appreciated by those skilled in the art that the elevated drain system and method of the present embodiments can improve the safe operation region margin (e.g., in terms of device breakdown and reliability) due to lower substrate currents and lower parasitic capacitances. For example, by relocating and optimizing the placement of the drain

120 (e.g., above the substrate 102), this highly doped region can be moved further away from substrate 102, so that junction breakdown voltage is not degraded. As such, the parasitic

What is claimed is:

1. A method for manufacturing an integrated circuit system comprising:
providing a substrate including an active device;
forming a drift region in the substrate, the drift region bounded in part by a top surface of the substrate and spaced apart from a source; and
forming a drain above the drift region.

2. The method as claimed in claim 1 wherein:
providing the active device includes providing an NMOS device.

3. The method as claimed in claim 1 wherein:
forming the drain inlcudes an epitaxial growth process.

4. The method as claimed in claim 1 wherein:
forming the drain inlcudes depositing a semiconducting material.

5. The method as claimed in claim 1 wherein:
forming the drain above the drift region alters the substrate current, the parasitic capacitance, or the on-state resistance of the active device.

6. A method for manufacturing an integrated circuit system comprising:
providing a substrate;
forming a drift region in the substrate, the drift region bounded in part by a top surface of the substrate;
forming a drain above the drift region;
forming a source in the substrate and spaced apart from the drift region;
forming a gate dielectric, a gate, and a spacer above the substrate; and
forming an electrical contact.

7. The method as claimed in claim 6 wherein:
forming the drain and the gate includes forming each structure to be substantially coplanar with the other.

8. The method as claimed in claim 6 wherein:
forming the drain above the drift region includes forming the drain on the substrate.

9. The method as claimed in claim 6 wherein:
forming the gate includes overlapping a portion of the source and the drift region with the gate.

10. The method as claimed in claim 6 wherein:

forming the electrical contact includes one of the electrical contact formed over the source and aligned to the spacer.

11. An integrated circuit system comprising:

a substrate including an active device;

a drift region in the substrate, the drift region bounded in part by a top surface of the substrate and spaced apart from a source; and

a drain above the drift region.

12. The system as claimed in claim 11 wherein:

the active device includes an NMOS device.

13. The system as claimed in claim 11 wherein:

the drain inlcudes an epitaxial material.

14. The system as claimed in claim 11 wherein:

the drain inlcudes a semiconducting material.

15. The system as claimed in claim 11 wherein:

the location of the drain above the drift region alters the substrate current, the parasitic capacitance, or the on-state resistance of the active device.

16. The system as claimed in claim 11 wherein:

the substrate includes a lightly doped region.

17. The system as claimed in claim 11 wherein:

the drain and the gate are substantially coplanar with each other.

18. The system as claimed in claim 11 wherein:

the drain is on the substrate.

19. The system as claimed in claim 11 further comprising:

a gate of the active device that overlaps a portion of the source and the drift region.

20. The system as claimed in claim 11 further comprising:

an electrical contact over the source and aligned to a spacer.

What is claimed is:

1. A method for manufacturing an integrated circuit system comprising:

providing a substrate including an active device;

forming a drift region in the substrate, the drift region bounded in part by a top surface of the substrate and spaced apart from a source; and

forming a drain directly on the drift region and not within the substrate wherein the drain is formed completely above the top surface of the substrate.

2. The method as claimed in claim 1 wherein:

providing the active device includes providing an NMOS device.

3. The method as claimed in claim 1 wherein:

forming the drain inlcudes an epitaxial growth process.

4. The method as claimed in claim 1 wherein:

forming the drain inlcudes depositing a semiconducting material.

5. The method as claimed in claim 1 wherein:

forming the drain above the drift region alters the substrate current, the parasitic capacitance, or the on-state resistance of the active device.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate;

forming a drift region in the substrate, the drift region bounded in part by a top surface of the substrate;

forming a drain directly on the drift region and not within the substrate wherein the drain is formed completely above the top surface of the substrate;

forming a source in the substrate and spaced apart from the drift region;

forming a gate dielectric, a gate, and a spacer above the substrate; and

forming an electrical contact.

7. The method as claimed in claim 6 wherein:

forming the drain and the gate includes forming each structure to be substantially coplanar with the other.

8. The method as claimed in claim 6 wherein:

forming the drain above the drift region includes forming the drain on the substrate.

9. The method as claimed in claim 6 wherein:
forming the gate includes overlapping a portion of the source and the drift region with the gate.

10. The method as claimed in claim 6 wherein:
forming the electrical contact includes one of the electrical contact formed over the source and aligned to the spacer.

11. An integrated circuit system comprising:
a substrate including an active device;
a drift region in the substrate, the drift region bounded in part by a top surface of the substrate and spaced apart from a source; and
a drain directly on the drift region and not within the substrate wherein the drain is formed completely above the top surface of the substrate.

12. The system as claimed in claim 11 wherein:
the active device includes an NMOS device.

13. The system as claimed in claim 11 wherein:
the drain inlcudes an epitaxial material.

14. The system as claimed in claim 11 wherein:
the drain inlcudes a semiconducting material.

15. The system as claimed in claim 11 wherein:
the location of the drain above the drift region alters the substrate current, the parasitic capacitance, or the on-state resistance of the active device.

16. The system as claimed in claim 11 wherein:
the substrate includes a lightly doped region.

17. The system as claimed in claim 11 wherein:
the drain and the gate are substantially coplanar with each other.

18. The system as claimed in claim 11 wherein:
the drain is on the substrate.

19. The system as claimed in claim 11 further comprising:
a gate of the active device that overlaps a portion of the source and the drift region.

20. The system as claimed in claim 11 further comprising:
an electrical contact over the source and aligned to a spacer.