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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Methods of Making Small Geometry Apertures in an Insulating Layer and Semiconductor Devices Produced by Such Methods

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to methods of making small geometry apertures in an insulating layer and semiconductor devices produced by such methods and more particularly to selective removal of insulating material provided on a semiconductor surface in order to provide special masking configurations for forming, for example, small geometry junction devices and ohmic connections to a semiconductor surface.

There is a continuing trend in the semiconductor field to demand devices operable at higher frequencies and capable of switching at higher speeds. In response to this demand, both diodes and transistors have been fabricated to incorporate design considerations in order to obtain these required operating characteristics. In particular, the physical dimensions of the diodes or the transistors must be made very small, especially the junction areas of these devices, in order to enable them to be operated at the high range of frequencies and the switching speeds demanded by space age requirements.

There is associated with the junctions of semiconductor devices, such as diodes or transistors, a capacitive reactance, which at high frequencies is of significant value to retard the operation of these devices. In addition when a diode is switched from forward to reverse bias, the storage of minority carriers in the body of the device can cause large transient reverse current. This effect is very important in diode switching circuits because it appears that the switch does not open immediately and this slows down the switching operation. To overcome these objections and to provide higher frequency and faster switching devices, it is necessary to have as small an operating junction area as possible, thus minimizing the capacitive reactance and the minority carrier storage at the junction. In addition, the reduced junction area will correspondingly mean reduced leakage current across the junction.

In response to this need for small junction area, there is presently known in the art diffused junction transistors and diffused junction diodes which utilize a photographic masking technique in their manufacture. For example, it is known to form an oxide layer on a surface of a silicon substrate and to apply a layer of photoresist material over the oxide layer. A photographic mask having opaque areas corresponding to the apertures to be formed for diffusion purposes is then placed over the photoresist and a photographic exposure made. Regions of the photoresist not covered by opaque regions of the mask are thus rendered etch resistant while the mask regions can be dissolved to uncover the underlying regions of the oxide layer which can then be apertured by use of an etchant which does not affect the etch resistant portions of the photoresist coating. As a result of this photographic technique, junction diodes and transistors having relatively small diffusion apertures (and consequently small junction areas) may be produced.

When such apertures, however, are required to have areas of the order 0.1 sq. mil or less, the limits of resolution in the photographic mask can result in undesired irregularities in the shape of the apertures

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produced. In particular, when using a mask having rectangular opaque areas, apertures may be produced having corners rounded to such an extent that the production of reasonably rectangular apertures having areas of about 0.1 sq. mil or less is impracticable. Furthermore, the small dimensions involved present a formidable resolution problem in aligning the masks or patterns for the series of diffusion steps needed to produce the desired junctions. Hence, there will be a corresponding limitation upon the size of the junctions' areas that may be formed, thus limiting the frequency and the switching speed at which transistors and diodes may be operated.

The present invention is a method of making a semiconductor device, in which:—

(a) a first layer of insulating material is formed on one surface of a semiconductor body;

(b) a portion of the insulating material is removed to form a first slot exposing a corresponding portion of the surface of the semiconductor body;

(c) a second layer of insulating material is formed on the surface of the semi-conductor body within the slot;

(d) insulating material is removed to form a second slot intersecting the first slot and to expose the semi-conductor body surface only over the area of intersection of the first and second slots, and

(e) an impurity is diffused into the portion of the semiconductor body exposed by the said step (b) or by the said step (d) or separately into both the said portions, the or each diffusion taking place following the step concerned.

Preferably, the first and second slots extend at right angles to each other. The slots can be formed by photographic techniques and since the length of the slots can be made comparatively large in comparison to the width of the slots, it is possible to intersect the first formed slots with subsequently formed slots without a high degree of resolution on the part of the operator. In addition, although each of the slots will have the distortion and irregularities in the form of rounded corners, etc. which were mentioned above, these distortions will occur at the ends of each of the slots. Since the intersection of the slots occurs at points between the ends, it is possible to produce at these intersections very small apertures which are well defined and free from distortion.

Diffusions of impurity made into these extremely small apertures result in the production of extremely small junction areas, thereby allowing the production of semiconductor devices capable of operation as high frequency, high speed switching devices. Devices may thus be produced, in accordance with the invention, in which the limitation upon the minimum area to which device junctions may be fabricated is the width to which each slot may be formed.

In a particular embodiment of the invention an intrinsic semiconductor body is used and the second insulating layer is thinner than the first layer. Separate portions of insulating material then are removed to form, respectively, second and third slots intersecting the first slot to produce first and second holes in the second insulating layer at the respective loci of intersection of the first slot with the second and third slots. Impurity material is diffused into the semiconductor body through the first and second holes to form first and second regions, of desired impurity characteristics, substantially beneath those holes. For example, a P-I-N diode can be produced by diffusing opposite type impurities through the first and second holes and attaching ohmic contacts to the first and second diffused regions. A transistor can be formed, for instance, by diffusing an impurity region into the semiconductor body through the first slot, that region having conductivity carriers of conductivity type opposite that of each of the first and second diffused regions, ohmic contacts being attached to each of the diffused regions.

In another embodiment, in which the second layer of insulating material is thinner than the first layer, the impurity is diffused into the semiconductor body through the first slot to form a first diffused region substantially beneath the first slot and the locus of intersection of the first and second slots defines a first hole through which impurity is diffused into the semiconductor body to form a second diffused region substantially beneath the first hole and within the first diffused region. A third layer of insulating material then is formed on the semiconductor surface within the first hole and insulating material is removed to form a third slot of lesser width than and extending along the second slot to produce in the third insulating layer a second hole at the locus of intersection of the first and third slots. An impurity is then diffused through the second hole into the semiconductor body to form a third diffused region substantially beneath the second hole and within the second diffused region. A transistor can be produced by formation of the first and third diffused regions with a conductivity type opposite that of the second diffused region and with individual ohmic contacts being connected to each of the diffused regions.

This invention can also be utilized in the production of miniaturized integrated semiconductor circuit devices wherein both active and passive circuit elements are incorporated within one semiconductor body.

A resistor for an integrated circuit can be formed by the diffusion of doping impurities into a semiconductor body in a defined pattern. Subsequently, a protective coating, such as silicon oxide for example, may be formed over the diffused resistor. Photomasking and etching techniques are employed to remove selected portions of the protective coating so that ohmic contacts to the resistor can be made. Heretofore, the resistor has been enlarged near the contact area to allow for photomask line-up clearance or tolerance around the contact area and thus ensure adequate contact surface on the resistor. There are several inherent disadvantages with integrated circuit resistors produced in this way. Each resistor requires more space on the semiconductor body because of the enlarged contact regions. Also, the enlarged contact regions increase the resistor-substrate capacitance. Resistors with multiple contacts are less accurate because of the varying cross-sectional areas. This latter disadvantage is especially important where master patterns are utilized in producing integrated circuits. In order to reduce the costs of integrated circuits, master photomasking patterns can be used to produce semiconductor wafers with a number of active and passive elements therein. By varying only the masking and etching for the conductive leads and ohmic contacts, any one of a variety of circuits can be obtained from each wafer. Each wafer has several resistive elements from which a wide range of resistance values can be obtained by selectively placing the resistor contacts.

By use of the present invention, integrated circuit resistors can be made with uniform cross-sectional areas. Impurity can be diffused into the portion of the semiconductor body following the said step (b) in the method according to the invention described above, and an ohmic metal contact can be deposited on the surface portion of the body exposed by the said step (d) in that method. The photo-mask used in making a contact surface on a resistor or other integrated circuit element provides an area for etching that is wider than the desired contact surface width, thus allowing for the mask line-up clearance. Because the protective coating, silicon oxide for example, is thinner over the desired contact surface than over the adjacent semiconductor wafer surface, controlled etching can remove the protective coating from the contact surface while sufficient protective coating will remain adjacent thereto to prevent the contact from shorting to the substrate. Contact to a resistor is possible by removing the protective coating from across the resistor at any point. These same principles can of course be used to make contacts to elements other than resistors.

By way of example the invention will be described in greater detail with reference to the accompanying drawings, in which:—

Figure 1 is a plan view of a small geometry P-N diode constructed in accordance with the present invention;

Figures 2 and 3 are pictorial views in section of the device of Figure 1, taken along the line 2-2, at various stages of manufacture;

Figure 4 is a plan view of a small geometry P-N diode device shown with the expanded ohmic contacts and external leads connected thereto;

Figure 5 is a plan view of a small geometry P-I-N diode constructed in accordance with the present invention;

Figure 6 is a pictorial view in section of the device of Figure 5, taken along the line 6-6, showing the manufacture thereof;

Figure 7 is a plan view of a small geometry P-I-N diode with the ohmic contacts and external connections thereof;

Figure 8 is a plan view of a small geometry surface-oriented transistor constructed in accordance with the present invention;

Figure 9 is a pictorial view in section of the transistor of Figure 8, taken along the line 9-9, showing the manufacture thereof;

Figure 10 is a plan view of a completed small geometry surface-oriented transistor shown with the ohmic contacts and external connections;

Figure 11 is a plan view of a matrix of elongated slots formed for a high power, high frequency transistor;

Figure 12 is a pictorial view in section of the transistor structure of Figure 11 taken along the line 12-12, showing the manufacture thereof;

Figures 13 and 14 are pictorial views in section showing the manufacture of a high frequency, high power, and high gain transistor;

Figure 15 is a plan view of the completed device shown in Figures 13 and 14 with the ohmic contacts and external leads connected thereto;

Figure 16 is a schematic diagram of an electronic circuit;

Figure 17 is a plan view, depicting the layout of all circuit elements, of the circuit of Figure 16 integrated in a semiconductor wafer;

Figures 18a-18f are cross-sectional views, taken along the sectional line 3-3 of Figure 17, of the semiconductor wafer during fabrication of the integrated circuit in accordance with this invention, and

Figures 18g-18i are enlarged cross-sectional views of a resistive element showing the steps in providing a contact surface on the resistive element in accordance with this invention.

Reference is made to Figures 1-4, wherein there is illustrated a small geometry diode semiconducting device, at various stages of manufacture thereof, in accordance with the present invention. It is to be noted that these views are of only one segment of an entire semiconductor slice which comprises many such segments during manufacture and is separated into individual wafers only after the diffusions have been made and contacts applied.

There is illustrated in Figure 1 a plan view of a small geometry P-N diode 1 constructed in accordance with the present invention, showing the thin cross stripes 12 and 18, and the small opening at the intersection 21. There is represented in Figure 2 an intrinsic body of semiconductor material 10 such as silicon or germanium for example. By the term "intrinsic" is meant a material having a high resistivity due to low concentration of impurities or due to the presence of trapping levels. This value of resistivity may be 100Ω-cm, for example. An insulating layer 11 is formed over the entire surface of the material 10 using any conventional technique and material such as silicon oxide. The insulating layer 11 can be formed of silicon oxide to a thickness of approximately 8000Å.

After the insulating layer 11 has been deposited, an elongated strip 12 of the layer is selectively removed so as to expose an elongated area of the surface of the semiconductor material 10. This removal may be accomplished by first coating the insulating layer 11 with a photoresist material such as one of the "Kodak" (Registered trade mark) resists designated KMER or KTFR, the latter being preferred. Next, a photomask is placed in contact with the surface of the photoresist film. Due to thickness of the photomask, the location of the opaque portion of the photomask relative to the surface of the resist, and the wave length of the exposing light, the light tends to be refracted around any portion of the photomask. This prevents accurately exposing the photoresist around a very small dot. However, refraction of the exposing light is of concern only in one direction around an opaque line on the mask so that the width of a strip of the photoresist masked from exposure can be controlled with considerable accuracy. The mask and unexposed area of the photoresist is then removed by a developing solution to expose the surface of the oxide insulating film 11 in the elongated area 12. Using this technique, it is possible with the state of the art at its present level to remove a strip of photoresist approximately 0.1 mil in width, while the length of the strip removed might be as much as 3 mils. After the unexposed strip of the photoresist is removed by developing, the substrate is subjected to a suitable etching fluid, such as a buffered HF solution saturated with ammonium bifluoride, and the portion of the oxide film 11 which is not protected from the etchant by the resist is selectively removed to form the elongated slot 12 and expose an area of the substrate approximately the same size as the strip of the photoresist removed, in other words, approximately 0.1 mil in width and approximately 3 mils in length. The photoresist material is then stripped from the surface of the oxide insulating layer 11.

The silicon oxide layer 11 which remains upon the intrinsic material 10 serves a number of purposes, two of which are of particular significance. First, the layer is formed of a material into which impurities to be employed during subsequent manufacturing steps will not diffuse. Second, the thickness of the silicon oxide layer 11 can play a significant role in carrying out the present invention, which significance will be subsequently observed.

As a further step in the manufacture of the small geometry diode, as illustrated in Figure 2, there is provided upon the upper surface of the semiconducting material 10 and within the elongated opening 12, a predetermined amount of acceptor impurity. Application of sufficient heat to the material 10 and the impurity results in a diffusion of the impurity applied into the body of intrinsic material 10 so as to produce a region proportion 20 of P-type silicon within the body of intrinsic material 10. During this diffusion and also during the impurity deposition preceding the diffusion, there is normally produced an oxidation of surface silicon so that a very thin silicon oxide layer 13 is formed as indicated in Figure 2. This layer 13 is substantially thinner than the silicon oxide insulating layer 11 which was previously grown purposefully. For example, the silicon oxide layer 13 which is naturally produced during the acceptor impurity diffusion step would be a thickness of approximately 1500Å to to 3500Å, while the oxide layer 11 would be fabricated to a thickness of approximately 8000Å, or over two times the thickness of layer 13.

A coat of photoresist, thereafter, is deposited upon the silicon oxide layers 11 and 13 and exposed in all areas except for an elongated area corresponding to the slot 18. The photoresist is then developed, and the exposed area is subjected to the fluid etchant, buffered HF solution: The silicon oxide layer 13, being substantially thinner than the silicon oxide layer 11, will completely etch away within the exposed portion, thereby exposing the P-type region 20 within the intersection area 21, without danger of the insulating layer 11 also being cut away com-

pletely. The remaining photoresist is then removed by a suitable stripping fluid.

As a result of the above-described process, there is produced at the intersection area 21 a small aperture exposing the upper surface of the P-type region 20 and into which impurities to be employed during a subsequent N-type diffusion operation may be deposited. This aperture may be as small as necessary in order to obtain any desired operating characteristics of the present invention, the small geometry diode. In one embodiment of the invention, the slots 12 and 18 were formed approximately 0.1 mil in width and approximately 3 mils in length. This resulted in an aperture or opening at the area 21 of approximately 0.01 square mil.

As a next step in the manufacture of the small geometry P-N diode, as illustrated in Figure 3, there is disposed into the small aperture or opening formed at the intersection area 21 and upon the upper surface of the P-type region 20 a predetermined amount of donor impurity, and heat is applied whereby the impurity diffuses into the region 20 to form an N-type layer 30. Intermediate the regions 20 and 30 there is provided a junction 25 in the well-known manner whereat particular desired electrical characteristics are realized. It is to be noted that the unremoved portion of the silicon oxide layer 13 serves as a mask to limit the lateral diffusion of the donor impurity. During the N-type diffusion and/or the impurity deposition a very thin silicon oxide layer 26 is formed which completely covers the exposed surface of the N-type layer 30.

As a further step in the manufacture of the small geometry diode, there will be attached external leads so as to allow for operation as a high frequency, high speed switching device. Due to the extremely small dimensions associated with the diffused regions being described, expanded contacts are utilized. The etchant fluid is first applied completely covering the surface of the entire device shown in Figure 3. Since the silicon oxide layer 26 is substantially thinner than the oxide layer 11 and 13, it will be relatively simple to closely control the duration of etching so as to competely remove the layer 26 without consequently cutting through the other layers 13 and 11. There is thereby provided a region where an expanded ohmic contact may be placed so as to allow an external lead to be connected to the cathode, or N-type layer 30. The entire device then goes back through a photomasking process whereby the silicon oxide layer 13 is selectively etched and removed to form an opening above the upper surface of the P-type region 20. There is thereby provided a region whereby an expanded ohmic contact may be placed so as to allow an external lead to be connected to the anode or P-type layer 20. An aluminum coating is then formed completely covering the upper surface of the device. This may be accomplished by any conventionel method as, for example, vacuum evaporation. Thereafter, the entire device again goes through a photographic masking and etching process which selectively removes the aluminum coating from substantially all portions except where the expanded ohmic contacts are to be placed. The aluminum coating remaining at the openings is then alloyed in the conventional manner into the underlying silicon. In this manner there is provided over the N-type layer 30 and over the P-type layer 20 expanded ohmic contacts 31 and 32, respectively, as illustrated in Figure 4. Since the width of the elongated slots 12 and 18 will normally be as narrow as photographic masking techniques will allow, presently at a value of approximately 0.1 mil, the expanded ohmic contacts 31 and 32 will necessarily overlap onto the insulating layers 11 and 13 as shown in Figure 4. This will present no problems since the layers 11 and 13 were fabricated from a nonconducting material, usually silicon oxide. Gold wires are then ball bonded to the expanded ohmic contacts 31 and 32 in a conventional manner to form the external cathode lead 33 and external anode lead 34. As a result of the extremely small region 21 provided at the intersection of the slots 12 and 8, a very small P-N junction has been fabricated, thus allowing the completed diode 1 to be operated at very high frequencies and at high switching speeds.

As an alternative method of producing the expanded ohmic contacts 31 and 32, the aluminum coating may be replaced by one of gold and molybdenum. Despite its advantages for use as a contact material in semiconductor devices, aluminum has nevertheless a number of disadvantages that are not characteristic of gold and molybdenum. The first and most prominent is that when the gold wires are bonded to aluminum ohmic contacts, an intermetallic compound of gold and aluminum is formed. This compound, being brittle, decrease the reliability of the devices upon which it is formed. In addition there is evidence that the application of aluminum films by means of evaporation often results in electrical degradation of semiconductor devices in the form of shorts, high saturation currents, decreased gain, and undesirably low reverse breakdown characteristics.

To overcome these disadvantages the ohmic contacts 31 and 32 may be fabricated from molybdenum and gold in the following manner. A thin film of bolybdenum is first applied to the upper surface of the device i shown in Figure 3. Then the molybdenum is

covered with a thin film of gold, and thereafter the gold and molybdenum are etched away in unwanted areas, leaving the desired pattern of contacts. It should be noted that with the use of molybdenum and gold, there is essentially an "alloyless" system. The molybdenum is not alloyed into its substrate, and the gold does not alloy with molybdenum. In contrast with aluminum where the deposited metal is ordinarily heated to a temperature above the aluminum silicon eutectic 577°C, the gold and molybdenum layers are deposited at reasonably low temperatures and need no heating to produce alloying. Since heating steps are avoided, degradation of the semiconductor devices is minimized.

Considering now the present invention as it relates to surface-oriented small geometry P-I-N high frequency diodes, reference is made to Figures 5-7 of the drawings. Figure 5 shows a schematic top view of the steps in the manufacture of the P-I-N diode 50. As can best be seen in the sectional view of Figure 6 taken along the line 6-6 of Figure 5, the diode 50 is comprised of the intrinsic material 55 having an oxide layer 56 completely covering the upper surface of the material 55. The oxide layer 56 may be composed of any conventional material, preferably silicon oxide, which may be formed upon the surface of the substrate by reactive sputtering or other suitable techniques. The oxide layer 56 would be formed to a thickness of approximately 8000Å and would be nonconductive in nature.

After the oxide layer 56 has been deposited, an elongated strip 52 of the layer is selectively removed so as to expose an elongated area of the surface of the intrinsic material 55. This may be accomplished by the same photographic techniques outlined above for the manufacture of the small geometry P-N diode. As a result of this photographic and etching process, there is formed the elongated slot 52, approximately 0.1 mil in width and approximately 3 mils in length. A second insulating layer 57 is next formed over the surface of the first insulating layer 56 and over the exposed surface of the intrinsic semiconductor region 55. The insulating layers 56 and 57 preferably are of the same material, preferably of silicon oxide. Close control over the etching process to be presently described may be maintained by fabricating the second insulating layer 57 to a thickness substantially smaller than the first insulating layer 56. For example, if the first silicon oxide layer 56 is of a thickness of 8000Å, the second silicon oxide layer 57 could be of a thickness of 2000Å.

A coat of photoresist is then deposited on the second insulating layer 57 and exposed in all areas except for an elongated area corresponding to the slot 54. Then when the photoresist is developed, and the device 50 subjected to the fluid etchant, buffered HF solution, the oxide layer 57 is selectively removed to form a slot 54. As a result of the difference in oxide thickness, the etchant will remove the second layer 57 to expose the upper surface of the intrinsic material 55 at the aperture 53 without consequently cutting through the first silicon oxide layer 56. As a result of the above-described process, there is produced a small aperture 53 into which impurities to be employed during a subsequent P-type diffusion operation may be deposited. Since the slots 52 and 54 would be approximately 0.1 mil in width, for example, the small aperture 53 will then be of an area of approximately 0.01 square mil.

As a further step in the manufacture of the surface oriented P-I-N high frequency diode, as shown in Figure 6, there is disposed upon the upper surface of the intrinsic material 55 within the small aperture 53 a predetermined amount of acceptor impurity. Heat is then applied so as to cause the impurity to diffuse into the substrate to form the P-type region 51. The insulating layer 57 will act as a diffusing mask so as to limit the lateral diffusion of the acceptor impurity into the substrate. During this diffusion process there will be naturally formed a very thin layer 58 of silicon oxide which will completely cover the exposed surface of the P-type region 51.

In the identical manner as the elongated slot 54 was previously formed, the elongated slot 64 is now formed so as to intersect the slot 52. Using the photographic technique and etching process described above, the insulating layer 57 is selectively removed in the area of the slot 64, thus exposing the upper surface of the intrinsic material 55 within the area of the small aperture 59. The aperture 59 will also be of an area 0.01 sq. mil, for example. Into this aperture 59, there is then diffused a predetermined amount of donor impurity so as to form the N-type region 60. There will again be normally produced a very thin silicon oxide layer 61 which will completely mask the exposed surface of the N-type region 60.

It is to be pointed out that the positioning of the slot 64 with respect to the slot 54 will determine the width of the intrinsic layer 55 beween the P-type region 51 and the N-type region 60, thus determining the operating characteristics of the entire diode 50. This positioning may be closely controlled through the use of the photographic masking techniques outlined above.

As the final steps in the manufacture of this device, ohmic contacts are provided so as to allow external leads to be connected to the anode, or P-type region 51 and to the cathode, or N-type region 60. The upper

surface of the device 50 is thereby covered with etchant fluid. Since the silicon oxide layers 58 and 61 are substantially thinner than either of the oxide layers 56 and 57, they will be selectively removed at the openings 53 and 59, respectively, as illustrated in Figure 7, without consequently cutting through the layers 56 and 57.

A coating of either aluminum or molybdenum and gold is next deposited upon the upper surface of the device 60. Thereafter, the device again goes through a photographic masking and etching process similar to those already described to selectively remove the coating from unwanted areas, thus forming the expanded ohmic contacts 62 and 63 at the openings 53 and 59, respectively. Gold wires are then ball bonded to the expanded ohmic contacts as illustrated in Figure 7 to form the external anode lead 65 and the external cathode lead 66.

Small geometry surface-oriented transistors can be manufactured in accordance with the present invention, as will be described with reference to Figs. 8-10 of the drawings. Figure 8 shows a schematic top view of the transistor 70. As can best be seen in the section view of Figure 9, transistor 70 is comprised of the intrinsic material 75 having an oxide layer 76 completely covering the upper surface of the material 75. The oxide layer 76 may be composed of any conventional material, preferably silicon oxide, which may be formed upon the surface of the substrate by reactive sputtering or other suitable techniques. The oxide layer 76 would be formed to a thickness of approximately 8000Å and would be insulating in nature.

After the oxide layer 76 has been formed, a strip 72 of the layer is selectively removed so as to expose an elongated area of the surface of the intrinsic material 75. This may be accomplished by the same photographic techniques outlined above for the manufacture of the small P-N and P-I-N diodes. As a result of this photographic and etching process, there is formed the elongated slot 72 which may be as narrow as 0.1 mil in width and approximately 3 mils in length. As a further step in the manufacture of the small geometry transistor, there is provided upon the upper surface of the semiconductor material 75 and within the elongated slot 72 a predetermined amount of impurity. Application of sufficient heat to the material 75 and the impurity alloy results in a diffusion of the impurity into the body of intrinsic material 75, so as to produce a region or portion 77 of P-type silicon within the body of intrinsic material 75. This region 77 will hereafter be referred to as the base region or layer. During this diffusion there will be normally produced an oxidation of the surface silicon so that a thin silicon oxide layer 78 is formed as indicated in Figure 9. As compared to the insulating oxide layer 76 which was purposefully fabricated to a thickness of 8000Å, the thin silicon oxide layer 78 would be naturally formed to a thickness of approximately 1500Å to 3500Å.

A coat of photoresist is deposited upon the upper surface of the silicon oxide layer 78 and the insulating oxide layer 76 and exposed in all areas except for the elongated regions corresponding to the slots 80 and 82. The photoresist is then developed and the exposed areas 80 and 82 are subjected to the fluid etchant, buffered HF solution, for example. When the insulating layer 76 is fabricated of silicon oxide, the same material that is naturally formed as the layer 78 during the P-type diffusion, the diffusion, the difference in thickness of the two layers (the thickness of layer 76 being approximately two times that of layer 78) will allow for the necessary control to be maintained over the second etching step in order that the very small apertures 81 and 83 may be formed above the P-type base region.

Within the small opening 81 and 83 and upon the exposed surface of the P-type base region 77, there is thereby disposed a quantity of donor impurity, as in the form of a silicon alloy, and heat is applied whereby the impurity diffuses into the region 77 to form N-type regions 84 and 85. The unremoved portion of the thin silicon oxide layer 78 will serve as a mask to limit the lateral diffusion of the donor impurity. As a result of this diffusion there is provided intermediate the base region 77 and the N-type region 84, hereafter referred to as the collector region or layer, a junction 86 which serves as the collector-base junction for the transistor device 70. In like manner, there will be provided intermediate the base region 77 and the N-type region 85, hereafter referred to as the emitter region or layer, a junction 87 which serves as the emitter-base junction for the transistor device 70. Due to the extremely small areas that may be obtained using the cross striping techniques as described to form the openings 81 and 83, it is possible with the state-of-the-art at its present level to produce very high frequency transistor devices with junctions having a functioning area of approximately 0.01 sq. mil. During the N-type diffusion there will be consequently formed a layer 90 of silicon oxide which completely covers the upper surface of the collector layer 84 and the upper surface of the emitter layer 85. This oxide layer 90 will be exteremely thin, approximately one-third the thickness of the silicon oxide layer 78, and less than one-sixteenth the thickness of the insulating layer 76.

The thin oxide layer 90 may then be

removed by any conventional technique, such as dip etching, the upper surfaces of the emitter region 87 and the collector region 86 thereby being exposed. Subsequently, using a photographic masking and etching process, a portion of the protective oxide layers 76 and 78 are selectively removed to expose the upper surface of the base region 77. Aluminum or molybdenum and gold is then deposited upon the exposed emitter, collector, and base surfaces and selectively etched so as to form expanded ohmic contacts to allow for external collector lead 91, external emitter lead 92, and external base lead 93 to be attached as illustrated in the plan view of Figure 10.

The cross-striping technique used to produce the extremely small junction areas in the previous embodiments also may be utilized to form a matrix of elongated slots for high power transistor fabrication as illustrated by the plan view of Figure 11. The sectional view of Figure 12 shows one portion of this matrix illustrating the fabrication. Referring to Figure 12, a thin layer 95 of P-type semiconducting material is formed upon a body 94 of low resistivity heavily doped P-type semiconducting material. The layer 94 will provide better ohmic contact between the layer 95 which serves as the collector region and subsequent external connections. In a manner described for the previous embodiments, an oxide layer 96 formed preferably of silicon oxide is formed above the collector region 95. Thereafter, a very thin elongated strip 97 is selectively removed as before to expose an elongated area of the surface of the collector area 95. Within this area there is diffused an N-type impurity to form a base region 98, thereby producing a junction 99, hereafter referred to as the collector-base junction. During the N-type diffusion operation, there will be naturally grown the thin silicon oxide layer 130. As a further step in the manufacture of the present device, a series of cross-stripes 132 and 134 are formed by the photographic masking and etching techniques which have been previously described producing the apertures 131 and 133 respectively. Within these apertures there is then diffused a P-type impurity forming the layers 135 and 136 hereafter referred to as the emitter regions. In between the emitter regions and the base region 98 there is produced the emitter-base function 137. A very thin silicon oxide layer will be formed during the P-type diffusion covering the upper surfaces of the emitter regions 135 and 136 within the apertures 131 and 133.

As the next steps in the manufacture of this device the thin elongated slots 138, 140 and 142 are formed, thereby exposing the base region within the openings 139, 141 and 143 respectively. Using any conventional technique, such as dip etching, the very thin silicon oxide layer covering the upper surface of the emitter regions 135 and 136 within the apertures 131 and 133 may be removed without consequently cutting through the oxide layers 96 and 130. Expanded ohmic contacts may then be deposited as shown in Figure 11 and selectively etched to connect the emitter regions together forming the emitter contact 144; similarly the base regions may be connected together by the base contact 145. External leads may then be attached to these contacts and directly to the layer 94 adjacent to the collector region 95 shown in Figure 12, the resultant device being capable of operation as a high frequency, high power transistor.

There is illustrated in Figures 13-15 a method for making a small geometry high-frequency high-power and high-gain transistor. Figure 13 shows the sectional view of the first steps of this method. Upon a body of intrinsic semiconductor material 100 there is purposefully grown an oxide layer 101 of insulating material, preferably silicon oxide, having a thickness of several thousand angstroms. Using a photographic masking and etching techniue, there is cut away from the layer 101 a strip of material so as to expose the upper surface of the intrinsic material 100 within the elongated slot 102. As pointed out in previous embodiments, this elongated slot may be as narrow as 0.1 mil for example. There is then diffused into the intrinsic material 100 at the slot 102 a predetermined amount of acceptor impurity so as to form the P-type layer 103 within the elongated slot 102. As collector region or layer. A thin layer of silicon oxide 104 naturally forms during this diffusion process so as to completely cover the upper surface of the P-type collector layer 103, hereafter referred to as the a further step in the manufacture of the transistor, a coat of photoresist is deposited upon the insulating layer 101 and upon the silicon oxide layer 104 and exposed in all areas except for an area corresponding to the region 105 as depicted in Figure 13. The photoresist is then developed and the exposed area 105 is subjected to a fluid etchant, buffered HF solution. The silicon oxide layer 104 will therefore be etched away and the upper surface of the P-type collector layer 103 will thereby be exposed at the intersection of the areas 102 and 105 within the opening 106.

As another step in the manufacture of the present device, there is disposed into the opening 106 and upon the upper surface of the collector region 103 a predetermined amount of donor impurity, and heat is applied whereby the impurity diffuses into the collector region 103 to form an N-type

layer 108, hereafter referred to as the base layer or region. As a result of this diffusion process, there is again formed a thin silicon oxide layer 111 which completely covers the upper surface of the base layer 108. Intermediate the base region 108 and the collector region 103 there is provided a junction 109 which will serve as the collector-base junction of the transistor device 110.

As a further step in the manufacture of this device, as depicted in Figure 14, a coat of photoresist is deposited upon the upper surface of the transistor 110 and exposed in all portions except in the area 112. Application of the etchant fluid will result in selectively etching away the silicon oxide layer 111 so as to expose the upper surface of the base layer 108 at the intersection of the elongated slot 112 and the elongated slot 102. There is thereby formed at the intersection of the slot 112 and the slot 102 a small opening 114 into which a small amount of acceptor impurity is deposited and subsequently diffused into the base area 108 to form a P-type layer 115, hereinafter referred to as the emitter layer or region. In a normal manner, there is again produced a very thin silicon oxide layer 118 completely covering the upper surface of the emitter layer 115 as illustrated in Figure 14. Intermediate these two layers there is produced a junction 116, which serves as the emitter-base junction.

Pursuant to the description above, it is to be noted that the width of the elongated slot 105 is approximatly five times as large as the width of the elongated slot 112. For example, if the slot 112 is formed to a width of 0.1 mil, the width of the slot 105 will be approximately 0.5 mil.

This difference in width will allow the placing of the elongated slot 112 within the boundaries defined by the slot 105 by photographic masking techniques without presenting a formidable task of resolution. As a result, the emitter layer 115 may be diffused above the collector layer 103 rather than to the side of the collector layer as the surface-oriented embodiment describes and is illustrated in Figures 8-12. Consequently, the width of the base region between the collector and emitter, being controlled by a diffusion operation rather than a photographic technique requiring a high degree of resolution, may be narrower than that achieved using the surface-oriented method. The resultant transistor device 110, therefore, will have a higher gain than that produced by the surface-oriented method.

It is realized, of course, that the small opening 106 shown in Figure 13 (into which the donor impurity was deposited and diffused to form the base region 108) will be of a larger area than the small opening 114 shown in Figure 14 (into which the acceptor impurity was deposited to form the emitter region 115). Notwithstanding, the opening 106 would be of a very small area, approximately 0.05 sq. mil. Consequently, the operating area of the emitter-base junction 116 would still be extremely small, allowing for operation of the transistor 110 in the high-frequency range.

As the final steps in the manufacture of the transistor 110, photographic masking and etching techniques are utilized to expose the upper surface of the emitter, base and collector layers so that ohmic contacts may be deposited upon the exposed areas for the subsequent connection of external leads. The entire upper surface of the transistor 110 is first subjected to an etchant fluid. Since the oxide layer 118 shown in Figure 14 is substantially thinner than any of the other oxide layers 101 or 111, it is possible to control this etching step so as to completely cut through the layer 118 and expose the emitter region 115 without consequently cutting through any of the other layers.

Photomasking and etching are then employed so as to cut through the oxide layers 111 and 102 exposing the base layer 108 and the collector layer 103 respectively. Expanded ohmic contacts fabricated of aluminum or molybdenum and gold, for example, are then deposited upon the exposed regions, and gold wires are bonded to the ohmic contacts to form the emitter lead 120, the base lead 121, and the collector lead 122 as illustrated in the plan view of Figure 15. In the same manner as described in the preceding embodiment, a matrix of elongated slots may be placed upon a single wafer, and the subsequently produced emitters, bases, and collectors connected together in a conventional manner, the resultant device having the characteristics of high frequency, high power and high gain.

It is preferred to use intrinsic material, having very high resistivity, as the initial substrate in most of the above-described embodiments. As a result, a minimum contact area is maintained, thus minimizing any stray capacitance within the devices.

Another feature to be noted is the orientation of the elongated slots formed by the photographic masking and etching techniques described. Although it is to be pointed out that when the elongated slots are placed perpendicular to each other, the resulting apertures formed at the intersection of the slot will be of a minimum area, the intersection of the slots at oblique angles will also produce very small apertures which are well defined and free from distortion, thus allowing for a small geometry junction subsequently to be fabricated.

The so-called negative resist has been heretofore described in connection with the practice of this invention .When using a negative resist, the exposed portion of the material is polymerized and the unexposed portion is removed by development to form the slots through which the oxide is etched. However, it is to be understood that a positive resist could also be used, in which case the exposed portion is depolymerized and removed by the developing solution. In such a case, the narrow slot in the resist may be exposed by light or by an electron beam and the process carried out as previously described.

Referring now to Figure 16, it will be noted that therein is shown a dual input gate circuit in which the contacts 222 and 223 are inputs to the dual emitter transistor 230 and the contact 224 is an output from the emitter follower transistor 240. The base of transistor 230 is connected through the series-connected resistors R_1 and R_2 to the voltage source contact 227. The collector of the transistor 240 is ohmically connected to the common point of resistors R_1 and R_2, and the base of the transistor 240 is ohmically connected to the collector of the transistor 230.

In Figure 17, depicting the circuit of Figure 16 integrated in a semiconductor wafer W, the semi-conductor wafer W includes the two dual emitter transistors 230 and 240 and the resistor elements 201-207. The resistor R_1 includes portions of the resistive elements 201-204 which are connected by the ohmic leads 212-214. The resistor R_2 includes portions of the resistive elements 205-207 which are connected by the ohmic leads 216 and 217. The common ohmic lead 215 of the series-connected resistors R_1 and R_2 is connected through the ohmic lead 226 to the collector 244 of the transistor 240. The ohmic lead 227 is connected to the ohmic contact 218 on the resistive element 207, and the resistive element 201 is connected at the contact 211 through the ohmic lead 221 to the base 233 of the transistor 230. The ohmic leads 222 and 223 are connected to the emitters 231 and 232, respectively, of the transistor 230, and the collector 234 of the transistor 230 is ohmically connected through the lead 225 to the base 243 of the transistor 240. The emitter 242 of the transistor 240 is ohmically contacted to the lead 224. The emitter 241 of the transistor 240 is not utilized in this circuit. The region 250 electrically isolates the transistor 230 and the transistor 240.

The utility of the present invention in integrated circuit production can be seen with reference to Figures 18a-18f which illustrates the steps in producing the embodiment of Figure 17. Master photomasking patterns can be used in forming the transistors 230 and 240 and the resistive elements 201-207. Only two special photomasking patterns are needed to provide the ohmic contacts and leads and thus complete the circuit. Photomasking, etching and diffusion techniques are well known in the art; and since the techniques are not part of the invention, the techniques are not discussed in detail herein. The figures are drawn out of proportion in order to depict all details of the circuit fabrication.

Figure 18a shows the water W with a P-type silicon substrate 260, an N-type epitaxial layer 270 and a silicon oxide layer 280. The first silicon oxide removal is performed which creates the openings through the siicon oxide layer 280 for the diffusion of the isolating P-type region 250.

In Figure 18b the isolating P-type region is formed by diffusing a P-type dopant through the N-type epitaxial layer 270 thus defining the transistor collector regions 234 and 244. Silicon oxide is formed in the openings in the silicon oxide layer 280 and a second silicon oxide removal forms openings through the silicon oxide layer 280 for the diffusion of the transistor base regions and the resistive elements.

In Figure 18c a P-type dopant is again diffused through the silicon oxide layer 280 thus forming the P-type transistor base regions 233 and 243 in the collector regions 234 and 244, respectively, and resistive element 201 in the epitaxial layer 270. The resistor elements 202-207, not shown, are also formed by this diffusion. Referring back to Figure 17 it will be seen that all resistive elements have uniform widths with no enlarged regions for contact surfaces. The ohmic values of the resistive elements are determined, of course, by the width and length of the diffused elements and by the doping impurity concentration. Silicon oxide is again formed in the openings in the silicon oxide layer 280, and a third silicon oxide removal forms openings in the silicon oxide layer 280 for the diffusion of the transistor emitter regions and for access to the transistor collector regions. It is to be noted that the silicon oxide over the resistive element 201 is not so thick as the silicon oxide immediately adjacent thereto. This is an important feature in the practice of this invention.

In Figure 18d, an N-type dopant is diffused through the silicon oxide layer 280 forming the N-type emitter regions 231 and 232 in the base region 233 and the N-type emitter regions 241 and 242 in the base region 243. N-type diffusion also occurs in the already N-type collector regions 234 and 244. Silicon oxide is again formed in all openings in the silicon oxide layer 280. At this point all active and passive elements have been

formed by using master photomask patterns. Two special photomask patterns can now be used in providing the ohmic contacts and leads peculiar to the desired circuit.

In Figure 18e a special photomask has been used to provide contact surfaces on the circuit elements. A contact surface is not provided on the emitter 41 since it is not needed in this circuit. The contact surfaces on the resistive elements 201-207 are selected to give the desired ohmic values for the resistors R_1 and R_2. Note in Figure 18e that the silicon oxide is not only removed from the resistive element 201 to allow for the contact 211 thereon, but also silicon oxide is removed from the silicon oxide layer 280 adjacent to the resistor element 201. This excess removal of silicon oxide is required to insure adequate contact surface on the resistor element 201 despite photomask line-up tolerances. Since the silicon oxide thickness adjacent to the resistive element 201 is greater than the silicon oxide thickness removed, the substrate area immediately adjacent to the area for contact 211 on resistive element 201 remains protected by silicon oxide. Though not shown in Figure 18e, this novel technique for providing a contact surface can be utilized in providing the contact surfaces to the transistor elements, particularly the emitters which are the smallest diffused regions.

In Figure 18f contacts and leads are formed by depositing a metal vapor on the wafer surface, masking the desired metal, and removing the unwanted metal by etching. Another special photomask is used in the masking of the desired metal. Shown in Figure 18f are the contact 211 and the ohmic leads 221-226.

The novel technique for providing the contact surface on the resistive element 201 for the ohmic contact 211 may be better visualized with reference to Figures 18g-18i. Shown are enlarged cross-sectional views of the resistive element 201 taken along the sectional line 3-3 of Figure 17. In Figure 18g the resistive element 201 is formed by diffusing a dopant through the opening in the silicon oxide layer 280 into the epitaxial layer 270. Note that the dopant diffuses under either side of the silicon oxide layer 280 thus creating a doped region which is wider that the width of the opening in the silicon oxide layer 280.

In Figure 18h silicon oxide is re-formed above the resistive element 201 in the opening in the silicon oxide layer 280. The thickness of the silicon oxide above the resistive element 201 may be only about one fifth the thickness of the silicon oxide layer 280 adjacent thereto.

In Figure 18i a contact surface is provided by masking the silicon oxide layer 280 with an etch resistant coating 285 except for a strip on the silicon oxide layer 280 extending laterally across the desired contact surface on the resistive element 201. The criticalness of photomask line-up tolerance in providing an adequate contact surface is reduced because the unmasked strip on the silicon oxide layer is wider than the desired contact surface width by more than twice the line-up tolerance. An etchant is applied to remove the unmasked silicon oxide. The etching process is controlled so that all the silicon oxide on the contact surface of the resistive element 201 is removed, but the substrate adjacent to the contact surface remains covered by the silicon oxide layer 280. The etching process also increases the width of the opening in the silicon oxide layer 280. However, the contact surface remains entirely on the resistive element 201 because the doped region is wider than the opening in the silicon oxide layer 280.

The novel method for providing contacts to integrated circuit resistors illustrated herein permits improved resistor geometries. As exemplified in the resistors R_1 and R_2 in the above-illustrative embodiment, resistors with uniform cross-sectional areas can be utilized. The accuracy of resistors with multiple contacts is improved. Since enlarged resistor portions are not required for line-up clearance around the resistor contact area, the resistor-substrate capacitance is reduced. While only resistor contacts have been illustrated herein, contacts to other integrated circuit elements, such as transistors, can be provided in a similar manner.

Although the above description of the process for manufacturing the small geometry diodes and the small geometry transistor structures have been referenced to a P-N or PNP type diffusion, it will be appreciated that it is equally applicable to N-P and NPN type diffusions.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A method of making a semiconductor device in which:

(a) a first layer of insulating material is formed on one surface of a semiconductor body;

(b) a portion of the insulating material is removed to form a first slot exposing a corresponding portion of the semiconductor body;

(c) a second layer of insulating material is formed on the surface of the semi-

formed by using master photomask patterns. Two special photomask patterns can now be used in providing the ohmic contacts and leads peculiar to the desired circuit.

In Figure 18e a special photomask has been used to provide contact surfaces on the circuit elements. A contact surface is not provided on the emitter 41 since it is not needed in this circuit. The contact surfaces on the resistive elements 201-207 are selected to give the desired ohmic values for the resistors R_1 and R_2. Note in Figure 18e that the silicon oxide is not only removed from the resistive element 201 to allow for the contact 211 thereon, but also silicon oxide is removed from the silicon oxide layer 280 adjacent to the resistor element 201. This excess removal of silicon oxide is required to insure adequate contact surface on the resistor element 201 despite photomask line-up tolerances. Since the silicon oxide thickness adjacent to the resistive element 201 is greater than the silicon oxide thickness removed, the substrate area immediately adjacent to the area for contact 211 on resistive element 201 remains protected by silicon oxide. Though not shown in Figure 18e, this novel technique for providing a contact surface can be utilized in providing the contact surfaces to the transistor elements, particularly the emitters which are the smallest diffused regions.

In Figure 18f contacts and leads are formed by depositing a metal vapor on the wafer surface, masking the desired metal, and removing the unwanted metal by etching. Another special photomask is used in the masking of the desired metal. Shown in Figure 18f are the contact 211 and the ohmic leads 221-226.

The novel technique for providing the contact surface on the resistive element 201 for the ohmic contact 211 may be better visualized with reference to Figures 18g-18i. Shown are enlarged cross-sectional views of the resistive element 201 taken along the sectional line 3-3 of Figure 17. In Figure 18g the resistive element 201 is formed by diffusing a dopant through the opening in the silicon oxide layer 280 into the epitaxial layer 270. Note that the dopant diffuses under either side of the silicon oxide layer 280 thus creating a doped region which is wider that the width of the opening in the silicon oxide layer 280.

In Figure 18h silicon oxide is re-formed above the resistive element 201 in the opening in the silicon oxide layer 280. The thickness of the silicon oxide above the resistive element 201 may be only about one fifth the thickness of the silicon oxide layer 280 adjacent thereto.

In Figure 18i a contact surface is provided by masking the silicon oxide layer 280 with an etch resistant coating 285 except for a strip on the silicon oxide layer 280 extending laterally across the desired contact surface on the resistive element 201. The criticalness of photomask line-up tolerance in providing an adequate contact surface is reduced because the unmasked strip on the silicon oxide layer is wider than the desired contact surface width by more than twice the line-up tolerance. An etchant is applied to remove the unmasked silicon oxide. The etching process is controlled so that all the silicon oxide on the contact surface of the resistive element 201 is removed, but the substrate adjacent to the contact surface remains covered by the silicon oxide layer 280. The etching process also increases the width of the opening in the silicon oxide layer 280. However, the contact surface remains entirely on the resistive element 201 because the doped region is wider than the opening in the silicon oxide layer 280.

The novel method for providing contacts to integrated circuit resistors illustrated herein permits improved resistor geometries. As exemplified in the resistors R_1 and R_2 in the above-illustrative embodiment, resistors with uniform cross-sectional areas can be utilized. The accuracy of resistors with multiple contacts is improved. Since enlarged resistor portions are not required for line-up clearance around the resistor contact area, the resistor-substrate capacitance is reduced. While only resistor contacts have been illustrated herein, contacts to other integrated circuit elements, such as transistors, can be provided in a similar manner.

Although the above description of the process for manufacturing the small geometry diodes and the small geometry transistor structures have been referenced to a P-N or PNP type diffusion, it will be appreciated that it is equally applicable to N-P and NPN type diffusions.

While the invention has been described with reference to specific methods and embodiments, it is to be understood that this description is not to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS :—

1. A method of making a semiconductor device in which:

(a) a first layer of insulating material is formed on one surface of a semiconductor body;

(b) a portion of the insulating material is removed to form a first slot exposing a corresponding portion of the semiconductor body;

(c) a second layer of insulating material is formed on the surface of the semi-

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conductor body within the slot;

(d) insulating material is removed to form a second slot intersecting the first slot and to expose the semiconductor body surface only over the area of intersection of the first and second slots, and

(e) an impurity is diffused into the portion of the semiconductor body exposed by the said step (b) or by the said step (d) or separately into both the said portions, the or each diffusion taking place following the step concerned.

2. A method according to claim 1, in which impurity having conduction carriers of one conductivity type is diffused into the semiconductor body through the slot formed by the said step (b), in which impurity having conduction carriers of opposite conductivity type is diffused into the semiconductor body in the portion exposed by the said step (d), and in which the two diffusions result in diffused regions defining a P-N junction.

3. A method according to claim 1 or claim 2, including the step of forming an ohmic metallic contact on to the said semiconductor body surface area exposed at the intersection of the first and second slots and in contact with the or one of the diffused region(s), the contact extending on to the first layer of insulating material.

4. A method according to any one of the preceding claims, in which the semiconductor body is of intrinsic semiconductor material.

5. A method of making a semiconductor device in which:—

a first layer of insulating material is formed on a surface of an intrinsic semiconductor body;

a portion of the first insulating layer is removed to form a first slot exposing a corresponding surface portion of the said body;

a second, thinner layer of insulating material is formed on the semiconductor body surface within the first slot;

separate portions of insulating material are selectively removed to form, respectively, second and third slots intersecting the first slot to product first and second holes in the second insulating layer exposing the semiconductor body surface only at the respective loci of intersection of the first slot with the second and third slots; and

impurity material is diffused into the semiconductor body through the first and second holes to form substantially beneath those holes first and second regions of desired impurity characteristics.

6. A method according to claim 5, in which the first and second diffused regions have conduction carriers of respectively opposite conductivity types.

7. A method according to claim 5, in which following formation of the first slot an impurity region is diffused into the semiconductor body through the first slot, which region has conduction carriers of conductivity type opposite that of each of the said first and second diffused regions.

8. A method according to any one of the preceding claims, in which the first slot extends at right angles to the or each other slot.

9. A method of making a semiconductor device in which:—

a first layer of insulating material is formed on a surface of an intrinsic semiconductor body;

a portion of the first insulating layer is removed to form a first slot exposing a corresponding surface portion of the said body, and an impurity is diffused into the body through the first slot to form a first diffused region substantially beneath the first slot;

a second thinner layer of insulating material is formed on the semiconductor body surface within the first slot;

insulating material is selectively removed to form a second slot intersecting the first slot to produce a first hole in the second insulating layer exposing the semiconductor body surface only at the locus of intersection of the first and second slots and an impurity is diffused into the semiconductor body through the first hole to form a second diffused region substantially beneath the first hole and within the first diffused region;

a third layer of insulating material is formed on the semiconductor surface within the first hole;

insulating material is removed to form a third slot of lesser width than and extending along the second slot to produce a second hole in the third insulating layer exposing the semiconductor body surface only at the locus of intersection of the first and third slots and an impurity is diffused into the semiconductor body through the second hole to form a third diffused region substantially beneath the second hole and within the second diffused region,

and in which the first and third diffused regions each have a conductivity type opposite that of the second diffused region.

10. A method according to claim 9, in which the second and third slots extend substantially parallel to each other and at right angles to the first slot.

11. A method according to any one of claims 7, 9 and 10, in which at least the second insulating layer is formed as a result of the diffusion of impurity through the first slot.

12. A method according to any one of claims 5-11, in which individual ohmic contacts are connected to each of the diffused regions.

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13. A method according to any one of the preceding claims, in which each insulating layer is composed of the same material.

14. A method according to claim 13, in which the insulating layers are composed of an oxide material.

15. A method of forming an intergated circuit device including a plurality of circuit elements adjacent one surface of a semiconductor body wherein at least one of the circuit elements is a resistor formed by a method according to claim 1, in which impurity is diffused into the semiconductor body through the slot formed by the said step (b) to provide the resistor, and in which an ohmic metal contact is deposited on the surface portion of the semi-conductor body exposed by the said step (d) to provide an ohmic connection with the said resistor.

16. A semiconductor device manufactured by a method according to any one of claims 1-5, 8, and 12-15.

17. A P-I-N diode manufactured by a method according to claim 6, and having ohmic contacts attached to the respective first and second diffused regions.

18. A transistor manufactured according to any of the claims 7, 9, 10 and 11, and having ohmic contacts attached to the respective diffused regions.

19. A method of manufacturing a semiconductor device substantially as described herein with reference to and as illustrated by Fgs. 1-4; or by Figs. 5-7; or by Figs. 8-10; or by Figs. 11 and 12; or by Figs. 13-15 of the accompanying drawings.

20. A method of manufacturing a semiconductor integrated circuit device substantially as described herein with reference to and as illustrated by Figs. 16-18 of the accompanying drawings.

21. A semiconductor device manufactured by any one of the methods claimed in claim 19 and claim 20.

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