ABSTRACT

METHOD TO FORM A SELF-ALIGNED CMOS INVERTER USING VERTICAL DEVICE INTEGRATION

A substrate comprises silicon implanted oxide (SIMOX) wherein oxide is sandwiched between underlying and overlying silicon layers. Ions are selectively implanted into a first part of the overlying silicon layer to form an NMOS drain, channel region, and source and into a second part to form a PMOS drain, channel region, and source. The drain is formed directly overlying the oxide layer, the channel region is formed overlying the drain, and the source is formed overlying the channel region. The PMOS transistor drain contacts the NMOS transistor drain. A gate trench is etched through the NMOS and PMOS sources and channel regions, terminating at the NMOS and PMOS drains and exposing the sidewalls of the NMOS and PMOS channel regions. A polysilicon layer is deposited over gate oxide and etched back to form polysilicon sidewalls and to thereby form gates for the closely-spaced, vertical NMOS and PMOS transistor pair.

Figure 12