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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Process for Etching Semiconductors in the Fabrication of Miniature Semiconductor Networks Comprising a Single Semiconductor Block

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the fabrication of miniature semiconductor networks wherein the electrical circuit, which includes at least two individual circuit elements, is formed out of a single block of semiconductor material.

More particularly the invention relates to an etching process which uniquely employs photomasking in combination with electrolytic etching techniques to selectively etch portions of semiconductor blocks with sufficient definition and resolution to satisfy the stringent tolerances required by such miniature semiconductor networks.

In recent years there has been an increasing trend toward miniaturization of electronic components, especially in the computer field. Included in this trend are the development of the transistor, the cryotron, the printed circuit and various compact computer memory devices, to name but a few.

A recent and highly valuable innovation is the miniature semiconductor network where the complete circuit is formed out of a single small block of semiconductor material. The terms "electrical circuit" and "semiconductor network", as used throughout this application, are to be taken to mean an interconnection of at least two individual electrical circuit elements such as transistors, diodes, resistors and capacitors. Thus, examples of an electrical circuit or semi-

conductor network according to the terminology used herein are a transistor and a resistor connected together; a resistor and a capacitor connected together; a transistor having a diode connected to one of its terminals, a capacitor connected to a second terminal, and a parallel resistor and capacitor connected to the third terminal.

In the miniature semiconductor network all circuit elements are formed out of, on, or completely within, a single small block of semiconductor material. This is accomplished simply by providing preselected patterns of conductivity zones, grooves, holes, cutaway portions, and terminal regions in a block of semiconductor material according to the particular combination of circuit elements desired. The present invention concerns the manufacture of such miniature semiconductor networks and has particular reference to the forming of grooves, holes and cutaway portions in the block of semiconductor material. These miniature semiconductor networks and their manufacture are fully disclosed in the Specification of our copending patent application No. 3633/60 (Serial No. 945,734).

In the past, photoengraving techniques have been used to etch small intricate patterns into the surfaces of semiconductors. By such methods the surface of the semiconductor to be etched is coated with a photosensitive material to form a resist, and the surface is exposed to light through a stencil. The portions of the coating protected from the light by the stencil are dissolved away by a suitable developing liquid, while those portions of the coating which have been exposed to light are insoluble in the developer and remain on the semiconductor. A corrosive fluid, such as nitric acid and hydrofluoric acid, which can etch the surface to be engraved but which

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cannot attack the protective coating, is then used to etch the stencil pattern into the semiconductor.

The above method has several desirable characteristics. First, extreme fineness of detail in the photoresist pattern itself is obtainable. Also, this etching method leaves a smooth and mechanically unstrained semiconductor surface, with the result that better electrical properties are obtained than would be possible using cutting or abrading methods which leave strained or imperfect surfaces.

However, the method is not free from drawbacks. For one thing, when the etching is done with strong acids, the resist coating, in addition to the semiconductor material, is often attacked and partly destroyed. This changes the resist pattern, and thus the extreme fineness in the detail and resolution achieved in the pattern by the photomaking process will be lost on account of the highly corrosive nature of the chemical etchants. It is also possible that portions of the resist will be completely removed, which causes even greater discrepancies between the etched semiconductors and the desired result. Another disadvantage of the acid chemical etching techniques accrues from a phenomenon known as undercutting. This occurs when the acid etchant attacks the semiconductor material with essentially equal intensity wherever it contacts the semiconductor. Thus, when a groove is etched it tends to become wider at the top than at the bottom since the etchant attacks the side walls of the groove, as well as the bottom. This undercutting is extremely difficult to control and results in loss of definition and resolution in the pattern to be etched because of the uncontrollable variations in the amounts of material underlying the mask which are removed from the semiconductor. An additional objection in the use of the prior art chemical etch is the fact that when the semiconductor material is silicon there is a marked tendency for the resist to peel off during the chemical etch process due to the concentrated acids used, whereas with the electrolytic etch of this invention the strong tendency for the resist to peel off of the silicon body has been eliminated by the use of a different type of solution and in employing a different phenomena as the basis of operation.

The above drawbacks may not be troublesome in the manufacture of diodes or transistors, but due to the extreme tolerance requirements for the cutaway portions of the miniature semiconductor networks, the drawbacks and shortcomings of the above-described photomasking acid chemical etching process become serious when used in the manufacture of miniature semiconductor

networks.

The present invention provides a method for the selective etching of semiconductors in which the high degree of definition and resolution necessary in the manufacture of the miniature semiconductor networks is obtained.

The present invention is a method for the selective etching of a semiconductor block to form a miniature semiconductor network comprising a single block of semiconductor material, said method comprising applying a photosensitive etch-resistant coating to the surface of the semiconductor block to be etched, exposing portions of said coating to light, developing the latent photographic image, removing the portions of said coating not exposed to light, placing a first electrode in an electrolyte solution, placing said semiconductor block in said electrolyte solution to form a second electrode, said second semiconductor block being positioned in such a manner that the portions of said semiconductor block which are exposed to light are in parallel alignment with said first electrode, and subjecting said semiconductor block to electrolytic etching whereby the etching of semiconductor material occurs in the region of said semiconductor block not covered by photosensitive etch-resistant coating in such a manner as to define a sharp edge adjacent the masked area.

Additional advantages and characteristic features of the invention will become readily apparent from the following detailed description of a preferred embodiment of the invention when taken in conjunction with the appended drawings, in which:

Figures 1, 2 and 4 are side views of a block of semiconductor material showing some of the respective stages in the fabrication process of the present invention;

Figure 3 is a side view of a block of semiconductor material which has been etched by acid chemical methods and which illustrates the phenomenon of undercutting as experienced by prior art methods; and

Figure 5 illustrates one arrangement used in carrying out the electrolytic etching method of the present invention.

Relating the steps of the invention in more detail, the block of semiconductor material to be processed is first cut to the desired size, after which it is lapped, polished, and washed. Then a photosensitive etch resistant coating is applied to a surface of the semiconductor block. This is shown in Figure 1 where a semiconductor block 10 is coated with a photosensitive resist 11. The block is dried in air at room temperature for about ten minutes, or, alternatively, held about eight inches from a 250 watt infrared heat lamp for three to five minutes. A stencil or photographic mask having open or trans-

parent areas according to the pattern desired to be etched in the semiconductor block, is placed in intimate contact with the coated side of the semiconductor block and held there, for example, by use of a vacuum contact frame. The coated semiconductor block is then exposed to light (preferably from a 20 amp double-arc lamp) for approximately three minutes. The desirable lamp to semiconductor distance is 30 inches.

After exposure, the stencil is removed and the semiconductor block is placed in a developing solution, the semiconductor block is rinsed under a stream of water which causes the part of the resist that was not exposed to light to be dissolved and washed away. In Figure 2 there is shown the semiconductor block 10 having portions 11 of the resist remaining, with the portions 12 where the resist not exposed to light is removed. After washing, the semiconductor block may be baked in an oven at 150°C. for about 10 minutes in order to harden, or cure the resist.

The semiconductor block with the photoresist mask thereon, as shown in Figure 2, is then ready for etching. By prior art techniques, the semiconductor block would be submerged in an acid chemical etch until material in the region of the block had been removed to the desired depth. However, such acid type chemical etches will usually cause severe undercutting as illustrated in Figure 3. In Figure 3, it may be seen that the acid type chemical etchant has removed material from the unmasked areas of the block to form grooves 13. However, it will be noted that material has been removed from the sides as well as from the bottom of the grooves so that severe undercutting, as illustrated at 14, results.

By the method of the present invention the masked block is etched by electrolytic methods as shown in Figure 5. As is shown in Figure 5, the semiconductor block 10 having regions 11 covered by the resist is immersed in a container 20 filled with an etching solution 21. For germanium, an etching solution of approximately 20% phosphoric acid may be used, while for silicon the usable range of concentrations in the solution may consist of 20-40% sulphuric acid and 1-8% ammonium bifluoride in deionized water, the preferred values being 31% and 3.2%, respectively. Electrode 22 is attached to the semiconductor 10, while the other electrode 23 is merely immersed in the solution at a point spaced from the semiconductor block 10. A DC voltage is then applied between the electrodes 22 (positive) and 23 (negative). A voltage causing a current density of .5 to 2.0 amps per square cm, has been found satisfactory. Electrolytic etching then ensues in those regions 12 of the semiconductor 10 not

covered with the resist 11. Since the resist is a good insulator and will not pass current directly into the solution, etching will occur only in the unmasked regions. Further, it has been found that undercutting in the etched area is greatly reduced by the electrolytic etching method.

A sample electrolytically etched semiconductor block is shown in Figure 4, where grooves 13 have been etched into the surface of the semiconductor block 10. These regions correspond to surface portions 12 of the semiconductor block shown in Figure 2 with very minute undercutting and with substantially straight sharp upper edges adjacent the resist. When the resist material is ultimately removed, the grooves 13 will have the desired sharp juncture with the top surface of the semiconductor block 10.

It has been found that by using a straight vertical electrode 23 of one polarity and inserting the semiconductor block 10 into the electrolyte in a straight vertical position or parallel to the first electrode as shown in Figure 5 so that it acts as the second electrode 22, then the anodic dissolution of the unmasked areas 12 will take place predominately in a direction parallel to the electrode 23 so that straight wall cavities 13 as shown in Figure 4 will result and the deep undercutting 14 as seen in Figure 3 will not take place.

WHAT WE CLAIM IS:—

1. A method for the selective etching of a semiconductor block to form a miniature semiconductor network comprising a single block of semiconductor material, said method comprising applying a photo-sensitive etch-resistant coating to the surface of the semiconductor block to be etched, exposing portions of said coating to light, developing the latent photographic image, removing the portions of said coating not exposed to light, placing a first electrode in an electrolyte solution, placing said semiconductor block in said electrolyte solution to form a second electrode, said second semiconductor block being positioned in such a manner that the portions of said semiconductor block which are exposed to light are in parallel alignment with said first electrode, and subjecting said semiconductor block to electrolytic etching whereby the etching of semiconductor material occurs in the region of said semiconductor block not covered by photosensitive etch-resistant coating in such a manner as to define a sharp edge adjacent the masked area.

2. A method according to claim 1, wherein the semiconductor block is germanium and wherein said electrolytic etching solution contains approximately 20% phosphoric acid.

3. A method according to claim 1, wherein the semiconductor block is silicon

parent areas according to the pattern desired to be etched in the semiconductor block, is placed in intimate contact with the coated side of the semiconductor block and held there, for example, by use of a vacuum contact frame. The coated semiconductor block is then exposed to light (preferably from a 20 amp double-arc lamp) for approximately three minutes. The desirable lamp to semiconductor distance is 30 inches.

After exposure, the stencil is removed and the semiconductor block is placed in a developing solution, the semiconductor block is rinsed under a stream of water which causes the part of the resist that was not exposed to light to be dissolved and washed away. In Figure 2 there is shown the semiconductor block 10 having portions 11 of the resist remaining, with the portions 12 where the resist not exposed to light is removed. After washing, the semiconductor block may be baked in an oven at 150°C. for about 10 minutes in order to harden, or cure the resist.

The semiconductor block with the photoresist mask thereon, as shown in Figure 2, is then ready for etching. By prior art techniques, the semiconductor block would be submerged in an acid chemical etch until material in the region of the block had been removed to the desired depth. However, such acid type chemical etches will usually cause severe undercutting as illustrated in Figure 3. In Figure 3, it may be seen that the acid type chemical etchant has removed material from the unmasked areas of the block to form grooves 13. However, it will be noted that material has been removed from the sides as well as from the bottom of the grooves so that severe undercutting, as illustrated at 14, results.

By the method of the present invention the masked block is etched by electrolytic methods as shown in Figure 5. As is shown in Figure 5, the semiconductor block 10 having regions 11 covered by the resist is immersed in a container 20 filled with an etching solution 21. For germanium, an etching solution of approximately 20% phosphoric acid may be used, while for silicon the usable range of concentrations in the solution may consist of 20-40% sulphuric acid and 1-8% ammonium bifluoride in deionized water, the preferred values being 31% and 3.2%, respectively. Electrode 22 is attached to the semiconductor 10, while the other electrode 23 is merely immersed in the solution at a point spaced from the semiconductor block 10. A DC voltage is then applied between the electrodes 22 (positive) and 23 (negative). A voltage causing a current density of .5 to 2.0 amps per square cm, has been found satisfactory. Electrolytic etching then ensues in those regions 12 of the semiconductor 10. not

covered with the resist 11. Since the resist is a good insulator and will not pass current directly into the solution, etching will occur only in the unmasked regions. Further, it has been found that undercutting in the etched area is greatly reduced by the electrolytic etching method.

A sample electrolytically etched semiconductor block is shown in Figure 4, where grooves 13 have been etched into the surface of the semiconductor block 10. These regions correspond to surface portions 12 of the semiconductor block shown in Figure 2 with very minute undercutting and with substantially straight sharp upper edges adjacent the resist. When the resist material is ultimately removed, the grooves 13 will have the desired sharp juncture with the top surface of the semiconductor block 10.

It has been found that by using a straight vertical electrode 23 of one polarity and inserting the semiconductor block 10 into the electrolyte in a straight vertical position or parallel to the first electrode as shown in Figure 5 so that it acts as the second electrode 22, then the anodic dissolution of the unmasked areas 12 will take place predominately in a direction parallel to the electrode 23 so that straight wall cavities 13 as shown in Figure 4 will result and the deep undercutting 14 as seen in Figure 3 will not take place.

WHAT WE CLAIM IS:—

1. A method for the selective etching of a semiconductor block to form a miniature semiconductor network comprising a single block of semiconductor material, said method comprising applying a photo-sensitive etch-resistant coating to the surface of the semiconductor block to be etched, exposing portions of said coating to light, developing the latent photographic image, removing the portions of said coating not exposed to light, placing a first electrode in an electrolyte solution, placing said semiconductor block in said electrolyte solution to form a second electrode, said second semiconductor block being positioned in such a manner that the portions of said semiconductor block which are exposed to light are in parallel alignment with said first electrode, and subjecting said semiconductor block to electrolytic etching whereby the etching of semiconductor material occurs in the region of said semiconductor block not covered by photosensitive etch-resistant coating in such a manner as to define a sharp edge adjacent the masked area.

2. A method according to claim 1, wherein the semiconductor block is germanium and wherein said electrolytic etching solution contains approximately 20% phosphoric acid.

3. A method according to claim 1, wherein the semiconductor block is silicon



and wherein the electrolytic etching solution comprises from about 20 to about 40% sulphuric acid, from about 2/3 of 1% to about 5-1/3% fluoride ion, and from about 5 79-1/3 to about 54-2/3% of deionized water.

4. A method for the selective etching of a semiconductor block to form a miniature semiconductor network comprising a single block of semiconductor material, substantially as hereinbefore described with reference to Figs. 1, 2, 4 and 5 of the accompanying drawings.

5. A miniature semiconductor network

comprising a single block of semiconductor material when formed by the selective etching of a semiconductor material according to the method of any preceding claim. 15

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