WHAT IS CLAIMED IS:

1. A non-volatile memory device, comprising:

a memory cell array configured to store initialization information for the non-volatile memory device in memory cells connected to a plurality of word lines;

a control circuit configured to control application of a first read voltage to a selected word line and to control application of a second read voltage to unselected word lines in an initialization information read operation of reading the initialization information; and

a voltage generator configured to decrease a source voltage to generate the second read voltage in response to a voltage control signal provided from the control circuit in the initialization information read operation.

2. The non-volatile memory device of claim 1, wherein the memory cells are single level cells storing one-bit data.

3. The non-volatile memory device of claim 2, wherein the first read voltage is set to have a voltage level for discriminating between erase states and program states of the single level cells.

4. The non-volatile memory device of claim 3, wherein the first read voltage is set as a ground voltage.

5. The non-volatile memory device of any one of claims 1 to 4, wherein the control circuit is configured to detect power-up to generate the voltage control signal.

6. The non-volatile memory device of any one of claims 1 to 5, wherein the voltage generator is configured to allow the source voltage not to be pumped in response to the voltage control signal.

7. The non-volatile memory device of any one of claims 1 to 6, wherein the voltage generator comprises:

a voltage divider including a plurality of resistors serially connected between the source voltage and a ground voltage, the voltage divider being configured to generate division voltages at both ends of each of the plurality of resistors; and

a selector configured to output one of the division voltages as the second read voltage in response to the voltage control signal.

8. The non-volatile memory device of any one of claims 1 to 6, wherein the voltage generator comprises:

a first resistor connected between the source voltage and a node through which the second read voltage is output;

a plurality of resistors serially connected between the node and a ground voltage; and

a plurality of transistors connected across the plurality of resistors, the voltage control signal being provided as bit information to a gate of each of the plurality of transistors.

9. The non-volatile memory device of any one of claims 1 to 6, wherein the voltage generator comprises:

a first resistor connected between the source voltage and a node through which the second read voltage is output;

a plurality of resistors connected in parallel between the node and a ground voltage;

and

a plurality of transistors connected across the plurality of resistors, the voltage control signal being provided as bit information to a gate of each of the plurality of transistors.

10. The non-volatile memory device of any one of claims 1 to 9, further comprising a set register storing the initialization information read through the initialization information read operation.

11. The non-volatile memory device of any one of claims 1 to 10, wherein the initialization information comprises protection information about inhibition or permission of program or erase operations performed on the memory cell array, trimming data for trimming an operating voltage level in a program, read, or erase operation mode of the non-volatile memory device, column repair information for repairing a failed bit line of the non-volatile memory device, or bad block information identifying bad memory cells of the non-volatile memory device.

12. A read method of a non-volatile memory device, the read method comprising:

detecting power-up;

in response to the detected power-up, reading initialization information for the non-volatile memory device which is stored in first memory cells of a memory cell array of the non-volatile memory device; and

when reading the initialization information,

generating a first read voltage which is to be provided to a selected word line of a plurality of word lines which is connected to the first memory cells, and

generating a second read voltage which is to be provided to unselected word

lines of the plurality of word lines which are not connected to the first memory cells,

wherein the second read voltage is generated by reducing a source voltage.

13. The read method of claim 12, further comprising allowing the source voltage not to be pumped in response to a voltage control signal associated with the power-up.

14. The read method of claim 12 or claim 13, wherein the generating of the second read voltage comprises dividing the source voltage, in response to a voltage control signal, to generate the second read voltage.

15. The read method of any one of claims 12 to 14, wherein the first memory cells are single level cells storing one-bit data.

16. The read method of claim 15, wherein the first read voltage is set to have a voltage level for discriminating between erase states and program states of the single level cells.

17. The read method of claim 16, wherein the first read voltage is set as a ground voltage.

18. The read method of claim 17, wherein the second read voltage is set to have at least one voltage level between a ground voltage and the source voltage.

19. The read method of any one of claims 12 to 18, further comprising setting the read initialization information in a set register.

20. The read method of any one of claims 12 to 19, wherein the initialization information comprises protection information about inhibition or permission of program or erase operations on the non-volatile memory device, trimming data for trimming an operating voltage level in a program, read, or erase operation mode for the non-volatile memory device, column repair information for repairing a failed bit line of the non-volatile memory device, or bad block information identifying bad memory cells of the non-volatile memory device.