CLAIMS

1. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having at least first and second transistors, wherein each of the transistors includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate,

a second diffusion region in the device region displaced away from the second side of the gate, wherein the first and second diffusion regions comprise dopants of a first polarity type, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region and a second device well disposed within the first device well;

a drift well which encompasses the second diffusion region, wherein edges of the drift well do not extend below the gate and is away from a channel region; and

a drain well having dopants of the first polarity type is disposed under the second diffusion region and within the first device well.

2. The device of claim 1 wherein the first device well comprises dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

3. The device of claim 2 wherein the first polarity type comprises n type and the second polarity type comprises p type.

4. The device of claim 1 wherein the second device well encompasses at least the first diffusion region and a part of the gate.

5. The device of claim 4 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

6. The device of claim 1 wherein the first device well and the drift well comprise dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

7. The device of claim 6 wherein the first polarity type comprises n type and the second polarity type comprises p type.

8. The device of claim 1 wherein the drain well is narrower than the drift well.

9. The device of claim 1 wherein a first edge of the drift well is below the center of the drift isolation region of the first transistor and a second edge of the drift well is below the center of the drift isolation region of the second transistor.

10. The device of claim 9 wherein the drain well is disposed within the drift well and is contiguous with the second diffusion region.

11. The device of claim 10 wherein a separation distance between a first edge of the drain well and the first edge of the drift well is the same as a separation distance between a second edge of the drain well and the second edge of the drift well.

12. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having at least first and second transistors, wherein each of the transistors includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate,

a second diffusion region in the device region displaced away from the second side of the gate, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region and a second device well disposed within the first device well;

a drift well which encompasses the second diffusion region, wherein edges of the drift well do not extend below the gate and is away from a channel region; and

a drain well disposed under the second diffusion region and within the drift well.

13. The device of claim 12 wherein:

the first device well comprises dopants of the first polarity type and the second device well comprises dopants of a second polarity type; and

the first and second diffusion regions comprise dopants of a first polarity type.

14. The device of claim 13 wherein the first polarity type comprises n type and the second polarity type comprises p type.

15. The device of claim 12 wherein a first edge of the drift well is below the center of the drift isolation region of the first transistor and a second edge of the drift well is below the center of the drift isolation region of the second transistor.

16. The device of claim 15 wherein the drain well is disposed within the drift well and is contiguous with the second diffusion region.

17. The device of claim 16 wherein a first edge 175a of the drain well is aligned with an edge of the drift isolation region of the first transistor which is away from the gate of the first transistor and a second edge 175b of the drain well is aligned with an edge of the drift isolation region of the second transistor which is away from the gate of the second transistor.

18. The device of claim 17 wherein a separation distance between the first edge of the drain well and the first edge of the drift well is the same as a separation distance between the second edge of the drain well and the second edge of the drift well.

CLAIMS

1. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having at least first and second transistors, wherein each of the transistors includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate,

a second diffusion region in the device region displaced away from the second side of the gate, the second diffusion region is disposed between adjacent second sides of the gates of the first and second transistors, wherein the first and second diffusion regions comprise dopants of a first polarity type, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region;

a drift well which encompasses the second diffusion region, wherein edges of the drift well do not extend below the second sides of the gates of the first and second transistors and is displaced away from channels of the transistors, the drift well comprises first polarity type dopants; and

a drain well having dopants of the first polarity type is disposed under the second diffusion region and disposed completely within the drift well.

2. The device of claim 1 further comprising a second device well disposed within the first device well, wherein the first device well comprises dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

3. The device of claim 2 wherein the first polarity type comprises n type and the second polarity type comprises p type.

4. The device of claim 1 further comprising a second device well disposed within the first device well, wherein the second device well encompasses at least the first diffusion region and a part of the gate.

5. The device of claim 4 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

6. The device of claim 4 wherein the first device well and the drift well comprise dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

7. The device of claim 6 wherein the first polarity type comprises n type and the second polarity type comprises p type.

8. The device of claim 1 wherein the drain well is narrower than the drift well.

9. The device of claim 1 wherein a first edge of the drift well is below the center of the drift isolation region of the first transistor and a second edge of the drift well is below the center of the drift isolation region of the second transistor.

10. The device of claim 9 wherein the drain well is contiguous with the second diffusion region.

11. The device of claim 10 wherein a separation distance between a first edge of the drain well and the first edge of the drift well is the same as a separation distance between a second edge of the drain well and the second edge of the drift well.

12. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having at least first and second transistors, wherein each of the transistors includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate,

a second diffusion region in the device region displaced away from the second side of the gate, the second diffusion region is disposed between adjacent second sides of the gates of the first and second transistors, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region;

a drift well which encompasses the second diffusion region, wherein edges of the drift well do not extend below the second sides of the gates of the first and second transistors and is displaced away from channels of the transistors, the drift well comprises first polarity type dopants; and

a drain well disposed under the second diffusion region and disposed completely within the drift well.

13. The device of claim 12 wherein:

the first device well comprises dopants of a first polarity type; and

the first and second diffusion regions comprise dopants of the first polarity type.

14. The device of claim 13 wherein the first polarity type comprises n type and the second polarity type comprises p type.

15. The device of claim 12 wherein a first edge of the drift well is below the center of the drift isolation region of the first transistor and a second edge of the drift well is below the center of the drift isolation region of the second transistor.

16. The device of claim 15 wherein the drain well is contiguous with the second diffusion region.

17. The device of claim 16 wherein a first edge 175a of the drain well is aligned with an edge of the drift isolation region of the first transistor which is away from the gate of the first transistor and a second edge 175b of the drain well is aligned with an edge of the drift isolation region of the second transistor which is away from the gate of the second transistor.

18. The device of claim 17 wherein a separation distance between the first edge of the drain well and the first edge of the drift well is the same as a separation distance between the second edge of the drain well and the second edge of the drift well.