DATA RECEIVING CIRCUIT, DATA RECEIVING SYSTEM, AND MEMORY DEVICE

Technical Field

Embodiments of the present application relate to the technical field of semiconductors, and in particular, to a data receiving circuit, a data receiving system, and a memory device.

Background

In memory applications, as a signal transmission rate becomes increasingly fast, a channel loss has a greater impact on signal quality, which easily leads to intersymbol interference. In addition, a difference in level between a data signal received by a data receiving circuit in a memory and a reference signal affects judgment of the data receiving circuit on the data signal, thereby affecting accuracy of a signal outputted by the data receiving circuit.

At present, an equalization circuit is usually configured to compensate for a channel, and the equalization circuit may select a continuous time linear equalizer (CTLE) or a decision feedback equalizer (DFE). However, the accuracy of the signal outputted by the equalization circuit currently used needs to be improved, receiving performance of the equalization circuit needs to be enhanced, and power consumption of the equalization circuit needs to be reduced.

Summary

Embodiments of the present application provide a data receiving circuit, a data receiving system, and a memory device, to at least facilitate reducing the power consumption of the data receiving circuit while improving the receiving performance of the data receiving circuit.