(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 May 2003 (15.05.2003)

PCT

(10) International Publication Number
WO 03/041127 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number: PCT/US02/35425

(22) International Filing Date:
6 November 2002 (06.11.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/986,167 7 November 2001 (07.11.2001) US

(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventors: **LANE, Richard, H.**; 204 W. State Street, Boise, ID 83702 (US). **MCDANIEL, Terry**; 1568 S. Riverstone Lane #303, Boise, ID 83706 (US).

(74) Agent: **SOFFEN, Stephen, A.**; Dickstein Shapiro Morin & Oshinsky LLP, 2101 L Street NW, Washington, DC 20037-1526 (US).

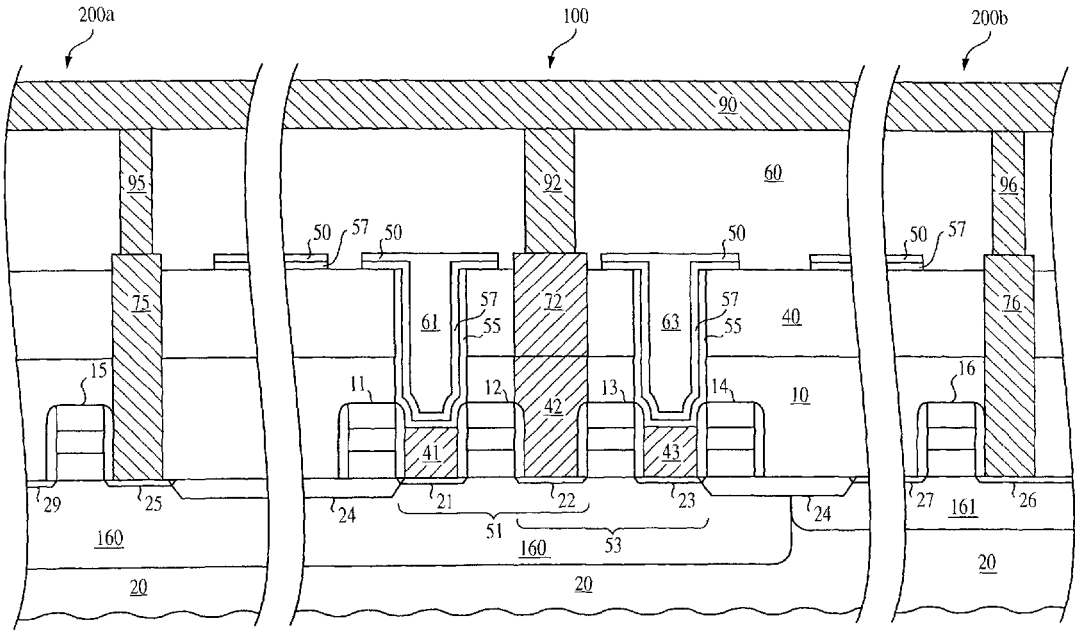
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROCESS FOR FORMING METALLIZED CONTACTS TO PERIPHERY TRANSISTORS



(57) Abstract: A process and apparatus directed to forming metal plugs in a peripheral logic circuitry area of a semiconductor device to contact both N+ and P+ doped regions of transistors in the peripheral logic circuitry area. The metal plugs are formed after all high temperature processing used in wafer fabrication is completed. The metal plugs are formed without metal diffusing into the active areas of the substrate. The metal plugs may form an oval slot as seen from a top down view of the semiconductor device.

WO 03/041127 A2