



159159

METHODS OF LASER ANNEALING A SEMICONDUCTOR LAYER AND SEMICONDUCTOR DEVICES PRODUCED THEREBY

FIELD OF THE INVENTION

5

The present invention relates to methods of laser annealing a semiconductor layer and semiconductor devices produced thereby.

BACKGROUND TO THE INVENTION

10

The production of semiconductor devices commonly includes one or more steps of laser annealing a semiconductor layer. Typically, but not exclusively, laser annealing is carried out to crystallize a non-single crystal semiconductor layer, such as an amorphous semiconductor layer of the semiconductor device before it is further processed. For example, in the production of flat panel display devices such as liquid crystal displays (LCDs) and organic light emitting diode (OLED) displays, an amorphous silicon (a-Si) layer may be laser annealed to form a polycrystalline silicon (p-Si) layer, from which thin film transistors (TFTs) that control the pixels of the LCD or OLED display may be formed.

20

Depending on the size of the layer to be annealed and the dimensions of the irradiating laser beam, laser annealing may be carried out in two or more sweeps or scans. Referring to Figure 1A-1C, a conventional laser annealing process is shown for an array of product regions (e.g. display panels). In the form illustrated, laser annealing is carried out on a 2×2 array 100 of product regions 102 comprising an a-Si semiconductor layer. The laser beam 104 used to anneal the array 100 may have a useful working area having a length x and width y . Typically, the maximum length x of the laser beam 104 is insufficient to irradiate the entire surface of the array 100. In most cases, therefore, the laser beam 104 is first scanned across a first area 106 (shown in shade) of the array 100 in the direction shown by arrow 108 in Figure 1B. The laser beam 104 is then scanned across a second area 110 (shown in shade) of the array 100 in the direction shown by arrow 112 in Figure 1C.

30



To ensure the entirety of the array 100 is annealed, the scanning of the laser beam 104 in the second area 110 is overlapped with the first area 106, creating an overlap region 114. Due to the dual exposure to laser annealing, the overlap region 114 generally exhibits undesirable characteristics, such as unacceptable variations in electrical or physical characteristics. To ensure these undesirable characteristics do not affect the products manufactured from the array, the overlap region 114 is conventionally arranged outside of the product regions 102, as shown in Figure 1C.

10 SUMMARY OF THE INVENTION

The method and device of the present invention are defined in the independent claims. Some optional features of the method and device are defined in the dependent claims.

15 A method incorporating the features of the independent claims may allow laser annealing to be carried out such that the overlap region does not exhibit undesirable electrical and physical characteristics. This in turn removes the limitation of having to arrange the overlap region outside of one or more product regions. In one disclosed embodiment, the method allows the entirety of a semiconductor layer to be laser
20 annealed using fewer laser scans than is conventionally required, thus reducing the time, energy and cost associated with the annealing process. Furthermore, the method also allows the gaps between product regions to be reduced since they no longer have to serve as overlap regions. This, in turn, allows a reduction of wasted semiconductor surface/material.

25

BRIEF DESCRIPTION OF THE FIGURES

Example embodiments of the method and device will now be described with reference to the accompanying figures in which:

30

Figures 1A, 1B and 1C are diagrams of an example semiconductor layer having an array of product regions undergoing conventional laser annealing,

Figure 2 is a flow chart illustrating the process flow of an example implementation of the method,

5 Figures 3A, 3B and 3C are cross-section diagrams of a semiconductor layer being annealed in accordance with one example implementation of the method,

 Figures 4A, 4B and 4C are cross-section diagrams of a semiconductor layer being annealed in accordance with another example implementation of the method,
10

 Figure 5A is a diagram of an array of product regions undergoing conventional laser annealing,

 Figure 5B is a diagram of an array of product regions undergoing laser annealing
15 in accordance with one implementation of the method,

 Figure 6A is a diagram of the overlapping of two laser scans during conventional laser annealing,

20 Figure 6B is a graph of the results of the conventional laser annealing shown in Figure 6A,

 Figure 6C is a diagram of the overlapping of two laser scans during laser annealing in accordance with one implementation of the method,
25

 Figure 6D is a graph of the results of the annealing of the implementation shown in Figure 6C, and

 Figure 7 is a diagram showing an example cross-section of the device.
30

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

An example method of laser annealing a semiconductor layer having a product region is shown in broad overview in Figure 2. The term 'product region' as used in this specification denotes a region of a semiconductor layer on or in which a semiconductor device or components of a semiconductor device have been or will be formed. Non-limiting examples of semiconductor devices include transistors, diodes, and sensors.

At step 200 of Figure 2, a nitrogen doped layer having a nitrogen concentration of at least 3×10^{20} atoms/cc is formed on the semiconductor layer. Laser irradiation in a low oxygen environment is then carried out at step 202 for a first area of the nitrogen doped layer, and at step 204 for a second area of the nitrogen doped layer, where a part of the second area overlaps with a part of the first area in at least one product region. A 'low oxygen environment' for the purposes of this specification is an environment in which the volume of oxygen is less than 2% of the total volume of the environment. In one form, the low oxygen environment has around 0.3% oxygen. In another form, the low oxygen environment has substantially 0% (i.e. 10ppm or less) oxygen.

One implementation of the method of Figure 2 will now be described with reference to Figures 3A-3C. In Figure 3A, a cross-section of an example semiconductor layer 300 having a product region 302 is shown attached to a substrate 304. Skilled persons will appreciate that a plurality of product regions 302 may be provided instead of a single product region 302. The substrate 304 may be, for example, a glass, silicon, quartz or sapphire substrate, and the semiconductor layer 300 may be a non-single crystal semiconductor layer, for example, an amorphous silicon (a-Si) layer, a microcrystalline silicon (μ -Si) layer, and polycrystalline silicon (p-Si) layer. The semiconductor layer 300 may be formed on the substrate 304 by sputtering, chemical vapour deposition (CVD, including specific types of CVD such as low pressure CVD, plasma CVD etc) or like processes, as will be known to skilled persons. It should be noted that the illustrated arrangement of layers in the figure is not essential and that the cross-section view shown does not represent the entirety of the semiconductor layer and its arrangement

over a substrate. For example, in certain regions, there may be additional layers provided above or beneath the semiconductor layer 300. Non-limiting examples of such additional layers include one or more metal layers, one or more additional a-Si layers, or one or more silicon oxide (SiO) and/or silicon nitride (SiN) layers.

5

Referring now to Figure 3B, a nitrogen doped layer 306 is shown formed on the semiconductor layer 300 in accordance with step 200 of Figure 2. The nitrogen doped layer 306 has a nitrogen concentration of at least 3×10^{20} atoms/cc. The applicant has found this to be a desirable concentration that reduces the occurrence of undesirable variations in characteristics, such as unacceptable ablation (i.e. loss of material from the surface) of the semiconductor layer when the laser annealing process is carried out in a low oxygen environment. The reason for annealing in a low oxygen environment will be explained later in this specification. In one example embodiment, the nitrogen concentration is between 3×10^{20} atoms/cc and 1×10^{22} atoms/cc. In another example embodiment, the nitrogen concentration is between 5×10^{20} atoms/cc and 5×10^{21} atoms/cc.

The nitrogen doped layer 306 may have a thickness in the range of 1nm to 30nm or in the range of 5nm to 15nm, for example. In one example form, the nitrogen doped layer 306 has a thickness of around 10nm. The range of 1nm to 30nm has been found by the applicant to allow large and uniform grain size to be obtained post-annealing, which improves the electron mobility of the annealed semiconductor layer, while ensuring ablation is reduced or avoided altogether. The specific range of 5nm to 15nm has been found by the applicant to allow the thickness of the nitrogen doped layer 306 to be more easily controlled during mass production of semiconductor devices, thus allowing improved operating margins. With regard to grain size, where the above ranges of thickness of the nitrogen doped layer 306 are implemented, the applicant has found it possible to obtain a desirably large and uniform grain size (i.e. not less than $0.2 \mu\text{m}$) post-annealing. In one example form, the grain size post-annealing is not less than $0.3 \mu\text{m}$.

In the exemplary implementation illustrated in Figure 3B, the nitrogen doped layer 306 is formed by depositing a further a-Si layer on the a-Si semiconductor layer 300, and doping the further a-Si layer with nitrogen. In other words, the semiconductor layer 300 is a first a-Si layer and the nitrogen doped layer 306 is a second a-Si layer that is doped with nitrogen. The second a-Si layer may be deposited by sputtering, chemical vapour deposition (CVD including specific types of CVD such as low pressure CVD, plasma CVD etc) or like processes, and may be doped with nitrogen using a CVD process, an ion implantation process or a plasma-doping process. Where CVD is used, the second a-Si layer may be deposited and doped substantially at the same time by introducing silane (SiH_4) gas and a nitrogen-based gas (e.g. N_2O) in a CVD chamber. For instance, the silane gas may be introduced at a first flow rate and N_2O gas may be introduced at a second flow rate. In this form, the nitrogen concentration and the thickness of the second a-Si layer may be controlled by controlling one or both of the first flow rate and the second flow rate. Also, in this form, the nitrogen doped layer may be provided in a single step, thus reducing the time and cost associated with forming the nitrogen doped layer. It is, however, not essential to both deposit and dope the second a-Si layer substantially at the same time. For instance, the second a-Si layer may be deposited by CVD first before being doped by ion implanting or plasma-doping nitrogen into the layer. In this form, the nitrogen concentration of the second a-Si layer may be controlled by controlling the energy used in the ion implantation or plasma-doping process.

Once the nitrogen doped layer 306 is formed, a first area of the nitrogen doped layer 306 is irradiated with a laser beam in a low oxygen environment, in accordance with step 202 of Figure 2, so as to anneal the first area and that portion of the a-Si semiconductor layer 300 which is substantially beneath the first area. The laser irradiation on the first area is represented in Figure 3B as solid arrows 308. A second area of the nitrogen doped layer 306 is then irradiated with a laser beam in a low oxygen environment, in accordance with step 204 of Figure 2, so as to anneal the second area and that portion of the a-Si semiconductor layer 300 which is substantially beneath the second area. The laser irradiation on the second area is represented in Figure 3B as dashed arrows 310. In one form, each of the annealing steps is carried out in an environment having about 0.3% oxygen. In another form, each of the annealing steps is

carried out in an environment having substantially 0% oxygen (oxygen concentration of 10ppm or less). A low oxygen environment is desirable during laser annealing as the concentration of oxygen in the annealing environment is directly proportional to the grain protrusion (i.e. a defect in the form of surface roughening) that is present on the semiconductor layer post-annealing. This leads to a deterioration in electrical and physical characteristics. In other words, a lower concentration of oxygen yields lower grain protrusion, which in turn yields desirable (or improved) electrical and physical characteristics. However, laser annealing in a low oxygen environment typically increases the occurrence of other defects, such as ablation (i.e. loss of material from the surface of the semiconductor layer). By using a nitrogen doped layer having a concentration of at least 3×10^{20} atoms/cc on the semiconductor layer to be annealed, the applicant has found that laser annealing can be carried out in a low oxygen environment while ensuring defects remain at an acceptable level. This will be described in further detail later in this specification.

Referring back to Figure 3B, and as highlighted earlier, the laser annealing (by laser irradiation) of the first and second areas of the nitrogen doped layer 306 is carried out such that a part of the first area and a part of the second area overlap in the product region 302. The benefits of having the overlap arranged in this manner will be apparent later in this specification. Once the laser annealing steps have been carried out, the resulting arrangement is as shown in Figure 3C, where the a-Si in the semiconductor layer 300 and the nitrogen doped layer 306 together form a polycrystalline silicon (p-Si) layer 312. Given the use of the nitrogen doped layer, the layer 312 will include a surface having a nitrogen concentration of at least 3×10^{20} atoms/cc. Once the layer 312 is formed, it can be sent for further processing (e.g. masking, etching etc). It will be apparent to skilled persons that the p-Si layer 312 formed in accordance with this implementation has a thickness equal to the thickness of the semiconductor layer 300 and the nitrogen doped layer 306 combined. As a non-limiting example, if a 50nm-thick p-Si layer is desired, the method may be carried out by forming and annealing a 10nm-thick a-Si nitrogen doped layer 306 on a 40nm-thick a-Si semiconductor layer 300.

Another implementation of the method of Figure 2 will now be described with reference to Figures 4A-4C. As with Figure 3A, Figure 4A shows a cross-section segment of an example semiconductor layer 400, which has a product region 402 and which is shown disposed on a substrate 404. In this form, step 200 of Figure 2 is carried out by ion
5 implanting or plasma-doping nitrogen into the upper portion 406 of the semiconductor layer 400. This results in the upper portion 406 of the semiconductor layer 400 being converted into a nitrogen doped layer 406. In other words, in this implementation, the nitrogen doped layer 406 forms part of the semiconductor layer 400 but it can be distinguished from the semiconductor layer 400 by virtue of the nitrogen concentration
10 in the nitrogen doped layer 406. The nitrogen concentration and depth of the nitrogen doped layer 406 may be controlled by controlling the energy used in the ion implantation or plasma-doping process. As before, the nitrogen concentration is at least 3×10^{20} atoms/cc. Steps 202 and 204 of Figure 2 are then carried out on the nitrogen doped layer 406 (i.e. a first area of the nitrogen doped layer 406 is subjected to laser
15 annealing 408, and a second area of the nitrogen doped layer 406 is subjected to laser annealing 410). As before, the first and second areas overlap in the product region 402, and the laser annealing process results in a crystallised layer 412. Where a-Si is used to form the semiconductor layer 400, the result of annealing is a p-Si layer 412. It will be apparent to skilled persons that the p-Si layer 412 in this embodiment will have a
20 thickness equal to the thickness of the semiconductor layer 400. As a non-limiting example, if a 50nm-thick p-Si layer is desired, the method in this embodiment may be carried out using a 50nm-thick semiconductor layer 400.

In another implementation of the method of Figure 2, step 200 further comprises
25 forming a nitrogen doped layer that includes oxygen, the oxygen concentration being in the range of 3×10^{21} atoms/cc to 7×10^{22} atoms/cc. More particularly, but not exclusively, the oxygen concentration is in the range of 5×10^{21} atoms/cc to 5×10^{22} atoms/cc. The oxygen concentration may be provided by forming the nitrogen doped layer using nitrous oxide (N_2O) gas in a CVD process, or otherwise in the presence of oxygen (e.g.
30 oxidation by air). Alternatively, the oxygen concentration may be provided by ion implanting or plasma-doping oxygen into the nitrogen doped layer. It should be noted that it is not essential that the oxygen concentration be provided after the layer has been

doped with nitrogen. Where necessary or desired, the oxygen concentration may be provided before or at the same time as doping the layer with nitrogen.

As outlined earlier, the use of the nitrogen doped layer in the present method allows a
5 reduction in certain defects that are typically observed at the overlap region after the
laser annealing process. In particular, the overlap region of a conventional laser
annealing method typically exhibits excessive grain protrusion (i.e. surface roughness),
which adversely affects the electrical and physical characteristics of that region of the
annealed semiconductor layer. Specifically, where excessive grain protrusion is
10 generated, it becomes difficult to cover the annealed semiconductor layer with a thin
insulating layer to form a semiconductor device. This, in turn, may result in an electrical
short between the annealed semiconductor layer and a conductive layer (e.g. a gate
electrode) via the insulating layer, which is disposed between the annealed
semiconductor layer and the conductive layer. This arrangement of layers of a
15 semiconductor device will be described in further detail later with reference to Figure 7.
Given the above drawbacks, conventional laser annealing is restricted in that the overlap
region must be provided outside of product regions. Referring to Figure 5A, for
example, given a 3x3 array 500 of product regions 502 and given the restriction of
having all overlap regions 506 to be outside of the product regions 502, the length of the
20 laser beam 504 is restricted to x_1 and the beam 504 will have to be scanned three times
over three areas 508, 510 and 512 to cover the entire array. Where a nitrogen doped
layer is used in accordance with the techniques described above, as shown in Figure 5B,
the annealing may be carried out in a low oxygen atmosphere, thus allowing the grain
protrusion of the overlap region to be reduced to an acceptable level. This, in turn,
25 makes it feasible for the overlap region to fall within one or more product regions and
for the annealing process to be completed by setting the laser beam to a length x_2 greater
than x_1 and by scanning the beam in fewer scans (two scans in the example of Figure 5B
- first area 514 and second area 516, as opposed to three scans over areas 508, 510 and
512 in the example of Figure 5A). In this implementation, the method allows annealing
30 to be carried out in less time (thus reducing the typical bottleneck that is created by the
laser annealing process) and using fewer laser shots. Production times are therefore

reduced, leading to an improvement in production efficiency and a reduction in production costs.

An example of the reduction in defects in the form of grain protrusions in the overlap region will now be described with reference to Figures 6A-6D. Figure 6A shows a diagrammatic side view of the excimer laser beam 600 with the energy density of 30mJ/cm² scanned over a first area (consisting of regions 1-2) of the semiconductor layer 604, and laser beam 602 scanned over a second area (consisting of regions 2-3) of the semiconductor layer 604. In the embodiment illustrated, the semiconductor layer 604 is a 50nm-thick a-Si layer that has been deposited on a glass substrate by introducing silane gas (together with argon (Ar) gas as a carrier) in a CVD chamber containing the glass substrate. Figure 6B shows the results from conventionally laser-annealing the semiconductor layer 604, with the x-axis representing the regions shown in Figure 6A and the y-axis representing grain protrusion height in nanometers. The y-axis includes an upper limit marker (e.g. 20nm), which represents the maximum grain protrusion height that can be adequately covered by the thin insulating layer (708 in Figure 7) that will be subsequently formed on the p-Si layer (702 in Figure 7). As outlined earlier, the presence of grain protrusions that exceed the upper limit typically results in the overlap region exhibiting undesirable electrical and physical characteristics. From Figure 6B, it is clear that the overlap region (region 2) in a conventional annealing process exhibits grain protrusion over the upper limit. Referring now to Figure 6C, the semiconductor layer 604 is shown having a nitrogen doped layer 608, in accordance with the present method. In the embodiment illustrated, the semiconductor layer 604 and nitrogen doped layer 608 are sequentially deposited as follows:

1. A glass substrate is supported on a susceptor in a CVD chamber.
2. The air in the CVD chamber is exhausted, and silane gas (together with Ar gas as carrier) is introduced in the CVD chamber containing the glass substrate.
3. A 40nm-thick a-Si layer is deposited on the glass substrate to form the semiconductor layer.

4. N₂O gas is introduced in the CVD chamber together with silane gas to form a 10nm-thick doped a-Si layer having nitrogen atoms and oxygen atoms at a concentration of 2×10^{21} atoms/cc and 2×10^{22} atoms/cc respectively.
- 5 As can be seen from Figure 6D, the result of using the nitrogen doped layer 608 is that the grain protrusion across the overlap region (region 2) is reduced to below the upper limit. For instance, the grain protrusion height in the overlap region has a root mean square (rms) value of 15nm, which is lower than the 20nm upper limit. The rms value of the grain protrusion height of the annealed semiconductor layer as a whole is therefore
- 10 less than the upper limit of 20nm. Furthermore, the grain size of the overlap region is larger than $0.2 \mu\text{m}$ (e.g. around $0.35 \mu\text{m}$), and is substantially uniform. With such acceptable grain size and protrusions, the overlap region no longer exhibits undesirable electrical and physical properties, thus allowing the overlap region to be formed in one or more product regions without adversely affecting the electrical and physical
- 15 characteristics of the product regions. It should be noted that the use of the nitrogen doped layer 608 results in the p-Si layer (i.e. after laser annealing) having a surface with a nitrogen concentration of 1×10^{21} atoms/cc, and an oxygen concentration of 1×10^{22} atoms/cc.
- 20 An example semiconductor device formed from the semiconductor layer annealed using the present method will now be described with reference to Figure 7. As described earlier, annealing the semiconductor layer results in a crystalline form (i.e. layers 312 and 412 in Figures 3C and 4C respectively) of the semiconductor layer. The product region(s) of the annealed semiconductor layer are then processed to form semiconductor
- 25 devices or components of such devices. Figure 7 shows the array substrate 700 for LCDs including a staggered type TFT 701 as the semiconductor device. The crystalline form of the semiconductor layer forms the TFT active layer 702 including a source region, a drain region, and a channel region sandwiched between source and drain regions on the glass substrate with an undercoat layer for preventing the influence of
- 30 impurities from the glass substrate. The TFT active layer 702 also includes a first surface and a second surface. When the active layer 702 is disposed on the substrate, the

second surface is adjacent the substrate. The first surface of the TFT active layer 702 forms the surface on which a gate insulating layer is arranged, as will be described below.

5 The TFT active layer 702 (and more specifically the first surface of the layer 702) may have a nitrogen concentration of 1×10^{21} atoms/cc. In more general terms, the first surface of the TFT active layer 702 may have a nitrogen concentration in the range of 3×10^{20} atoms/cc to 1×10^{22} atoms/cc, more specifically 5×10^{20} atoms/cc to 5×10^{21} atoms/cc. As described earlier, the nitrogen concentration is the result of initial doping
10 of the nitrogen doped layer. The TFT active layer 702 (and more specifically the first surface of the layer 702) may also have an oxygen concentration of 1×10^{22} atoms/cc. In more general terms, the first surface of the TFT active layer 702 may have an oxygen concentration in the range of 3×10^{21} atoms/cc to 7×10^{22} atoms/cc, more specifically 5×10^{21} atoms/cc to 5×10^{22} atoms/cc. In one form, the first surface of the TFT active
15 layer 702 has a nitrogen concentration of at least 3×10^{20} atoms/cc.

The TFT 701 also includes source and drain electrodes 704 and 706, which are electrically connected to the source and drain regions of the active layer 702 respectively, and an insulating layer 708, which is interposed between a gate electrode
20 710 and the first surface of the active layer 702. In one form, the TFT 701 controls a pixel electrode 711 disposed on the TFT 701 through insulating layers in an LCD, and is one of a plurality of TFTs formed in each product region, where each product region makes up an LCD display region or panel. In another form, the TFT controls pixels in an OLED display device, and is one of a plurality of TFTs formed in each product
25 region, where each product region makes up an OLED display region or panel.

The foregoing describes exemplary embodiments, which, as will be understood by those skilled in the art, may be subjected to variations or modifications in design, construction or operation without departing from the spirit and scope of the claims. For example,
30 while the method has been described with reference to steps to be carried out in a certain order, the method may be modified such that the steps are carried out in a different order, where appropriate. Also, the method may be modified such that

additional steps are carried out. Skilled persons will appreciate that the feature of having the overlap region within one or more product regions does not restrict the overlap region to be only formed within product regions, and that it is sufficient for at least part of the overlap region to be formed with a product region. Also, while the nitrogen doped layer has been described as advantageous for reducing grain protrusion, it is not limited for such use. For example, the nitrogen doped layer may also be used to reduce ablation and other like defects. The above variations, for instance, are intended to be covered by the spirit and scope of the claims.

CLAIMS

1. A method of laser annealing a non-single crystalline semiconductor layer, the non-single crystalline semiconductor layer including a product region, the method comprising:
 - forming a nitrogen doped layer on the non-single crystalline semiconductor layer, the nitrogen doped layer having a nitrogen concentration of at least 3×10^{20} atoms/cc,
 - irradiating a first area of the nitrogen doped layer in a low oxygen environment with a laser beam, and
 - irradiating a second area of the nitrogen doped layer in a low oxygen environment with a laser beam, a part of the second area overlapping with a part of the first area in the product region.
2. The method of claim 1 wherein the nitrogen doped layer is formed by doping nitrogen into the non-single crystalline semiconductor layer.
3. The method of claim 1 wherein the non-single crystalline semiconductor layer and the nitrogen doped layer are sequentially deposited by using a chemical vapour deposition (CVD) process.
4. The method of claim 3 wherein the CVD process is carried out by introducing SiH_4 gas at a first flow rate and N_2O gas at a second flow rate into a CVD chamber.
5. The method of claim 4 further comprising controlling a concentration of nitrogen in the nitrogen doped layer by controlling one or both of the first flow rate and the second flow rate.
6. The method of claim 2 wherein the step of doping nitrogen into the non-single crystalline semiconductor layer is carried out using an ion implantation or plasma-doping process.

7. The method of any one of the preceding claims wherein the nitrogen doped layer has a thickness in the range of 1nm to 30nm.
- 5 8. The method of claim 7 wherein the nitrogen doped layer has a thickness in the range of 5nm to 15nm.
9. The method of any one of the preceding claims wherein the nitrogen doped layer has a nitrogen concentration in the range of 3×10^{20} atoms/cc to 1×10^{22} atoms/cc.
- 10 10. The method of claim 9 wherein the nitrogen concentration is in the range of 5×10^{20} atoms/cc to 5×10^{21} atoms/cc.
11. The method of any one of the preceding claims wherein the nitrogen doped layer is also doped with oxygen and has an oxygen concentration in the range of 3×10^{21} atoms/cc to 7×10^{22} atoms/cc.
- 15 12. The method of claim 11 wherein the oxygen concentration is in the range of 5×10^{21} atoms/cc to 5×10^{22} atoms/cc.
- 20 13. The method of any one of the preceding claims wherein the non-single crystalline semiconductor layer includes a plurality of product regions, each comprising a display region of a display device.
- 25 14. A semiconductor device comprising a laser-annealed semiconductor layer, the laser-annealed semiconductor layer having a nitrogen concentration of at least 3×10^{20} atoms/cc at a surface thereof.
- 30 15. The semiconductor device of claim 14 wherein the semiconductor layer is a polycrystalline silicon layer.

16. The semiconductor device of claim 14 or 15 wherein the nitrogen concentration is in the range of 3×10^{20} atoms/cc to 1×10^{22} atoms/cc.
- 5 17. The semiconductor device of claim 16 wherein the nitrogen concentration is in the range of 5×10^{20} atoms/cc to 5×10^{21} atoms/cc.
18. The semiconductor device of any one of claims 14-17 wherein the semiconductor layer has an oxygen concentration in the range of 3×10^{21} atoms/cc to 7×10^{22} atoms/cc at the surface thereof.
- 10 19. The semiconductor device of claim 18 wherein the oxygen concentration is in the range of 5×10^{21} atoms/cc to 5×10^{22} atoms/cc.
- 15 20. The semiconductor device of any one of claims 14-19 wherein the semiconductor device is one of a plurality of semiconductor devices formed in a display region of a display device.
- 20 21. A semiconductor device comprising a gate electrode, a source electrode, a drain electrode, an insulating layer, and a semiconductor layer, the insulating layer being interposed between the gate electrode and the semiconductor layer, and the source and drain electrodes being electrically connected to the semiconductor layer, the semiconductor layer including a surface having a nitrogen concentration of at least 3×10^{20} atoms/cc.
- 25 22. A semiconductor device comprising a laser-annealed semiconductor layer, the laser-annealed semiconductor layer having a nitrogen concentration of at least 3×10^{20} atoms/cc at a surface thereof, and a root mean square (rms) value of grain protrusion height of less than 20nm.
- 30

23. A semiconductor device comprising:

a laser-annealed semiconductor layer having a first surface and second surface, and being disposed on a substrate such that the second surface is adjacent the substrate;

5 a gate electrode disposed over the laser-annealed semiconductor layer and adjacent the first surface, with a gate insulating layer separating the gate electrode and the first surface; and

source and drain electrodes connected to the laser-annealed semiconductor layer;

10 wherein a nitrogen concentration at the first surface of the laser-annealed semiconductor layer is at least 3×10^{20} atoms/cc.

24. The semiconductor device of claim 23, wherein the laser-annealed semiconductor layer is the result of a semiconductor layer being irradiated with
15 a laser beam using at least a first beam scan and a second beam scan.

25. The semiconductor device of claim 23 or 24, wherein the laser-annealed semiconductor layer has a grain size not less than $0.2 \mu\text{m}$.

20 26. The semiconductor device of claim 25, wherein the grain size of the laser-annealed semiconductor layer is not less than $0.3 \mu\text{m}$.