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# SEMICONDUCTOR SUBSTRATE AND PRODUCING METHOD THEREOF

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a semiconductor substrate and a producing method thereof. More specifically, the present invention relates to dielectric isolation or a producing method of a single-crystal semiconductor on an insulator and a single-crystal compound semiconductor on an Si substrate, and further relates to a producing method of a semiconductor substrate suitable for an electronic device or an integrated circuit formed at a single-crystal semiconductor layer.

### Related Background Art

Formation of a single-crystal Si semiconductor layer on an insulator is widely known as a silicon on insulator (SOI) technique and has been researched to a large extent since a device utilizing the SOI technique has a number of advantageous points which can not be achieved by a bulk Si substrate forming the normal Si integrated circuit. Specifically, for example, the following advantageous points can be achieved by employing the SOI technique:

1. Dielectric isolation is easy and high integration is possible;

2. Radiation resistance is excellent;

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3. Floating capacitance is reduced and high speed is possible;

4. Well process can be omitted;

5. Latch-up can be prevented;

6. Fully depleted (FD) field effect transistor is achieved through film thickness reduction.

These are described in detail, for example, in the literature of Special Issue: "Single-crystal silicon on non-single-crystal insulators"; edited by G.W. Cullen, Journal of Crystal Growth, volume 63, no 3, pp 429-590 (1983).

Further, over the past few years, the SOI has been largely reported as a substrate which realizes the acceleration of a MOSFET and the low power consumption (IEEE SOI conference 1994). Since an element has an insulating layer at its lower part when employing the SOI structure, an element separation process can be simplified as compared with forming an element on a bulk silicon wafer so that a device process can be shortened. Specifically, in addition to achieving the higher performance, reduction of the wafer cost and the process cost is expected in total as compared with a MOSFET or IC on bulk silicon.

Particularly, the fully depleted (FD) MOSFET is expected to achieve the higher speed and the lower power consumption through improvement in driving force. In general, a threshold voltage (Vth) of a MOSFET is

determined by the impurity concentration at a channel portion. On the other hand, in case of the FD MOSFET using the SOI, a depletion layer is also subjected to an influence of a film thickness of the SOI. Thus, for producing the large scale integrated circuits at the high yield, uniformity of the SOI thicknesses has been strongly demanded.

On the other hand, a device on a compound semiconductor has the high performance, such as, high speed and luminescence, which can not be achieved by Si. Presently, such a device is normally formed in an epitaxial layer grown on a compound semiconductor substrate, such as a GaAs substrate.

However, there is a problem that the compound semiconductor substrate is expensive while low in mechanical strength so that the large area wafer is difficult to be produced.

Under these circumstances, an attempt has been made to achieve the heteroepitaxial growth of a compound semiconductor on an Si wafer which is inexpensive and high in mechanical strength so that the large area wafer can be produced.

Referring back to the SOI, the researches on formation of the SOI substrates have been active since the 1970s. In the beginning, the researches were well performed in connection with the SOS (sapphire on silicon) method which achieves the heteroepitaxial

growth of single-crystal silicon on a sapphire substrate being an insulator, the FIPOS (fully isolation by porous oxidized silicon) method which forms the SOI structure by dielectric isolation based on oxidation of porous Si, and the oxygen ion implantation method.

In the FIPOS method, an n-type Si layer is formed on a surface of a p-type Si single-crystal substrate in the island shape through the proton ion implantation (Imai and collaborator, J. Crystal Growth, vol 63, 547 (1983)) or through the epitaxial growth and the patterning, then only the p-type Si substrate is rendered porous so as to surround the Si island from the surface by means of the anodizing method in a HF solution, and thereafter the n-type Si island is dielectric-isolated through accelerating oxidation. In this method, there is a problem that the isolated Si region is determined in advance of the device process so that the degree of freedom of device designing is limited.

The oxygen ion implantation method is a method called SIMOX first reported by K. Izumi. After implanting about $10^{17}$ to $10^{18}/cm^2$ of oxygen ions into an Si wafer, the ion-implanted Si wafer is annealed at the high temperature of about 1,320°C in the atmosphere of argon/oxygen. As a result, oxygen ions implanted with respect to a depth corresponding to a projection range

(Rp) of ion implantation are bonded with silicon so as to form a silicon oxide layer. On this occasion, a silicon layer which has been rendered amorphous at an upper portion of the silicon oxide layer due to the oxygen ion implantation is also recrystallized so as to be a single-crystal silicon layer. Conventionally, there have been a lot of defects included in the silicon layer on the surface, that is, about $10^5/cm^2$. On the other hand, by setting an implantation amount of oxygen to about $4x10^{17}/cm^2$, defects are successfully reduced to about $10^2/cm^2$. However, since the ranges of implantation energy and implantation amount for maintaining the quality of the silicon oxide layer, the crystalline property of the surface silicon layer and the like are so narrow that thicknesses of the surface silicon layer and the buried silicon oxide (BOX: buried oxide) layer were limited to particular values. For achieving a desired thickness of the surface silicon layer, it was necessary to perform sacrificial oxidation and epitaxial growth. In this case, there is a problem that, since the degradation caused through these processes is superposed on the distribution of thicknesses, the thickness uniformity is deteriorated.

It has been reported that a formation failure region of silicon oxide called a pipe exists in the BOX layer. As one cause of this, the foreign matter upon implantation, such as dust, is considered. In the

portion where the pipe exists, the deterioration of the device characteristic is generated due to leak between an active layer and a support substrate.

Further, since the ion implantation in the SIMOX is large in implantation amount as compared with the ion implantation in the ordinary semiconductor process, implantation time is long even after the apparatus to be used exclusively for that matter has been developed. The ion implantation is performed by raster-scanning an ion beam of a given current amount or expanding the beam so that increment of the implantation time is predicted following increment in area of the wafer. Further, in the high temperature heat treatment of the large-area wafer, it has been pointed out that a problem of occurrence of slip due to the temperature distribution in the wafer becomes severer. In the SIMOX, the heat treatment is essential at the high temperature, that is, 1,320°C, which is not normally used in the silicon semiconductor process, so that there has been concern that this problem including the development of the apparatus becomes more significant.

On the other hand, apart from the foregoing conventional SOI forming method, attention has been recently given to the method which forms the SOI structure by sticking an Si single-crystal substrate to a thermal-oxidized Si single-crystal substrate through the heat treatment or using adhesives. In this method,

it is necessary to form an active layer for the device into a uniform film. Specifically, it is necessary to form an Si single-crystal substrate of a thickness of as much as hundreds of microns into a film of several microns or less. There are three kinds of methods for thickness reduction as follows:

1. Thickness reduction through polishing;
2. Thickness reduction through local plasma etching;
3. Thickness reduction through selective etching.

In the polishing of 1, the uniform thickness reduction is difficult. Particularly, in case of thickness reduction to submicrons, the irregularity amounts to as much as tens of percents so that uniformalization is a big problem. If the size of wafer is further enlarged, the difficulty is increased correspondingly.

In the method of 2, after reducing the thickness to about 1 to 3μm through the polishing of 1, the thickness distribution is measured at many points. Thereafter, by scanning the plasma using the SF6 of a diameter of several millimeters based on the thickness distribution, etching is performed while correcting the thickness distribution, so as to reduce the thickness to a given value. In this method, it has been reported that the thickness distribution can be within the range of about ±10nm. However, if the foreign matter (particles) exists on the substrate upon plasma

etching, the foreign matter works as an etching mask so that projections are formed on the substrate.

Since the surface is rough immediately after the etching, touch polishing is necessary after completion of the plasma etching. The polishing amount is controlled based on the time management, and hence, the final film thickness control and the deterioration of film thickness distribution due to polishing have been pointed out. Further, in the polishing, abrasives such as colloidal silica directly rub the surface working as an active layer so that there has been concern about formation of a fracture layer due to polishing and introduction of processing distortion. Further, if the wafer is increased in area to a large extent, since the plasma etching time is increased in proportion to increment of the wafer area, there is concern about extreme reduction of the throughput.

In the method of 3, a film structure capable of selective etching is formed in advance in a substrate to be formed into a film. For example, a $p^+$-Si thin layer containing boron in the concentration no less than $10^{19}/cm^3$ and a $p^-$-Si thin layer are formed on a $p^-$ substrate using the method of, for example, the epitaxial growth so as to form a first substrate. The first substrate is bonded with a second substrate via an insulating layer such as an oxide film, and then the underside of the first substrate is ground or polished

in advance so as to reduce in thickness. Thereafter, the $p^+$ layer is exposed through the selective etching of the $p^-$ layer and further the $p^-$ layer is exposed through the selective etching of the $p^+$ layer, so as to achieve the SOI structure. This method is detailed in the report of Maszara.

Although the selective etching is said to be effective for uniform thickness reduction, it has the following problems:

The ratio of etching selectively is $10^2$ at most, which is not sufficient.

Since the surface property after etching is bad, the touch polishing is required after etching. However, as the result thereof, the film thickness is reduced and the thickness uniformity tends to be deteriorated. Particularly, although the polish amount is managed based on time, since dispersion of the polish speed is large, the control of the polish amount is difficult. Thus, it becomes a problem particularly in forming an extremely thin SOI layer of, for example, 100nm.

The crystalline property is bad because of using the ion implantation, the epitaxial growth or the heteroepitaxial growth on the high-concentration B dope Si layer.

The surface property of a surface to be bonded with is inferior to the normal silicon wafer (C.

Harendt, et. al., J. Elect. Mater. Vol. 20, 267 (1991), H. Baumgart, et. al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991), C.E. Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991)). Further, the selectivity of selective etching largely depends a difference in concentration of impurities such as boron and sharpness of the profile in the depth direction. Accordingly, if the high-temperature bonding annealing for increasing the bonding strength or the high-temperature epitaxial growth for improving the crystalline property is performed, the depth direction distribution of the impurity concentration expands so that the selectivity of etching is deteriorated. That is, it is difficult to improve both the ratio of etching selectively and the crystalline property or the bonding strength.

Recently, in view of the foregoing problems, Yonehara and collaborators have reported the bonded SOI which is excellent in thickness uniformity and crystalline property and capable of batch processing. Brief explanation about this will be given using Figs. 6A to 6E. In this method, a porous layer 62 formed on an Si substrate 61 is used as a material for selective etching (Fig. 6A). After epitaxial-growing a non-porous single-crystal Si layer 63 on the porous layer 62 (Fig. 6B), the three-layer composite is bonded with

a support substrate 64 via the oxidized Si layer 63 (Fig. 6C). The Si substrate 61 is reduced in thickness through grinding or the like from the underside so as to expose the porous Si 62 all over the substrate (Fig. 6D). The exposed porous Si 62 is removed through etching using a selective etching liquid, such as, KOH or $HF+H_2O_2$ (Fig. 6E). At this time, since the ratio of etching selectively porous Si relative to bulk Si (non-porous single-crystal silicon) can be set fully high, that is, 100,000 times, the non-porous single-crystal silicon layer grown on the porous layer in advance can be left on the support substrate without being hardly reduced in thickness, so as to form the SOI substrate. Accordingly, the thickness uniformity of the SOI is substantially determined during the epitaxial growth. Since a CVD apparatus used in the normal semiconductor process can be used for the epitaxial growth, according to the report of Sato and collaborator, the thickness uniformity is realized, for example, within 100nm ± 2%. Further, the crystalline property of the epitaxial silicon layer is also excellent and has been reported to be $3.5x10^2/cm^2$.

In the conventional method, since the selectivity of etching depends on the difference in impurity concentration and the depth direction profile, the temperature of the heat treatment (bonding, epitaxial growth, oxidation or the like) which expands the

concentration distribution is largely limited to approximately no higher than 800°C. On the other hand, in the etching of this method, since the difference in structure between porous and bulk determines the etching speed, the limitation of the heat treatment temperature is small. It has been reported that the heat treatment at about 1,180°C is possible. For example, it is known that the heat treatment after bonding enhances the bonding strength between the wafers and reduces the number and size of voids generated at the bonded interface. Further, in the etching based on such a structural difference, the particles, even if adhered on porous silicon, do not affect the thickness uniformity.

On the other hand, in general, on a light transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorderliness in crystal structure of the substrate, so that the high-performance device can not be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer can not be achieved even by merely depositing the Si layer.

However, the semiconductor substrate obtained through bonding normally requires two wafers one of which is removed wastefully for the most part through polishing, etching or the like, so that the finite

resources of the earth are wasted.

Accordingly, in the conventional method, the bonded SOI has various problems about controllability, uniformity and economics.

A method is proposed in Japanese Patent Application No. 7-045441 for recycling the first substrate which is wasted in such a bonding method.

In this method, the following method is adopted, in the foregoing bonding and etch-back method using the porous Si, instead of the step for reducing in thickness the first substrate through grinding, etching or the like from the underside so as to expose the porous Si. This will be explained using Figs. 7A to 7E.

After forming porous a surface layer 72 of an Si substrate 71 (Fig. 7A), a single-crystal Si layer 73 is formed thereon (Fig. 7B). Then, the single-crystal Si layer 73 along with the Si substrate 71 is bonded to a main surface of another Si substrate 74, working as a support substrate, via an insulating layer therebetween (Fig. 7C). Thereafter, the bonded wafers are separated at the porous layer 72 and the porous Si layer 72 exposed on the surface at the side of the Si substrate 74 is selectively removed so that the SOI substrate is formed. Separation of the bonded wafers is performed, for example, a method selected from the following methods that the tensile force or pressure is

sufficiently applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane; that the wave energy such as the ultrasonic wave is applied; that the porous layer is exposed at the wafer end surfaces, the porous Si is etched to some extent, and what is like a razor blade is inserted thereinto; that the porous layer is exposed at the wafer end surfaces and a liquid such as water is impregnated into the porous Si, and the whole bonded wafers are heated or cooled so as to expand the liquid. Alternatively, separation is performed by applying the force to the Si substrate 71 in parallel to the support substrate 74.

Each of these methods is based on the fact that, although the mechanical strength of the porous Si layer 72 differs depending on the porosity, it is considered to be much weaker than the bulk Si. For example, if the porosity is 50%, the mechanical strength can be considered to be half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is first ruptured. As the porosity is increased, the porous layer can be ruptured with a weaker force.

However, if the porosity of porous silicon is increased, it is possible that distortion is introduced due to the ratio of bulk silicon relative to the lattice constant being increased so as to increase

warpage of the wafer. As a result, the following problems may be raised, that is, the number of void bonding failure regions called void is increased upon bonding, the crystal defect density is increased and, in the worst case, cracks are introduced into the epitaxial layer, and slip lines are introduced on the periphery of the wafer due to influence of thermal distortion upon the epitaxial growth.

When applying the force in the vertical or horizontal direction relative to the surface of the wafer, since the semiconductor substrate is not a fully rigid body but an elastic body, the wafer may be subjected to elastic deformation depending on a supporting fashion of the wafer so that the force escapes and thus is not applied to the porous layer effectively. Similarly, when inserting what is like a razor blade from the wafer end surface, unless the razor blade is fully thin and fully high in rigidity, the yield may be lowered.

Further, if the bonding strength at the bonded interface is weaker as compared with the strength of the porous Si layer or if weak portions exist locally, the two wafers may be separated at the bonded interface so that the initial object can not be achieved.

Further, since, in any of the methods, the position where separation occurs in the porous layer is not fixed, if the ratio in etching speed between the

porous Si and the bulk Si is not sufficient, the epitaxial silicon layer is first etched more or less at a portion where the porous layer remains thin rather than at a portion where the porous layer remains thick. Thus, the thickness uniformity of the SOI layer may be deteriorated. Particularly, when the final thickness of the SOI layer is reduced to about 100nm, the thickness uniformity is deteriorated so that a problem may be raised when forming the element such as the fully depleted MOSFET whose threshold voltage is sensitive to the film thickness.

Japanese Patent Application No. 5-211128 (corresponding to United States Patent No. 5,374,564) discloses a method for producing the SOI. In this method, hydrogen ions are directly implanted into a single-crystal Si substrate, and then the single-crystal Si substrate and a support substrate are bonded together. Finally, the single-crystal Si substrate is separated at a layer where hydrogen ions are implanted, so as to form the SOI. In this method, since hydrogen ions are directly implanted into the single-crystal Si substrate which is then separated at the ion-implanted layer, the flatness property of the SOI layer is not good. Further, the thickness of the SOI layer is determined by the projection range, so that the degree of freedom of the thickness is low. Further, it is necessary to select an implanting condition satisfying

both of the layer thickness and the separation, which creates a difficulty in the control. Further, in case of aiming at obtaining a thin layer the thickness of which can not be determined by the ion implantation, it is necessary to carry out a reducing process in thickness such as grinding and etching, which process is nonselective, so that there is a fear of deteriorating the thickness uniformity.

In view of the foregoing, the method has been demanded for producing, with high reproducibility, the SOI substrate which is high in quality and whose SOI layer has the excellent flatness property, and simultaneously for achieving resources saving and reduction in cost through recycling of the wafer.

On the other hand, in general, on a light transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorderliness in crystal structure of the substrate, so that the high-performance device can not be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer can not be achieved even by merely depositing the Si layer.

The light transmittable substrate is important for constituting a contact sensor as being a light-receiving element or a projection-type liquid-crystal image display device. For achieving further

densification, further high resolution and further fineness of picture elements of the sensor or the display device, the high-performance drive element is required. As a result, it is necessary to produce the element on the light transmittable substrate using the single-crystal layer having the excellent crystalline property.

Further, when using the single-crystal layer, reduction in size and acceleration of a chip can be achieved by incorporating a peripheral circuit for driving the picture elements and an image processing circuit into the same substrate having the picture elements.

Specifically, in case of amorphous Si or polycrystalline Si, it is difficult, due to its defective crystal structure, to produce the drive element having the performance which is required or will be required in the future.

On the other hand, for producing the device of the compound semiconductor, the substrate of the compound semiconductor is essential. However, the compound semiconductor substrate is expensive and further is very difficult to be increased in area to a large extent.

Further, an attempt has been made to achieve the epitaxial growth of the compound semiconductor such as GaAs on the Si substrate. However, due to difference

in lattice constant or thermal expansion coefficient, the grown film is poor in crystalline property and thus is very difficult to be applied to the device.

Further, an attempt has been made to achieve the epitaxial growth of the compound semiconductor on porous Si for reducing misfit of lattice. However, due to low thermostability and aged deterioration of porous Si, the stability and the reliability are poor as the substrate during or after production of the device. However, there is a problem that the compound semiconductor substrate is expensive and low in mechanical strength so that the large-area wafer is difficult to be produced.

In view of the foregoing, an attempt has been made to achieve the heteroepitaxial growth of the compound semiconductor on the Si wafer which is inexpensive and high in mechanical strength so that the large-area wafer can be produced.

Further, recently, attention has been given to porous silicon also as a luminescent material for photoluminescence, electroluminescence or the like, and many research reports have been made therefor. In general, the structure of porous silicon largely differs depending on the type (p, n) and the concentration of impurities contained in silicon. When the p-type impurities are doped, the structure of porous silicon is roughly divided into two kinds

depending on whether the impurity concentration is no less than $10^{18}/cm^3$ or no more than $10^{17}/cm^3$. In the former case, the pore walls are relatively thick, that is, from several nanometers to several tens of nanometers, the pore density is about $10^{11}/cm^2$ and the porosity is relatively low. However, it is difficult for this porous silicon to serve for luminescence. On the other hand, in the latter case, as compared with the former case, porous silicon whose pore wall is no more than several nanometers in thickness, whose pore density is greater by one figure and whose porosity exceeds 50%, can be easily formed. Most of luminous phenomena, such as photoluminescence, are mainly based on the formation of porous silicon using the latter as a starting material. However, the mechanical strength is low corresponding to the largeness of porosity. Further, since a lattice constant deviation relative to bulk Si is as much as $10^{-3}$ (about $10^{-4}$ in the former case), there has been a problem that, when epitaxial-growing the single-crystal silicon layer on such porous silicon, defects are largely introduced into the epitaxial Si layer and cracks are further introduced thereinto. On the other hand, for utilizing the fine porous structure, which is suitable for a luminescent material, as a luminescent element, it has been desired that the epitaxial Si layer be formed on porous silicon for providing a contact or the MOSFET or the like as a

peripheral circuit be formed on the epitaxial silicon layer.

SUMMARY OF THE INVENTION

The present invention has an object to provide a semiconductor substrate and a forming method thereof which can solve the foregoing various problems by superposing a finer porous structure in a porous layer.

As a result of assiduous efforts made by the present inventors, the following invention has been achieved.

Specifically, a semiconductor substrate of the present invention is characterized by having a porous Si layer at a surface layer of an Si substrate, and a porous Si layer with large porosity existing in a region of the above-mentioned porous Si layer, which region is at a specific depth from the surface of the above-mentioned porous Si layer. In the semiconductor substrate, a non-porous Si portion may exist on the surface of the porous Si layer and an electrode may be formed on respective surfaces of the Si substrate and the non-porous Si layer, so that the semiconductor substrate constitutes a luminescent element.

According to a semiconductor substrate of the present invention, for example, a structure can be easily achieved, wherein a porous layer having a fine structure to work as a luminescent material is

sandwiched in a porous layer having a high mechanical strength, such as porous silicon formed on a $p^+$-Si substrate. Although the porous layer having such a fine structure differs from bulk Si in lattice constant, by sandwiching it in the large porous Si layer having intermediate lattice constant, stresses can be relaxed and introduction of cracks or defects can be suppressed. Specifically, since the luminescent layer which is stable in structure can be formed, it is not only possible to serve for formation of peripheral circuit or wiring, but also possible to provide a material which is excellent in long-term stability.

Further, according to a semiconductor substrate of the present invention, an extremely thin porous layer corresponding to a projection range of ion implantation can be formed. Since the pore size of such a porous layer can be set small, that is, no greater than several tens of nanometers, even the small foreign matter contained in gas and exceeding several tens of nanometers in diameter can be removed. Further, a thickness of such a porous layer can be set small, that is, no greater than 20μm, the conductance of the gas can be ensured. Specifically, when using it as a filter for particles in the gas, it is possible to produce a filter which can remove the particles greater than several tens of nanometers in diameter and whose pressure loss is small. Further, if high purity Si

which is used in the semiconductor process is used as a substrate, there is no worry about contamination from the filter itself.

The present invention includes a producing method of a semiconductor substrate.

Specifically, a producing method of a semiconductor substrate of the present invention comprises a porous-forming step for forming an Si substrate porous and forming a porous Si layer on at least a surface of the Si substrate, and a high-porosity layer forming step for forming a porous Si layer with large porosity in the region at the specific depth from the porous layer in the porous Si layer. The high-porosity layer forming step can be carried out as an ion implanting step for implanting ions into the porous Si layer with a given projection range. It is preferable that the ions comprises at least one kind of noble gas, hydrogen and nitrogen. It is preferable that a non-porous layer forming step is provided for forming a non-porous layer on a surface of the porous Si layer before the ion implanting step. It is preferable that a bonding step is provided for bonding a support substrate on a surface of the non-porous layer after the high-porosity layer forming step and that a separating step is provided for separating the Si substrate into two at the porous Si layer with the large porosity after the bonding step. It is

preferable that the separating step is performed by heat-treating the Si substrate, by pressurizing the Si substrate in a direction perpendicular to a surface thereof, by drawing the Si substrate in a direction perpendicular to a surface thereof or by applying a shearing force to the Si substrate.

It is preferable that the non-porous layer is made of single-crystal Si, single-crystal Si having an oxidized Si layer on a surface to be bonded or a single-crystal compound semiconductor. It is preferable that the support substrate is an Si substrate, an Si substrate having an oxidized Si layer on a surface to be bonded or a light transmittable substrate. It is preferable that the bonding step is performed by anode bonding, pressurization, heat treatment or a combination thereof. It is preferable that a porous Si removing step is provided, after the separating step, for removing the porous Si layer exposed on a surface of the support substrate and exposing the non-porous layer. It is preferable that the porous Si removing step is performed by an electroless wet etching using at least one of hydrofluoric acid, a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to buffered hydrofluoric

acid. It is preferable that a flattening step is provided for flattening a surface of the non-porous layer after the porous Si removing step. It is preferable that the flattening step is performed by heat treatment in the atmosphere including hydrogen.

It may be arranged that the porous-forming step forms porous Si layers on both sides of the Si substrate, and that the bonding step bonds two support substrates to the porous Si layers formed on both sides of the Si substrate. It may be arrange that a second non-porous layer forming step is provided, after the separating step, for forming a non-porous layer again on the surface of the porous Si layer exposed on the surface of the Si substrate, and that a second ion implanting step is provided, after the porous layer forming step, for implanting ions into the porous Si layer with a given projection range and forming a porous Si layer with large porosity in the porous Si layer. It is preferable that the porous-forming step is performed by anodization. It is preferable that the anodization is performed in an HF solution.

The high-porosity layer forming step can be carried out by also altering the current density, during the porous-forming step.

After removing the remaining porous layer, the Si substrate separated by the foregoing method may be reused as an Si substrate by performing the surface

flattening process if the surface flatness property is insufficient. The surface flattening process may be polishing, etching or the like normally used in the semiconductor process. On the other hand, the heat treatment in the atmosphere including hydrogen may also be used. By selecting the condition, this heat treatment can achieve the flatness to an extent where the atomic step is locally presented.

According to the producing method of the semiconductor substrate of the present invention, upon removal of the Si substrate, the Si substrate can be separated at one time in large area via the porous layer. Thus, the process can be shortened. Further, since the separating position is limited to within the porous layer with large porosity due to the ion implantation, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with excellent selectivity.

According to the producing method of the semiconductor substrate of the present invention, the Si substrate can be separated in advance at one time in large area via the porous layer. Thus, the grinding, polishing or etching process which was essential in the prior art for removing the Si substrate to expose the porous silicon layer can be omitted to shorten the process. Further, since the separating position is

limited to within the porous layer with large porosity by implanting ions of at least one kind of noble gas, hydrogen and nitrogen into the porous layer so as to have the projection range, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with excellent selectivity. It is hard to happen that the thickness of the remaining porous layer is thin locally, so that the non-porous layer appears on the surface earlier and is etched accordingly. In the case, the forming method of the porous layer having a high porosity is not restricted to the ion implantation, but the formation can be realized by also altering the electric current at the anodization. Specifically, not only the grinding or etching process which was essential in the prior art for exposing porous silicon can be omitted, but also the removed Si substrate can be reused as an Si substrate by removing the remaining porous layer. If the surface flatness property after the removal of porous silicon is insufficient, the surface flattening process is performed. Since the position where the bonded two substrates are separated is regulated by the projection range, the dispersion of the separating positions within porous silicon does not occur as opposed to the prior art. Thus, upon removal of porous silicon, the single-crystal silicon layer is prevented from being

exposed and etched to deteriorate the thickness uniformity. Further, the Si substrate can be reused in the desired number of times until its structural strength makes it impossible. Further, since the separating position is restricted to around the depth corresponding to the projection range of the ion implantation, the thickness of the porous layer can be set smaller as compared with the prior art. Further, it is capable of making the layer having a high porosity a layer having a specific depth constant from the surface of the porous layer to separate it, so that such a quality as the crystalizability of the porous layer is not deteriorated.

Alternatively, without removing the remaining porous layer, the separated Si substrate can be reused again as an Si substrate of the present invention by forming a non-porous single-crystal Si layer. Also in this case, the Si substrate can be reused in the desired number of times until its structural strength makes it impossible.

In the conventional method of producing the bonded substrates, the Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the Si substrate is held in the initial state other than its

surface layers so that, by using both sides of the Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one Si substrate. Thus, the process can be shortened and the productivity can be improved. As appreciated, also in this case, the separated Si substrate can be recycled as an Si substrate after removing the remaining porous Si.

Specifically, the present invention uses a single-crystal Si substrate which is excellent in economics, flat and uniform over a large area and has an extremely excellent crystalline property, and removes from one side thereof to an Si or compound semiconductor active layer formed on the surface which thus remains, so as to provide a single-crystal Si layer or a compound semiconductor single-crystal layer with extremely less defects on an insulating material.

The present invention provides a producing method of a semiconductor substrate which is capable of achieving an Si or compound semiconductor single-crystal layer with a crystalline property as good as a single-crystal wafer on a transparent substrate (light transmittable substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

Further, the present invention provides a producing method of a semiconductor substrate which is

replaceable for an expensive SOS or SIMOX upon producing a large scale integrated circuit of an SOI structure.

According to the present invention, the single-crystal compound semiconductor layer with excellent crystalline property can be formed on porous Si, and further, this semiconductor layer can be transferred onto the large-area insulating substrate which is excellent in economics. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound semiconductor layer with excellent crystalline property on the insulating substrate.

Further, since porous Si has a low mechanical strength and an extensive surface area, removal of the porous Si layer of the present invention can also be performed by selective polishing using the single-crystal layer as a polishing stopper.

According to the producing method of the semiconductor substrate, since the porous layer of a fine structure can be formed after formation of the single-crystal silicon layer on the porous layer, the epitaxial growth condition of the single-crystal layer can be set free of influence of the structural change of the porous layer. Specifically, since the fine-structure porous layer, working as a luminescent layer,

which tends to change due to thermal treatment, can be formed after completion of thermal treatment for the film formation, the characteristic of the element can be stable.

According to the producing method of the semiconductor substrate, upon removal of the Si substrate, the Si substrate can be separated at one time in large area via the porous layer, the process can be shortened. Further, since the separating position is limited to within the porous layer by means of the ion implantation, thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with high selectivity. Thus, even when the etching is unstable due to the size of the apparatus or the change of the environment, the non-porous thin film, such as the single-crystal Si layer or the compound semiconductor single-crystal layer, which is excellent in economics, flat and uniform over the large area and has the extremely excellent crystalline property, can be transferred onto the support substrate with high yield. Specifically, the SOI structure with the single-crystal Si layer formed on the insulating layer can be obtained with high uniformity of film thickness and high yield. Further, since the separating position is regulated by the projection range of the ion implantation so as to be within the porous layer, the

thicknesses of the porous layer remaining on the support substrate side can be uniform so that the porous layer can be removed with high selectivity. Further, the removed Si substrate can be reused as an Si substrate by removing the remaining porous layer. If the surface flatness property after removal of porous silicon is insufficient, the surface flattening process is performed.

The present invention provides a producing method of a semiconductor substrate which is capable of achieving an Si or compound semiconductor single-crystal layer with a crystalline property as good as a single-crystal wafer on a transparent substrate (light transmittable substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

According to the producing method of the semiconductor substrate of the present invention, since the selective etching which is excellent in a ratio of etching selectively can be performed, by performing the bonding with the support substrate, the SOI substrate or the compound semiconductor single crystal on the support substrate, which is flat and uniform over the large area and has an extremely excellent crystalline property, can be achieved.

Further, according to the producing method of the semiconductor substrate, the single-crystal compound semiconductor layer with high crystalline property can

be formed on porous Si, and further, this semiconductor layer can be transferred onto the large-area insulating substrate which is excellent in economics. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound semiconductor layer with excellent crystalline property on the insulating substrate.

Further, even if non-formation regions of the implanted layer are formed due to presence of the foreign matter on the surface upon the ion implantation, since the mechanical strength of the porous layer itself is smaller than bulk Si, the separation occurs in the porous layer. Thus, the bonded two substrates can be separated without causing damages such as cracks in the non-porous single-crystal silicon layer.

Further, since the gettering effect is available at the ion-implanted region, even if metal impurities exist, the bonded two substrates are separated after achieving the gettering of the impurities into the ion-implanted region, and then the ion-implanted region is removed so that it is also effective against the impurity contamination.

Further, since the separating region is limited to the ion-implanted region within the porous layer, the depths of the separating region do not disperse within

the porous layer. Accordingly, even if the ratio of etching selectively porous silicon is insufficient, a time for removing porous silicon can be rendered substantially constant so that the thickness uniformity of the single-crystal silicon layer transferred onto the support substrate is not spoiled.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are schematic diagrams for explaining a semiconductor substrate producing process according to a first preferred embodiment of the present invention;

Figs. 2A to 2C are schematic diagrams for explaining a semiconductor substrate producing process according to a second preferred embodiment of the present invention;

Figs. 3A to 3C are schematic diagrams for explaining a semiconductor substrate producing process according to a third preferred embodiment of the present invention;

Figs. 4A to 4F are schematic diagrams for explaining a semiconductor substrate producing process according to a fourth preferred embodiment of the present invention;

Figs. 5A to 5F are schematic diagrams for explaining a semiconductor substrate producing process according to a fifth preferred embodiment of the

present invention;

Figs. 6A to 6E are schematic diagrams for explaining a semiconductor substrate producing process which has been proposed before;

Figs. 7A to 7E are schematic diagrams for explaining a conventional semiconductor substrate producing process;

Figs. 8A to 8E are schematic diagrams for explaining a semiconductor substrate producing process according to a sixth preferred embodiment of the present invention;

Figs. 9A to 9G are schematic diagrams for explaining a semiconductor substrate producing process according to a seventh preferred embodiment of the present invention;

Figs. 10A to 10G are schematic diagrams for explaining a semiconductor substrate producing process according to an eighth preferred embodiment of the present invention;

Figs. 11A and 11B are schematic diagrams for explaining anodization; and

Figs. 12A to 12D are sectional views showing a process of a EL element.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention simultaneously solves the foregoing various problems by superposing a finer

porous structure in the foregoing porous layer.

It has been reported that, by performing ion implantation of helium or hydrogen into bulk silicon and applying heat thereto, micro-cavities having diameters in the range from several nanometers to several tons of nanometers are formed at the implanted region in the density of as much as $10^{16}$ to $10^{17}/cm^3$ (for example, A. Van Veen, C.C. Griffioen, and J. H. Evans, Mat. Res. Soc. Symp. Proc. 107 (1988, Material Res. Soc. Pittsburgh, Pennsylvania) p. 449). Recently, it has been researched to utilize these micro-cavity groups as gettering sites of metal impurities.

V. Raineri and S.U. Campisano implanted helium ions into bulk silicon and applied a heat treatment thereto so as to form the cavity groups, then exposed the sides of the cavity groups by forming grooves in the substrate and applied an oxidation treatment thereto. As a result, the cavity groups were selectively oxidized so as to form a buried silicon oxide layer. That is, they reported that the SOI structure could be formed (V. Raineri and S.U. Campisano, Appl. Phys. Lett. 66 (1995) p. 3654). However, in their method, thicknesses of the surface silicon layer and the buried silicon oxide layer were so limited as to achieve both formation of the cavity groups and relaxation of stresses introduced due to volume expansion upon oxidation and further the

formation of the grooves were necessary for selective oxidation so that the SOI structure could not be formed all over the substrate. Such formation of the cavity groups have been reported as a phenomenon following the implantation of light elements into metal along with an expansion or separation phenomenon of the cavity groups as a part of the research about a first reactor wall of the nuclear fusion reactor.

Porous Si was found in the course of the research of electropolishing of the semiconductor in 1956 by Uhlir and collaborator (A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)). Porous silicon can be formed by anodizing the Si substrate in the HF solution. Unagami and collaborator researched the dissolution reaction of Si in the anodization and reported that positive holes were necessary for the anodizing reaction of Si in the HF solution and the reaction was as follows (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)):

$$Si + 2HF + (2-n)\ e^+ \rightarrow SiF_2 + 2H^+ + ne^-$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4-\lambda)\ e^+ \rightarrow SiF_4 + 4H^+ + \lambda e^-$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

wherein $e^+$ and $e^-$ represent a hole and an electron, respectively, and n and $\lambda$ represent the numbers of holes necessary for dissolution of one Si element,

respectively. It was reported that porous Si was formed when $n>2$ or $\lambda>4$ was satisfied.

As appreciated from the foregoing, p-type Si having the holes is rendered porous while n-type Si is not rendered porous. The selectivity while getting porous has been proved by Nagano and collaborators and Imai (Nagano, Nakajima, Yasuno, Oonaka, Kajiwara, Engineering Research Report of Institute of Electronics and Communication Engineers of Japan, vol. 79, SSD79-9549 (1979)), (K. Imai, Solid-State Electronics, vol. 24, 159 (1981)).

However, there have also been reports that high-concentration n-type Si can be rendered porous (R.P. Holmstrom and J.Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)) so that it is important to choose the substrate which can be rendered porous, irrespective of p- or n-type.

Porous silicon can be formed by anodizing the Si substrate in the HF solution. The porous layer has a structure like sponge including holes of about $10^{-1}$ to 10nm in diameter arranged at intervals of about $10^{-1}$ to 10nm. The density thereof can be changed in the range of 1.1 to 0.6g/cm$^3$ by changing the HF solution concentration in the range of 50 to 20% and by changing the current density, as compared with the density 2.33g/cm$^3$ of the single-crystal Si. That is, the porosity can be changed. Although the density of

porous Si is no more than half as compared with the single-crystal Si as described above, the monocrystalline property is maintained so that the single-crystal Si layer can be epitaxial-grown at the upper part of the porous layer. However, at the temperature no less than 1,000°C, rearrangement of the internal holes occurs to spoil the accelerating etching characteristic. In view of this, it has been said that the low temperature growth, such as the molecular beam epitaxial growth, the plasma CVD, the vacuum CVD, the optical CVD, the bias sputtering or the liquid deposition, is suitable for the epitaxial growth of the Si layer. On the other hand, if a protective film is formed in advance on the pore walls of the porous layer by means of the method of low temperature oxidation or the like, the high temperature growth is also possible.

Further, the porous layer is reduced in density to no more than half due to the formation of a lot of the internal cavities therein. As a result, since the surface area is greatly increased as compared with the volume, the chemical etching speed thereof is extremely increased as compared with the etching speed of the normal single-crystal layer.

Although the mechanical strength of porous Si differs depending on porosity, it is considered to be smaller than that of bulk Si. For example, if porosity is 50%, the mechanical strength can be considered to be

half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is first ruptured. As the porosity is increased, the porous layer can be ruptured with a weaker force.

The present invention simultaneously solves the foregoing various problems by superposing a finer porous structure in the foregoing porous layer.

It has been found that, when ion implantation of at least one kind of noble gas, hydrogen and nitrogen is performed into the porous layer with a projection range ensured, the porosity of the implanted region is increased. When observing in detail the implanted layer using an electron microscope, a lot of micro-cavities were formed in the pore walls of the porous layer formed in advance. Specifically, the fine porous structure was formed. Upon irradiation of ultraviolet light, the luminous phenomenon at the wavelength around 700nm was confirmed.

If choosing further implantation conditions, porous silicon can be separated at a depth corresponding to the projection range of the ion implantation.

The separation can be improved in uniformity or achieved with less implantation amount by forming in advance a thin film on the pore walls of porous silicon using the method of particularly low temperature

oxidation. The separation can be facilitated by applying the heat treatment after the ion implantation.

By ion-implanting at least one kind of noble gas, hydrogen and nitrogen into the porous layer with a projection range ensured after formation of at least one layer of non-porous film, such as a non-porous single-crystal silicon layer, on porous silicon or without such formation, the porosity of the implanted is increased. If such an Si substrate is bonded to the support substrate and then the bonded substrates are subjected to the mechanical force or the heat treatment, or even without such processes, the bonded two substrates can be separated into two at a portion of the porous silicon layer where ions are implanted.

By supporting both sides of the ion-implanted layer with a fully thick elastic or rigid body, the separation can be achieved uniformly over the large area. Further, it is possible to facilitate the separation of the substrates by applying the heat treatment, the force or the ultrasonic wave to the substrates.

Even if non-formation regions of the implanted layer are formed due to presence of the foreign matter on the surface upon the ion implantation, since the mechanical strength of the porous layer itself is smaller than bulk Si, the separation occurs in the porous layer. Thus, the bonded two substrates can be

separated without causing the cracks or the line in the non-porous single-crystal Si layer. In other words, the phenomenon of the separation can be selected by selecting a timing for the manifestation from the time of implantation and the time of heat treatment; and a condition of implantation such as an amount of implanted beam and energy thereof. Further, the layer having a large porosity may be formed at a region of a constant depth from the surface of the porous layer by controlling the condition at the anodization.

Further, by selectively removing the porous Si layer remaining on the surface of the separated substrate using the method of etching, polishing or the like, the single-crystal Si layer is exposed on the support substrate. On the other hand, after removing the remaining porous Si, the Si substrate can be again formed with porous silicon, then formed with a single-crystal Si layer and subjected to the ion implantation of at least one kind of noble gas, hydrogen and nitrogen into the porous layer with the projection range ensured, and then bonded to a support substrate. That is, the Si substrate can be recycled. Further, if the Si substrate, with the porous silicon layer remaining, is subjected to the heat treatment in the reduction atmosphere including hydrogen or the like, the porous silicon surface is rendered flat and smooth so that the single-crystal silicon layer can be formed

successively. By bonding the single-crystal silicon layer to the support substrate, the Si substrate can also be recycled.

According to this method, since the portion to be separated is limited to the ion-implanted region in the porous layer, the depth of the separated region is not dispersed in the porous layer. Thus, even if the ratio of etching selectively porous silicon is insufficient, porous silicon can be removed for substantially a constant time so that the uniformity of thickness of the single-crystal silicon layer provided on the support substrate is not spoiled.

In the conventional method of producing the bonded substrates, the Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the Si substrate is held in the initial state other than its surface layers so that, by using both sides of the Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one Si substrate. As appreciated, also in this case, the Si substrate can be recycled as an Si substrate after removing the remaining porous Si.

The support substrate may be, for example, a light transmittable substrate, such as an Si substrate, an Si substrate with a silicon oxide film formed thereon, a silica glass substrate or a glass substrate, or a metal substrate, but not particularly limited thereto.

The thin film formed on the porous Si layer on the Si substrate may be, for example, a non-porous single-crystal Si film, a compound semiconductor film of such as GaAs or InP, a metal film or a carbon film, but not particularly limited thereto. Further, the thin film is not necessarily formed all over the porous Si layer, but may be partially etched by the patterning process.

[First Embodiment]

As shown in Fig. 1A, an Si single-crystal substrate 11 is first prepared and then rendered porous at its surface layer. Numeral 12 denotes the obtained porous layer. As shown in Fig. 1B, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 12. Then, a porous layer 13 having large porosity is formed in the porous layer 12. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{13}/cm^2$ and more

preferably $1x10^{14}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is confirmed. Or an EL (Electroluminescence) element can be formed.

In Fig. 1B, the semiconductor substrate of the present invention is shown. The layer 13 is the porous Si layer with the large porosity obtained as the result of the foregoing ion implantation. The fine porous structure showing the luminous phenomenon is formed uniformly in large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the stain manner as in the prior art, so that metallic wiring can be easily arranged.

[Second Embodiment]

As shown in Fig. 2A, an Si single-crystal substrate 21 is first prepared and then rendered porous

at its surface layer. Numeral 22 denotes the obtained porous layer. As shown in Fig. 2B, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 22. Then, a porous layer (ion-implanted layer) 23 having large porosity is formed in the porous layer 22. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed or at least one of compressive, tensile and shear stresses is applied to the wafer in a direction perpendicular to the surface according to necessity, so as to divide the semiconductor substrate into two at the ion-implanted layer as a border. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

In Fig. 2C, the extremely thin porous substrate obtained by the present invention is shown. Since the

division of the substrate starts spontaneously upon the heat treatment or the like as a trigger due to the internal stress introduced upon the implantation, the extremely thin porous structure can be formed uniformly all over the substrate. The pores of the porous structure are formed from one main surface of the substrate toward the other main surface. Accordingly, when the gas is implanted under pressure from the one main surface, it is ejected out from the other main surface. In this case, since the pore size of the porous structure is in the range from several nanometers to several tens of nanometers, the particle greater than this can not pass therethrough. On the other hand, although the pressure loss is caused depending on the pore size, the pore density and a thickness of the extremely thin porous substrate, the strength of the substrate and the pressure loss can be both within the practical range if the thickness of the porous layer is approximately no more than 20μm.

[Third Embodiment]

As shown in Fig. 3A, an Si single-crystal substrate 31 is first prepared and then rendered porous at its surface layer. Numeral 32 denotes the obtained porous layer. Subsequently, as shown in Fig. 3B, at least one layer 33 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an

amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like.

As shown in Fig. 3C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 32. Then, a porous layer 34 having large porosity is formed in the porous layer 32. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is

confirmed. Or an EL element can be formed.

The EL element is realized by forming a construction where a voltage is applied to a porous layer having a large porosity formed in the porous layer by means of ion implantation and so forth. For example, when turning $p^+$ substrate 121 porous, the EL element is realized by implanting phospho-ion and so forth in porous layer 122 including porous layer 123 having a large porosity from the surface in a manner of making the ion reach a region of a constant depth from the surface, or by diffusing the ion by means of heat diffusion etc., to form a p-n junction in porous layer 123 having a large porosity or in neighborhood thereof. A portion 127 is an n-region of the porous layer having a large porosity, which region is obtained as a result of the above-mentioned process.

Electrodes 125 and 126 are secured with the substrate and the surface of the porous portion. The electrodes may be formed in the side of the surface of the porous portion by a process comprised of forming epitaxial Si layer 124 on the porous portion prior to the formation of the electrode and then forming the electrode thereon (see Fig. 12C). Further, as shown in Fig. 12D, the epitaxial Si layer may be removed partly as the occasion demands so as to facilitate the penetration of the light of the EL.

In Fig. 3B, the semiconductor substrate of the

present invention is shown. The fine porous structure showing the luminous phenomenon is formed uniformly in large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the cracks or the like as in the prior art, so that metallic wiring can be easily arranged.

[Fourth Embodiment]

As shown in Fig. 4A, an Si single-crystal substrate 41 is first prepared and then rendered porous at its surface layer. Numeral 42 denotes the obtained porous layer. Subsequently, as shown in Fig. 4B, at least one non-porous thin film 43 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed.

As shown in Fig. 4C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 42 so as to form an implanted layer 44. When observing the implanted layer by a transmission electron microscope, formation of numberless micro-cavities can be seen. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion

implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

As shown in Fig. 4D, after abutting a support substrate 45 and the surface of the first substrate with each other at room temperature, they are bonded to each other through anodic bonding, pressurization, heat treatment or a combination thereof. As a result, both substrates are firmly coupled with each other.

When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the support substrate can be selected from among an Si substrate, an Si substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the

bonding is fully flat. The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

Subsequently, the substrates are divided at the ion-implanted layer 44 in the porous Si layer 42 (Fig. 4E). The structure of the second substrate side includes the porous Si layer 42, the non-porous thin film (for example, the single-crystal Si layer) 43 and the second substrate 45.

Further, the porous Si layer 42 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 42 is subjected to the electroless wet chemical etching using at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remain on the second substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid due to the extensive surface area of porous Si. Alternatively, the porous Si layer 42 may be removed through selective polishing using the single-crystal Si

layer 43 as a polishing stopper.

In case of the compound semiconductor layer formed on the porous layer, only the porous Si layer 42 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so as to render the thickness-reduced single-crystal compound semiconductor layer 43 remain on the insulating substrate 45. Alternatively, the porous Si layer 42 is removed through selective polishing using the single-crystal compound semiconductor layer 43 as a polishing stopper.

In Fig. 4F, the semiconductor substrate of the present invention is shown. On the insulating substrate 45, the non-porous thin film, such as the single-crystal Si thin film 43, is formed in large area all over the wafer, flatly and uniformly reduced in thickness. The semiconductor substrate thus obtained can be suitably used also in view of production of the insulated electronic element.

The Si single-crystal substrate 41 can be reused as an Si single-crystal substrate 41 after removing remaining porous Si and after performing surface-flattening if the surface flat property is bad to an extent which is not admissible.

Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in Fig. 4B, which is then subjected

to the processes shown in Figs. 4C to 4F.

[Fifth Embodiment]

As shown in Fig. 5A, an Si single-crystal substrate 51 is first prepared and then rendered porous at both surface layers thereof. Numerals 52 and 53 denote the obtained porous layers. Subsequently, as shown in Fig. 5B, at least one non-porous thin film 54, 55 is formed on each of the porous layers. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed.

As shown in Fig. 5C, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layers 52 and 53 so as to form implanted layers 56 and 57. When observing the implanted layers by a transmission electron microscope, formation of numberless micro-cavities can be seen, and accordingly the porosity enlarges. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less

than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

As shown in Fig. 5D, after abutting two support substrates 58 and 59 and the surfaces of the non-porous thin films 54 and 55 of the first substrate with each other at room temperature, they are bonded to each other through anode bonding, pressurization, heat treatment or a combination thereof. As a result, the three substrates are firmly coupled with each other. Alternatively, the bonding may be performed in five plies with insulating thin plates interposed therebetween.

When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the support substrate can be selected from among an Si substrate, an Si substrate with a silicon oxide film formed thereon, a light transmittable substrate such as quartz, a sapphire substrate and the like, but not

limited thereto as long as the surface serving for the bonding is fully flat.

The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

Subsequently, the substrates are divided at the ion-implanted layers 56 and 57 in the porous Si layers 52 and 53 (Fig. 5E). The structure of each of the two support substrate sides includes the porous Si layer 52, 53, the non-porous thin film (for example, the single-crystal Si layer) 54, 55 and the support substrate 58, 59.

Further, the porous Si layer 52, 53 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 52, 53 is subjected to the electroless wet chemical etching using at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remain on the support substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid due to the extensive surface area of porous Si.

Alternatively, the porous Si layer 52, 53 may be removed through selective polishing using the single-crystal Si layer 54, 55 as a polishing stopper.

In case of the compound semiconductor layer formed on the porous layer, only the porous Si layer 52, 53 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so as to render the thickness-reduced single-crystal compound semiconductor layer 54, 55 remain on the insulating substrate. Alternatively, the porous Si layer 52, 53 is removed through selective polishing using the single-crystal compound semiconductor layer 54, 55 as a polishing stopper.

In Fig. 5F, the semiconductor substrates of the present invention are shown. On the support substrates, the non-porous thin films, such as the single-crystal Si thin films 54 and 55, are formed in large area all over the wafer, flatly and uniformly reduced in thickness, so that the two semiconductor substrates are simultaneously formed. The semiconductor substrates thus obtained can be suitably used also in view of production of the insulated electronic elements.

The first Si single-crystal substrate 51 can be reused as a first Si single-crystal substrate 51 after removing remaining porous Si and after performing

surface-flattening if the surface flat property is bad to an extent which is not admissible. Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in Fig. 5B, which is then subjected to the processes shown in Figs. 5C to 5F. The support substrates 58 and 59 are not necessarily identical with each other.

[Sixth Embodiment]

The sixth preferred embodiment will be described with reference to Figs. 8A to 8E.

First, a single-crystal Si substrate 100 is anodized to form a porous Si layer 101 (Fig. 8A). In this case, a thickness to be rendered porous is in the range from several micrometers to several tens of micrometers on one surface layer of the substrate. It may be arranged to anodize the whole Si substrate 100.

The method of forming porous silicon will be explained using Figs. 11A and 11B. First, as the substrate, a p-type single-crystal silicon substrate 600 is prepared. An n-type may also be used. However, in this case, it is necessary that the substrate is limited to a low-resistance substrate or that the light is applied onto the surface of the substrate so as to facilitate generation of the holes. The substrate 600 is set in an apparatus as shown in Fig. 11A. Specifically, one side of the substrate is in contact

with a hydrofluoric acid solution 604 having therein a negative electrode 606, while the other side of the substrate is in contact with a positive metal electrode 605. On the other hand, as shown in Fig. 11B, a positive electrode 605' may also be provided in a solution 604'. In any case, the substrate is first rendered porous from the negative electrode side abutting the hydrofluoric acid solution. As the hydrofluoric acid solution 604, concentrated hydrofluoric acid (49%HF) is used in general. As diluted by pure water ($H_2O$), although depending on current values, etching occurs from a certain concentration so that it is not preferable. During anodization, bubbles are generated from the surface of the substrate 600. Alcohol may be added as a surface active agent for effective removal of the bubbles. As alcohol, methanol, ethanole, propanol, isopropanol or the like is used. Instead of the surface active agent, an agitator may be used to agitate the solution so as to achieve anodization. The negative electrode 606 is made of a material, such as gold (Au) or platinum (Pt), which does not corrode relative to the hydrofluoric acid solution. A material of the positive electrode 605 may be metal which is used in general. On the other hand, since the hydrofluoric acid solution 604 reaches the positive electrode 605 when anodization is achieved relative to the whole substrate 600, it is

preferable to coat the surface of the positive electrode 605 with a metal film which is resistive to the hydrofluoric acid solution. The maximum current value for anodization is several hundreds of $mA/cm^2$, while the minimum current value therefor is arbitrary other than zero. This current value is determined in the range where the good-quality epitaxial growth is achieved on the surface of porous silicon. In general, as the current value increases, the anodization speed increases and the density of the porous Si layer decreases. That is, the volume of the pores increases. This changes the condition of the epitaxial growth.

On the porous layer 101 thus formed, a non-porous single-crystal silicon layer 102 is epitaxial-grown (Fig. 8B).

Subsequently, the surface of the epitaxial layer 102 is oxidized (including thermal oxidation) so as to form an $SiO_2$ layer 103 (Fig. 8C). This is necessary because, if the epitaxial layer is directly bonded to the support substrate in the next process, impurities tend to segregate at the bonded interface and dangling bonds of atoms at the interface increase, which will be causes for rendering unstable the characteristic of the thin film device. However, this process is not essential, but may be omitted in case of a device structure wherein such phenomena are not serious. The $SiO_2$ layer 103 works as an insulating layer of the SOI

substrate and should be formed on at least one side of the substrate to be bonded. There are various manners for formation of the insulating layer.

Upon oxidation, a thickness of the oxidized film is set to a value which is free of influence of contamination taken into the bonded interface from the atmosphere.

Thereafter, the foregoing ion implantation is performed so as to form a layer with large porosity in the porous Si layer 101.

The substrate 100 having the foregoing epitaxial surface with the oxidized surface and a support substrate 110 having an $SiO_2$ layer 104 on the surface are prepared. The support substrate 110 may be a silicon substrate whose surface is oxidized (including thermal oxidation), quartz glass, crystallized glass, an arbitrary substrate with $SiO_2$ deposited thereon, or the like. A silicon substrate without the $SiO_2$ layer 104 may also be used as the support substrate.

The foregoing two substrates are bonded together after cleaning them (Fig. 8D). The cleaning is performed pursuant to the process of cleaning (for example, before oxidation) the normal semiconductor substrate.

By pressurizing the whole substrates after the bonding, the bonding strength can be enhanced.

Subsequently, the bonded substrates are subjected

to the heat treatment. Although the higher temperature is preferable for the heat treatment, if it is too high, the porous layer 101 tends to cause the structural change or the impurities contained in the substrate tend to be diffused into the epitaxial layer. Thus, it is necessary to select temperature and time which does not cause them. Specifically, about 600 to 1,100°C is preferable. On the other hand, there is such a substrate that can not be subjected to the thermal treatment at the high temperature. For example, in case of the support substrate 110 being made of quartz glass, it can be subjected to the thermal treatment only at the temperature no greater than 200°C due to difference in thermal expansion coefficient between silicon and quartz. If exceeding this temperature, the bonded substrates may be separated or ruptured due to stress. The thermal treatment is sufficient as long as it can endure the stress upon grinding or etching of the bulk silicon 100 performed in the next process. Accordingly, even at the temperature no greater than 200°C, the process can be performed by optimizing the surface processing condition for activation.

Then, by the foregoing method, the substrates are separated into two at the porous Si layer having the large porosity. The layer having the large porosity can be formed by altering current in the anodization, besides the ion implantation.

Subsequently, the silicon substrate portion 100 and the porous portion 101 are selectively removed with the epitaxial layer 102 remaining (Fig. 8E). In this fashion, the SOI substrate is obtained.

The following processes may be added to the foregoing processes:

(1) A thickness of the wall between the adjacent holes in the oxidized (preoxidation) porous silicon layer of the pore internal walls of the porous layer is very small, that is, several nanometers to several tens of nanometers. Thus, if the high-temperature process is applied to the porous layer upon formation of the epitaxial silicon layer or upon heat treatment after bonding, the pore wall may agglomerate to be enlarged so that the pore wall may clog the pore to lower the etching speed. In view of this, after formation of the porous layer, a thin oxidized film is formed on the pore wall so as to suppress the enlargement of the pore wall. On the other hand, since it is necessary to epitaxial-grow the non-porous single-crystal silicon layer on the porous layer, it is necessary to oxidize only the surface of the pore inner wall such that the monocrystalline property remains inside the pore wall of the porous layer. It is preferable that the oxidized film to be formed is in the range of several angstroms to several tens of angstroms. The oxidized film of such a thickness is formed through the heat

treatment in the oxygen atmosphere at the temperature of 200°C to 700°C, and more preferably 250°C to 500°C.

(2) Hydrogen Baking Process

The present inventors have shown in the Publication No. EP553852A2 that, through the heat treatment in the hydrogen atmosphere, small roughness on the silicon surface can be removed to obtain the very smooth silicon surface. Also in the present invention, the baking in the hydrogen atmosphere can be applied. The hydrogen baking can be performed, for example, after formation of the porous silicon layer and before formation of the epitaxial silicon layer. Apart from this, the hydrogen baking can be performed to the SOI substrate obtained after etching removal of the porous silicon layer. Through the hydrogen baking process performed before formation of the epitaxial silicon layer, a phenomenon that the pore surface is closed due to migration of silicon atoms forming the porous silicon surface. When the epitaxial silicon layer is formed in the state where the pore surface is closed, the epitaxial silicon layer with less crystal defects can be achieved. On the other hand, through the hydrogen baking process performed after etching of the porous silicon layer, the epitaxial silicon surface which was more or less roughened by etching can be smoothened, and boron from the clean room inevitably taken into the bonded interface upon bonding and boron

thermally diffused in the epitaxial Si layer from the porous Si layer can be removed.

[Seventh Embodiment]

The seventh preferred embodiment will be described with reference to Figs. 9A to 9G. Numerals in Figs. 9A to 9G which are the same as those in Figs. 8A to 8E represent the same portions in Figs. 8A to 8E. In the embodiment shown in Figs. 8A to 8E, the surfaces of the two substrates to be bonded are the $SiO_2$ layer 103 and the $SiO_2$ layer 104. However, both of these surfaces are not necessarily the $SiO_2$ layers, but at least one of them may be made of $SiO_2$. In this preferred embodiment, the surface of an epitaxial silicon layer 1102 formed on a porous silicon layer is bonded to the surface of an oxidized film 1104 formed on a silicon substrate 1110, and the surface of an oxidized film 1103 formed by thermal oxidation of the surface of the epitaxial silicon layer 1102 is bonded to the surface of the silicon substrate 1110 which is not oxidized. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs. 8A to 8E.

[Eighth Embodiment]

The eighth preferred embodiment will be described with reference to Figs. 10A to 10G. Numerals in Figs. 10A to 10G which are the same as those in Figs. 8A to 8E represent the same portions in Figs. 8A to 8E. In this preferred embodiment, it is characterized in that

a substrate bonded to a substrate formed with an epitaxial silicon film is made of a glass material 1210, such as quartz glass or blue glass. In this preferred embodiment, an epitaxial silicon layer 1102 is bonded to the glass substrate 1210, and an oxidized film 1103 formed by thermal oxidation of the surface of the epitaxial silicon layer 1102 is bonded to the glass substrate 1210. In this preferred embodiment, the other processes can be performed as in the embodiment shown in Figs. 8A to 8E.

Hereinbelow, the present invention will be described in detail using concrete examples. However, the present invention is not limited thereto.

[Example 1]

A first p- or n-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

Subsequently, $He^+$ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 30keV. Then, the substrate was subjected to

the heat treatment at 850°C in the vacuum for 8 hours.

When the light of a mercury lamp was applied to the substrate, luminescence of the red light with wavelength around 750nm was confirmed.

[Example 2]

Two first p-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared, and one of them was anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

$He^+$ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 100keV. Then, these substrates were subjected to the heat treatment at 850°C in the vacuum for 8 hours. Further, ITO electrodes were deposited on the surfaces.

When the voltage was applied between the Si substrates and the ITO electrodes, luminescence of

wavelength around 750nm was confirmed at the porous substrate, while luminescence was not confirmed at the other substrate.

[Example 3]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared, and one of them was anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 20 (μm)

Porosity: 15 (%)

The anodized substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with a thermal-oxidized film. Subsequently, hydrogen ions of $1x10^{17}/cm^2$ were implanted all over the porous side of the porous substrate and all over the other substrate at acceleration voltage of 0.76MeV.

When these substrates were subjected to the heat treatment at 1,000°C in the vacuum for 1 hour, the porous layer was separated uniformly all over the substrate with a thickness of about 1μm corresponding to the ion-implanted region, while a lot of swells like blisters were only formed at the non-porous substrate.

[Example 4]

A first p-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with a thermal-oxidized film. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.1mm on porous Si. The growing condition was as follows:

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

$He^+$ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized

substrate and the surface side of the other substrate at acceleration voltage of 100keV. Then, these substrates were subjected to the heat treatment at 850°C in the argon atmosphere for 8 hours. Further, ITO electrodes were deposited on the surfaces.

When the voltage was applied between the Si substrate and the ITO electrode, luminescence of wavelength around 750nm was confirmed at the porous substrate.

[Example 5]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 3 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing condition was as follows:

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, $He^+$ ions of $1x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 50keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support Si substrate formed with an $SiO_2$ layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 1,000°C for 2 hours so as to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, no change on the outward appearance was caused on the substrate which was not subjected to the helium ion implantation, and the substrates remained bonded to each other. Thus, the porous Si substrate side of the bonded substrates (not subjected to the helium ion implantation) was

ground using a grinder for the normal semiconductor so as to expose the porous Si layer. However, due to insufficient grinding accuracy, the whole porous layer could not be exposed.

Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of etching selectively relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. No change was caused on the single-crystal Si layer even by the selective etching of porous Si.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 6]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, hydrogen ions of $5x10^{16}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 50keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support Si substrate formed with an $SiO_2$ layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 1,000°C for 2 hours so as to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, no change on the outward appearance was caused on the substrate which was not subjected to the hydrogen ion implantation, and the substrates remained bonded to each other. The porous substrate side of the bonded substrates (not subjected to the hydrogen ion implantation) was ground using a grinder for the normal semiconductor so as to expose the porous layer. However, due to insufficient grinding accuracy, a thickness of the remaining porous layer was 1 to 9μm.

Thereafter, the porous Si layer remaining on the

support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of etching selectively relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 101nm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon.

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness

at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 7]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, hydrogen ions of $5x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. The sufficient pressure is applied

to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the porous Si layer was divided into two at the ion-implanted region.

On the other hand, when the pressure was further applied to the substrate (not subjected to the hydrogen ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.5μm in thickness was formed on the Si oxidized film.

Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11nm with the hydrogen ion implantation.

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

Using the CVD (chemical vapor deposition) method, single-crystal Si was again epitaxial-grown by 0.55μm on porous Si remaining at the first substrate side. The growing condition was as follows. The accuracy of the film thickness was ±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 1/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

When evaluating the crystal defect density of this single-crystal Si layer through the defect revealing etching, the defect density was about $1x10^3/cm^2$ and this substrate could be again put into the processes of ion implantation and bonding.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 8]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA•cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was

±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, helium ions of $1x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support Si substrate formed with an $SiO_2$ layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 400°C for 2 hours. The sufficient tensile force is applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the two substrates were completely separated at a position corresponding to the projection range of the helium ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found.

On the other hand, when the pressure was further applied to the substrate (not subjected to the helium

ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 101nm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to

influence of dispersion of thicknesses of porous silicon.

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 9]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in

resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal Si was epitaxial-grown by 0.5μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

Temperature: 700°C

Pressure: $1 \times 10^{-9}$ Torr

Growing Speed: 0.1 nm/sec

Temperature: 950 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, helium ions of $1 \times 10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

The surface of the $SiO_2$ layer and the surface of a

separately prepared support Si substrate formed with an $SiO_2$ layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 300°C for 2 hours. The bonded two wafers were fixed by a vacuum chuck and applied with torsion and shearing forces in the horizontal direction relative to the main surface of the wafers. Then, the two substrates were completely separated at a position corresponding to the projection range of the helium ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found.

On the other hand, when the pressure was further applied to the substrate (not subjected to the helium ion implantation), the vacuum chuck was detached and the substrate could not be put into the subsequent process.

Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of

the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 101nm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon.

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si

layer.

At the same time, the porous Si layer remaining on the Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porous-forming process.

[Example 10]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was

±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

On the other hand, no change was observed at the substrate which was not subjected to the helium ion implantation.

Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was

selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.5μm in thickness was formed on the quartz substrate. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming

the oxidized film on the surface of the epitaxial Si layer.

[Example 11]

A first p- or n-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MOCVD (metal organic chemical vapor deposition) method, single-crystal GaAs was epitaxial-grown by 1μm on porous Si. The growing condition was as follows.

Source Gas: $TMG/AsH_3/H_2$

Gas Pressure: 80 Torr

Temperature: 700°C

Subsequently, helium ions of $1x10^{18}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 100keV.

The surface of the GaAs layer and the surface of a

separately prepared support Si substrate were overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to enhance the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

Thereafter, after removing the oxidized film on the inner walls of the porous Si layer using hydrofluoric acid, the porous Si was etched with a solution of ethylenediamine, pyrocatechol and water (ratio: 17ml:3g:8ml) at 110°C. Single-crystal GaAs remained without being etched so that porous Si was selective-etched using single-crystal GaAs as etching stopper and fully removed.

The etching speed of single-crystal GaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

Specifically, the single-crystal GaAs layer having 1μm in thickness was formed on the Si substrate. No change was caused on the single-crystal GaAs layer even by the selective etching of porous Si.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the GaAs layer and the excellent crystalline property was maintained.

By using the Si substrate with the oxidized film

as the support substrate, GaAs on the insulating film could also be produced similarly.

[Example 12]

A first p- or n-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 10 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 24 (minutes)

Thickness of Porous Si: 20 (μm)

Porosity: 17 (%)

The substrate was oxidized at 400°C in the oxygen atmosphere for 2 hours. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal AlGaAs was epitaxial-grown by 0.5μm on porous Si.

Subsequently, helium ions of $1x10^{18}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 100keV.

The surface of the AlGaAs layer and the surface of a separately prepared support substrate of low melting point glass were overlapped and abutted with each other, and subjected to the heat treatment at 500°C for 2 hours. Through this heat treatment, the substrates

were firmly bonded with each other.

When the sufficient pressure was applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane, the porous Si layer was divided into two at the ion-implanted region.

Thereafter, porous Si was etched with a hydrofluoric acid solution. Single-crystal AlGaAs remained without being etched so that porous Si was selective-etched using single-crystal AlGaAs as etching stopper and fully removed.

The etching speed of single-crystal AlGaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

Specifically, the single-crystal AlGaAs layer having 0.5μm in thickness was formed on the glass substrate. No change was caused on the single-crystal AlGaAs layer even by the selective etching of porous Si.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the AlGaAs layer and the excellent crystalline property was maintained.

[Example 13]

A first p- or n-type (100) single-crystal Si substrate with both sides polished and having 625μm in

thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was prepared and anodized at both sides thereof in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 x 2 (minutes)

Thickness of Porous Si: 10 (μm) for each side

Porosity: 15 (%)

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 1μm on porous Si formed at each side. The growing condition was as follows.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous layers at acceleration voltage of 100keV.

The surfaces of the $SiO_2$ layers and the surfaces of separately prepared two support Si substrates each formed with an $SiO_2$ layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 600°C for 2 hours so as to achieve bonding. Then, the porous Si layer was divided into two at the ion-implanted region.

Thereafter, the porous Si layer was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the two single-crystal Si layers each having 1μm in thickness were simultaneously formed on the Si oxidized films. No change was caused on the single-crystal Si layers even by the selective etching of porous Si.

As the result of section observation by a transmission electron microscope, it was confirmed that

no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[Example 14]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

The anodization condition was as follows:

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

Source Gas: $SiH_2Cl_2/H_2$

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

Further, an $SiO_2$ layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

Subsequently, hydrogen ions of $1x10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

The surface of the $SiO_2$ layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. Subsequently, the wave energy such as the ultrasonic wave was applied to the substrates. Then, the porous Si layer was divided into two at the ion-implanted region.

On the other hand, no change was observed at the substrate which was not subjected to the hydrogen ion implantation.

Thereafter, the porous Si layer remaining on the support substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% hydrogen peroxide water for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching

stopper and fully removed.

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than $10^5$ and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

Specifically, the single-crystal Si layer having 0.5μm in thickness was formed on the quartz substrate. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501nm ± 11nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystalline property was maintained.

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si

layer.

The single-crystal Si substrate was reused as a single-crystal Si substrate after removing remaining porous Si and performing surface-polishing to provide a mirror finished surface.

WHAT IS CLAIMED IS:

1. A semiconductor substrate producing method comprising:

a porous-forming step for forming a porous Si layer on at least a surface of an Si substrate; and

a large porosity layer forming step for forming large porosity layer at a constant depth from a surface of said porous Si in said porous Si layer.

2. The semiconductor substrate producing method according to claim 1, wherein said large porosity layer forming step has an ion implanting step for implanting ions into said porous Si layer with a given projection range.

3. The semiconductor substrate producing method according to claim 2, further comprising a non-porous layer forming step for forming a non-porous layer on a surface of said porous layer before said ion implanting step.

4. The semiconductor substrate producing method according to claim 2, wherein said ions comprises at least one kind of noble gas, hydrogen and nitrogen.

5. The semiconductor substrate producing method according to claim 3, further comprising a bonding step

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for bonding said non-porous layer and a support substrate together; and a separating step for separating said Si substrate into two at said large porosity layer.

6. The semiconductor substrate producing method according to claim 5, wherein said separating step is performed by heat-treating said Si substrate.

7. The semiconductor substrate producing method according to claim 5, wherein said separating step is performed by pressurizing said Si substrate in a direction perpendicular to a surface thereof.

8. The semiconductor substrate producing method according to claim 5, wherein said separating step is performed by drawing said Si substrate in a direction perpendicular to a surface thereof.

9. The semiconductor substrate producing method according to claim 5, wherein said separating step is performed by applying a shearing force to said Si substrate.

10. The semiconductor substrate producing method according to claim 3, wherein said non-porous layer is made of single-crystal Si.

11. The semiconductor substrate producing method according to claim 3, wherein said non-porous layer is made of single-crystal Si having an oxidized Si layer on a surface to be bonded.

12. The semiconductor substrate producing method according to claim 3, wherein said non-porous layer is made of a single-crystal compound semiconductor.

13. The semiconductor substrate producing method according to claim 5, wherein said support substrate is an Si substrate.

14. The semiconductor substrate producing method according to claim 5, wherein said support substrate is an Si substrate having an oxidized Si layer on a surface to be bonded.

15. The semiconductor substrate producing method according to claim 5, wherein said support substrate is a light transmittable substrate.

16. The semiconductor substrate producing method according to claim 5, wherein said bonding step is performed by anode bonding, pressurization, heat treatment or a combination thereof.

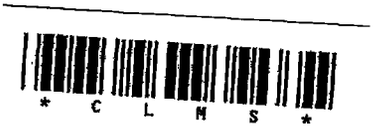
17. The semiconductor substrate producing method according to claim 5, further comprising a porous Si removing step, after said separating step, for removing the porous Si layer exposed on a surface of said support substrate and exposing said non-porous layer.

18. The semiconductor substrate producing method according to claim 17, wherein said porous Si removing step is performed by an electroless wet etching using at least one of hydrofluoric acid, a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and hydrogen peroxide water to buffered hydrofluoric acid.

19. The semiconductor substrate producing method according to claim 17, further comprising a flattening step for flattening a surface of said non-porous layer after said porous Si removing step.

20. The semiconductor substrate producing method according to claim 19, wherein said flattening step is performed by heat treatment in the atmosphere including hydrogen.

21. The semiconductor substrate producing method



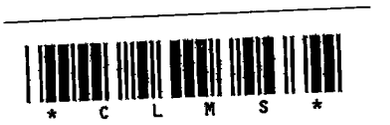

according to claim 5, wherein said porous-forming step forms porous Si layers on both sides of said Si substrate, and said bonding step bonds two support substrates to said porous Si layers formed on both sides of said Si substrate.

22. The semiconductor substrate producing method according to claim 5, further comprising a second non-porous layer forming step, after said separating step, for forming non-porous layer again on the surface of said porous Si layer, and a second ion implanting step, after said second non-porous layer forming step, for implanting ions into said porous Si layer with a given projection range and forming large porosity layer in said porous Si layer.

23. The semiconductor substrate producing method according to claim 1, wherein said porous-forming step is performed by anodization.

24. The semiconductor substrate producing method according to claim 23, wherein said anodization is performed in an HF solution or a mixture of an HF solution and alcohol.

25. The semiconductor substrate producing method according to claim 1, wherein said large porosity layer




forming step is performed by changing a current density of anodization in said porous-forming step.

26. A semiconductor substrate comprising:

a porous Si layer formed at a surface layer of an Si substrate; and

a large porosity layer formed in said porous Si layer wherein said large porosity layer exists in a region located at a constant depth from a surface of said porous Si layer.

27. The semiconductor substrate according to claim 26, wherein non-porous si layer exists on surface of said porous si layer, and electrodes are formed on surface of said non-porous Si layer and on surface of said Si substrate, in order that said semiconductor substrate becomes an EL element.